TB3200

UART with DALI Protocol Technical Brief

Introduction

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The Digital Addressable Lighting Interface (DALI) is an international standard that governs intelligent lighting control. DALI was developed to replace analog lighting control with a flexible digital control system. Microchip's Universal Asynchronous Receiver Transmitter (UART) module has added protocol support features that simplify DALI usage. This technical brief will give a short summary of the DALI protocol and explain how to use the UART module for DALI control.

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1. DALI Overview

Lighting systems were originally designed for one purpose: to provide light for visual tasks. A simple light switch either turned on or turned off the system, while a dimmer switch changed the intensity of a lighting fixture's output. If a fixture burned out, it could be replaced, but there was no assurance that the new light would behave the same as other fixtures within the system. If the new fixture was brighter or dimmer than the other fixtures, the overall lighting would not be uniform across the area being illuminated. Other than physically noticing that a fixture needed to be replaced, there was not a way to detect if a fixture was operational.

Today, the demand for power efficiency and customization has led to the design of intelligent lighting control systems. The DALI protocol was designed to meet these demands.

DALI lighting systems have several advantages over traditional analog lighting systems, including:

- Simple wiring of control lines
- Control of individual units or groups of units through addressing
- Simultaneous control of all units through broadcast addressing
- Simple communication structure
- Ability to check the status of an individual or group of fixtures for faults, power levels, etc.
- Creation of custom lighting scenes
- Logarithmic dimming that matches the eye's sensitivity
- More functionality and lower-system cost compared to 1-10V systems

1.1 DALI Terminology

The list below contains basic DALI terminology used in the protocol:

- Control Device: A device that transmits commands to other devices connected to the same bus. A control device can also receive commands and backward frames.
- Control Gear: A device that receives commands in order to control its output.
- Ballast: An electronic device that regulates current and voltage to the lamp.
- Frame: A packet of information consisting of a Start bit, command/data byte(s), and a Stop condition.
- Forward Frame: The frame sent by the control device to the control gear. A forward frame consists of a Start bit, an address byte, up to two data bytes, and a Stop condition.
- Backward Frame: The frame sent back to the control device from a responding control gear. The backward frame consists of a Start bit, one data byte, and a Stop condition.
- Command: A specific instruction intended to cause a reaction in a receiver.
- Short Address: The address of an individual control gear within the system.
- Group Address: The address of a group of control gears within the system.
- Broadcast: The address used to communicate with all control gears within the system.
- Arc Power: Power supplied to the lighting source.
- Direct Arc Power Control (DAPC): A method that immediately sets an individual or multiple control gears to a specific power level.
- Scene: A configurable preset lighting level.

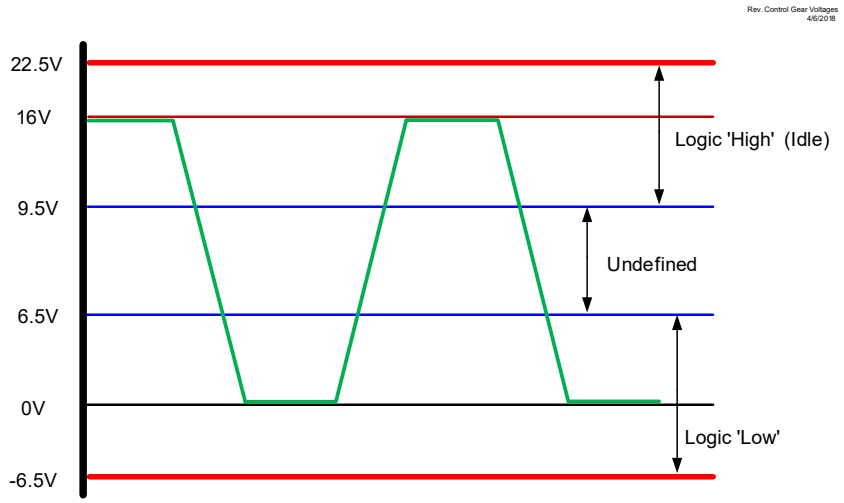
- Building Management System (BMS): A computer-based control system installed in buildings that controls and monitors the mechanical and electrical equipment of a building.

1.2 Electrical Specifications

The DALI bus operates at a nominal voltage range between 0V and 20.5V, and an absolute maximum voltage range between -6.5V and 22.5V. The maximum allowable voltage drop across the bus is 2V. The maximum current of the DALI bus is 250 mA, with each unit on the bus limited to a maximum current consumption of 2 mA.

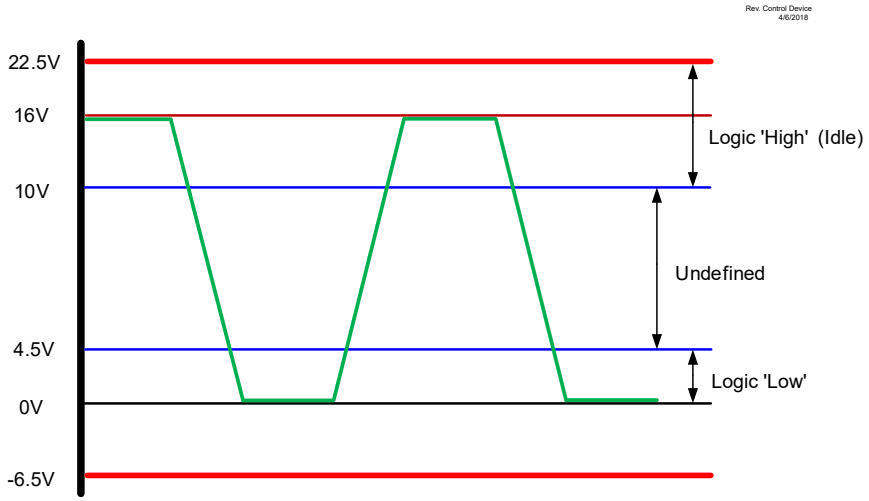
A Control Gear's logic 'high' level falls within the range of 9.5V and 20.5V, although the most common is 16V. A logic 'low' level falls between +6.5V and -6.5V. The threshold (undefined) voltage region falls between 6.5V and 9.5V (see figure below).

Figure 1-1. Control Gear Voltages



A Control Device's logic 'high' level falls in the range of 10V and 22.5V. A logic 'low' level falls between 0V and 4.5V. The threshold (undefined) voltage region falls between 4.5V and 10V (see figure below).

Figure 1-2. Control Device Voltages



The bus may have a single power supply, multiple power supplies, or a power supply that has been integrated into one of the ballasts. The output voltage of the bus power supply must be between 12V and 20.5V.

1.3 Bus Topology

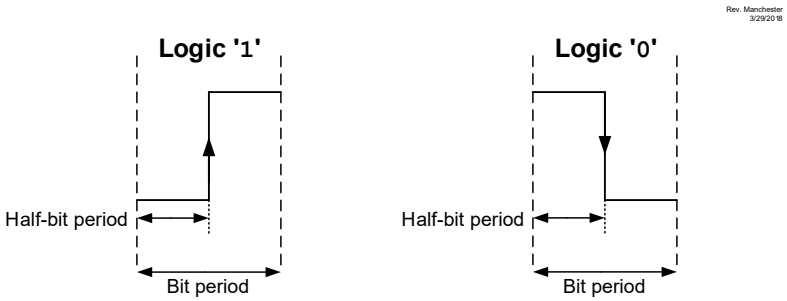
The DALI protocol limits the system to a maximum of sixty-four single units, a maximum of sixteen groups, and a maximum of sixteen scenes. Each of the sixty-four single units is assigned a short address, which is stored within the ballast. Each individual unit may also contain a group assignment number, lighting scene values, fading times, and emergency lighting levels. Short addresses may be programmed into the ballast by the manufacturer during production, or may be programmed by the designer during the installation process. Group addresses are typically assigned by software during installation, allowing for future changes in the group structure.

DALI has a free-form wiring structure, so the use of daisy-chained, linear, star, or mixed structure wiring connections are allowed, with the exception of ring-shaped connection structures. DALI sets a maximum distance of 300 meters between unit connections, and allows a maximum of a 2-volt drop across the connecting wires from the interface power supply to each unit. The DALI bus operates at a 1200 bps baud rate, so there is no need for special cables or wires.

1.4 Bus Communication

DALI frames (data packets) are created using Manchester (bi-phase) encoding, which is done through UART hardware. The Manchester code is a digital encoding format in which a logic '1' represents a rising-edge transition that occurs during a bit period, while a logic '0' represents a falling-edge transition during a bit period (see figure below). Start and Stop bits are encoded as a logic '1'.

Figure 1-3. Manchester Bit Encoding



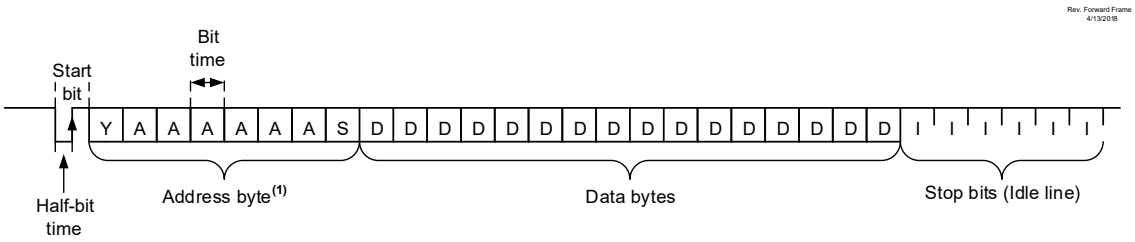
Frames are transmitted at a baud rate of 1200 bps, and each frame is always sent with the Most Significant bit (MSb) first. Since the baud rate is 1200 bps, each bit period lasts for 833.33 µs, and each half-bit last for 416.67 µs. Half-bit period times are important since Manchester encoding requires two-bit transitions for each logical data bit.

A forward frame is the data packet transmitted by the control device to the control gear or input device.

A DALI 1.0 forward frame contains the Start bit, followed by the address byte, one data byte, and two Stop bits.

A DALI 2.0 forward frame contains the Start bit, followed by the address byte, up to two data bytes, and a Stop condition (see Figure 1-4). The DALI 2.0 24-bit forward frame, including the Start and Stop bits, lasts for 23.2 ms, or approximately 56 half-bit times, while the 16-bit forward frame lasts for 16.2 ms, or 39 half-bit periods. Once the control device completes the transmission of the frame, the control gear must begin to transmit the backward frame no sooner than 5.5 ms (approximately 14 half-bit times) and no later than 10.5 ms (approximately 25 half-bit periods). Once the backward frame has been received in its entirety, the control device must wait a minimum of 2.4 ms (approximately six half-bit periods) before transmitting the next forward frame (see Figure 1-5).

Figure 1-4. DALI Forward Frame



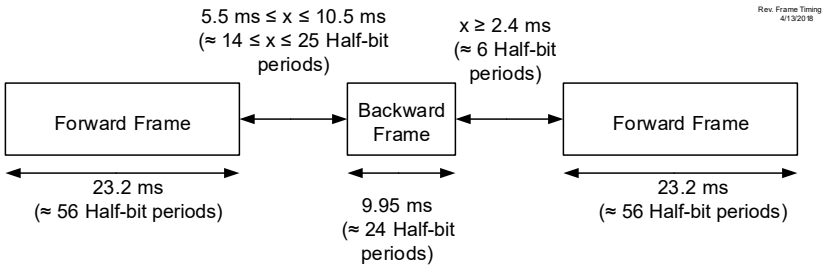
Note 1: The addressing scheme for the Address byte is as follows:

Y: Address type bit
Y = 0: Indicates an individual or short address
Y = 1: Indicates a group address or broadcast

A: Address bits

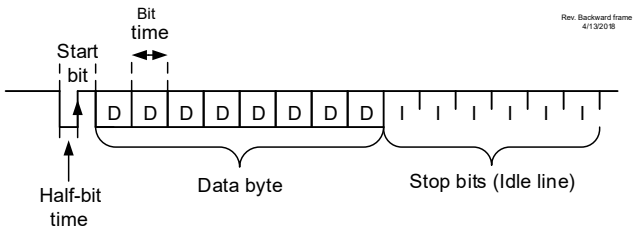
S: Selector bit
S = 0: Data bytes indicate Direct Arc Power level
S = 1: Data bytes indicate a command

Figure 1-5. DALI Frame Timing



A backward frame is the response packet transmitted from the control gear to the control device. A backward frame consists of the Start bit, one data byte, and a Stop condition (see figure below). A backward frame, including the Start and Stop bits, lasts for 9.95 ms (approximately 24 half-bit periods). The data byte may be of any value, depending on the command that was issued by the control device. If a backward frame's data byte is 0xFF, the response is considered a 'yes'. If a response is expected and the bus remains Idle, the response is considered a 'no'.

Figure 1-6. DALI Backward Frame



2. Configuring the UART for DALI

The UART module can be configured for DALI mode communication via the UART Mode Select (MODE<3:0>) bits of the UART Control Register 0 (UCON0). There are two selections for DALI – either Control Device mode or Control Gear mode.

2.1 DALI Control Device Mode

The DALI Control Device mode is configured using the following settings:

- Load the MODE<3:0> bits of U1CON0 with '0b1000', placing the UART into Control Device mode.
- Set the Transmit Enable Control (TXEN) bit of U1CON0 to allow transmission.
- Set the Receive Enable Control (RXEN) bit of U1CON0 to allow reception.
- Load the UART Parameter 1 Register (U1P1H:U1P1L) pair with the number of half-bit periods of Idle time between consecutive forward frame transmissions. In this case, the minimum value loaded should be 0x16, or 22 half-bit periods.
- Load the UART Parameter 2 Register (U1P2H:U1P2L) pair with the number of half-bit periods of idle time used to determine if the frame is a forward frame. If a frame is received before the half-bit delay expires, it is considered a backward frame. If reception occurs after the half-bit period delay expires, the frame is detected as a forward frame, and sets the Parity Error Interrupt Flag (PERIF) bit of the UART Error Interrupt Flag Register (U1ERRIR).
- Load the value used to achieve a 1200 baud rate into the UART Baud Rate Generator Register (U1BRGH:U1BRGL) pair.
- Configure the Transmit Polarity Control (TXPOL) bit of the UART Control Register 2 (U1CON2) to match the appropriate output polarity of the interface circuit.
- Configure the Receive Polarity Control (RXPOL) bit of U1CON2 to match the appropriate input polarity of the interface circuit.
- Load the value '0b10' into the Stop Bit Mode Control (STP<1:0>) bits of U1CON2 to ensure the frames contain two Stop bits as required by the DALI protocol.
- Load the RxyPPS register (PPS output) with the Tx pin selection code to map the Tx output to the desired pin.
- Configure the U1RXPPS register to match the desired input pin.
- Clear the TRIS bit associated with the Tx output pin.
- Set the TRIS bit associated with the Rx input pin.
- Clear the ANSEL bit associated with the Rx input pin.
- Set the Serial Port Enable (ON) bit of U1CON1.

A forward frame is initialized by writing the address byte into the UART Transmit Register (U1TXB). If there is no data residing in the Transmit Shift Register (TSR), the address byte is immediately transferred to the TSR, allowing the first data byte to be written into U1TXB. Once the TSR shifts out the address byte, the data in U1TXB is transferred into the TSR, setting the UART Transmit Interrupt Flag (U1TXIF) bit.

Once the U1TXIF is set, but before the Transmit Shift Register Empty Interrupt Flag (TXMTIF) bit of the U1ERRIR register is set, the next data byte must be loaded into U1TXB to ensure that each byte within the frame is transmitted without an interruption. The TXMTIF bit is set once the TSR has shifted out the last byte and there is no data in the U1TXB register, indicating the end of the frame. When TXMTIF is set,

hardware holds the Tx output in the Idle state for the number of Stop bits selected by the STP<1:0> bits of U1CON2.

After the last Stop bit has been transmitted, the Tx output is held in the Idle state for the number of half-bit times found in the U1P1H:U1P1L register pair. Any writes to the U1TXB register that occur after TXMTIF has set but before the U1P1 wait time expires are held in U1TXB. Once the wait time expires, the data is immediately transmitted. If a backward frame is received during the wait time, any data written into U1TXB will be held until the complete reception of the backward frame plus the additional U1P1 wait time.

Once the two Stop bits of a backward frame have been received, the U1P1 wait timer resets and restarts its timing function. Any data pending in the TSR will be transmitted once the wait time elapses.

Forward frame data stored in the TSR and U1TXB can be replaced or deleted by setting the Transmit Buffer Empty Status (TXBE) bit of the UART FIFO Status register (U1FIFO). Setting TXBE flushes any data left in both the TSR and the U1TXB registers. It is important to note that the TXBE bit can only be cleared by hardware, and is clear whenever there is data in either the TSR or U1TXB.

It is important to note that backward frames are automatically received, and may or may not arrive within the allowed time window. If the backward frame arrives outside of the time window and collides with a forward frame, the Transmit Collision Interrupt Flag (TXCIF) bit of the U1ERRIR register is set. If the backward frame arrives outside of the time window and no collision occurs, the module continues normal operation. TXCIF will also be set when a received bit is missing the half-bit transition.

2.2 DALI Control Gear Mode

The DALI Control Gear mode is configured using the following settings:

- Load the MODE<3:0> bits of U1CON0 with '`0b1001`', placing the UART into Control Gear mode.
- Set the Transmit Enable Control (TXEN) bit of U1CON0 to allow transmission.
- Set the Receive Enable Control (RXEN) bit of U1CON0 to allow reception.
- Load the UART Parameter 1 Register (U1P1H:U1P1L) pair with the number of half-bit periods of Idle time between the reception of forward frame and the transmission of a backward frame. The allowable time frame is between 5.5 ms and 10.5 ms, so loading a value of 0x16 (22 half-bit periods or 9.17 ms) will meet the timing requirements.
- Load the UART Parameter 2 Register (U1P2H:U1P2L) pair with the number of half-bit periods of Idle time used to determine if the frame is a forward frame. If a frame is received before the half-bit delay expires, it is considered a backward frame. If reception occurs after the half-bit period delay, the frame is detected as a forward frame, and sets the Parity Error Interrupt Flag (PERIF) bit of the UART Error Interrupt Flag Register (U1ERRIR).
- Load the value used to achieve a 1200 baud rate into the UART Baud Rate Generator Register (U1BRGH:U1BRGL) pair.
- Configure the Transmit Polarity Control (TXPOL) bit of the UART Control Register 2 (U1CON2) to match the appropriate output polarity of the interface circuit.
- Configure the Receive Polarity Control (RXPOL) bit of U1CON2 to match the appropriate input polarity of the interface circuit.
- Load the value '`0b10`' into the Stop Bit Mode Control (STP<1:0>) bits of U1CON2 to ensure the frames contain two Stop bits as required by the DALI protocol.
- Load the RxyPPS register (PPS output) with the Tx pin selection code to map the Tx output to the desired pin.

- Configure the U1RXPPS register to match the desired input pin.
- Clear the TRIS bit associated with the Tx output pin.
- Set the TRIS bit associated with the Rx input pin.
- Clear the ANSEL bit associated with the Rx input pin.
- Set the Serial Port Enable (ON) bit of U1CON1.

When the UART is set into Control Gear mode and the serial port is enabled, the UART begins to monitor for a received forward frame. Frames that are received after the U1P2 wait time expires are detected as a forward frame and are stored in the receive FIFO; if a frame is received before the U1P2 wait time expires, the frame is detected as a backward frame and ignored since a control gear can only receive forward frames. Backward frames from other Control Gear are ignored.

Once the Control Gear receives the last Stop bit of the forward frame, hardware starts a timer to delay the backward frame response by the number of half-bit periods stored in the U1P1 register.

The data received in the forward frame is processed by the Control Gear's application software. If a response is required, the application software writes the backward frame into U1TXB. The frame is held for transmission until the wait time delay expires. If the response is written into U1TXB after the wait time delay expires, the TXMTIF bit is held low, and the response is held in U1TXB until a new forward frame is received and the wait time associated to that frame has expired. If the UART Receive Interrupt Flag (U1RXIF) bit is set before TXMTIF becomes set, it means that a new forward frame was received before the pending backward frame was sent. In this case, the pending backward frame may hold an incorrect response to the new forward frame, therefore, the pending backward frame can be deleted by setting the TXBE bit.

3. Conclusion

The Digital Addressable Lighting Interface (DALI) protocol is a commercial and industrial standard related to digitally controlled lighting. Microchip's UART module has added protocol support features that simplify DALI. Module hardware automatically adds Start and Stop bits to the data stream, and does the necessary Manchester encoding/decoding required by the DALI protocol. For more information, please visit www.microchip.com.

REFERENCES:

- International Standard CEI IEC 60929, Third Edition 2006 – 01
- International Standard IEC 62386-101, Edition 2.0 2014 – 11
- International Standard IEC 62386-102, Edition 2.0 2014 – 11
- International Standard IEC 62386-103, Edition 1.0 2014 – 11

4. DALI Commands

The DALI protocol defines several standard commands which allow system designers to use devices from different manufacturers without having to modify software. The Microchip DALI 2.0 library contains the following commands:

Command	Opcode	Description
OUTPUT LEVEL INSTRUCTIONS		
OFF	0x00	Switches off lamp(s)
UP	0x01	Increases lamp(s) illumination level
DOWN	0x02	Decreases lamp(s) illumination level
STEP UP	0x03	Increases the target illumination level by 1
STEP DOWN	0x04	Decreases the target illumination level by 1
RECALL MAX LEVEL	0x05	Changes the current light output to the maximum level
RECALL MIN LEVEL	0x06	Changes the current light output to the minimum level
STEP DOWN AND OFF	0x07	If the target level is zero, lamp(s) are turned off; if the target level is between the min. and max. levels, decrease the target level by one; if the target level is max., lamp(s) are turned off
ON AND STEP UP	0x08	If the target level is zero, lamp(s) are set to minimum level; if target level is between min. and max. levels, increase the target level by one
ENABLE DAPC SEQUENCE	0x09	Indicates the start of DAPC (level) commands
GO TO LAST ACTIVE LEVEL(1)	0x0A	Sets the target level to the last active output level
GO TO SCENE	0x10	Sets a group of lamps to a predefined scene
CONFIGURATION INSTRUCTIONS		
DALI RESET	0x20	Configures all variables back to their Reset state
STORE ACTUAL LEVEL IN DTR0	0x21	Stores the actual level value into Data Transfer Register 0 (DTR0)
SAVE PERSISTENT VARIABLES(1)	0x22	Stores all variables into Nonvolatile Memory (NVM)
SET OPERATING MODE DTR0(1)	0x23	Sets the operating mode to the value listed in DTR0

RESET MEMORY BANK DTR0[(1)]	0x24	Resets the memory bank identified by DTR0 (memory bank must be implemented and unlocked)
IDENTIFY DEVICE[(1)]	0x25	Instructs a control gear to run an identification procedure
SET MAX LEVEL DTR0	0x2A	Configures the control gear's maximum output level to the value stored in DTR0
SET MIN LEVEL DTR0	0x2B	Configures the control gear's minimum output level to the value stored in DTR0
SET SYSTEM FAILURE LEVEL DTR0	0x2C	Sets the control gear's output level in the event of a system failure to the value stored in DTR0
SET POWER ON LEVEL DTR0	0x2D	Configures the output level upon power-up based on the value of DTR0
SET FADE TIME DTR0	0x2E	Sets the fade time based on the value of DTR0
SET FADE RATE DTR0	0x2F	Sets the fade rate based on the value of DTR0
SET EXTENDED FADE TIME DTR0[(1)]	0x30	Sets the extended fade rate based on the value of DTR0; used when fade time = 0
SET SCENE	0x40	Configures scene 'x' based on the value of DTR0
REMOVE FROM SCENE	0x50	Removes one of the control gears from a scene
ADD TO GROUP	0x60	Adds a control gear to a group
REMOVE FROM GROUP	0x70	Removes a control gear from a group
SET SHORT ADDRESS DTR0	0x80	Sets a control gear's short address to the value of DTR0
ENABLE WRITE MEMORY	0x81	Allows writing into memory banks
QUERY INSTRUCTIONS		
QUERY STATUS	0x90	Determines the control gear's status based on a combination of gear properties
QUERY CONTROL GEAR PRESENT	0x91	Determines if a control gear is present
QUERY LAMP FAILURE	0x92	Determines if a lamp has failed
QUERY LAMP POWER ON	0x93	Determines if a lamp is On
QUERY LIMIT ERROR	0x94	Determines if the requested target level has been modified due to max. or min. level limitations

QUERY RESET STATE	0x95	Determines if all NVM variables are in their Reset state
QUERY MISSING SHORT ADDRESS	0x96	Determines if a control gear's address is equal to 0xFF
QUERY VERSION NUMBER	0x97	Returns the device's version number located in memory bank 0, location 0x16
QUERY CONTENT DTR0	0x98	Returns the value of DTR0
QUERY DEVICE TYPE	0x99	Determines the device type supported by the control gear
QUERY PHYSICAL MINIMUM	0x9A	Returns the minimum light output that the control gear can operate at
QUERY POWER FAILURE	0x9B	Determines if an external power cycle occurred
QUERY CONTENT DTR1	0x9C	Returns the value of DTR1
QUERY CONTENT DTR2	0x9D	Returns the value of DTR2
QUERY OPERATING MODE(1)	0x9E	Determines the control gear's operating mode
QUERY LIGHT SOURCE TYPE(1)	0x9F	Returns the control gear's type of light source
QUERY ACTUAL LEVEL	0xA0	Returns the control gear's actual power output level
QUERY MAX LEVEL	0xA1	Returns the control gear's maximum output setting
QUERY MIN LEVEL	0xA2	Returns the control gear's minimum output setting
QUERY POWER ON LEVEL	0xA3	Returns the value of the intensity level upon power-up
QUERY SYSTEM FAILURE LEVEL	0xA4	Returns the value of the intensity level due to a system failure
QUERY FADE TIME FADE RATE	0xA5	Returns a byte in which the upper nibble is equal to the fade time value and the lower nibble is the fade rate value
QUERY MANUFACTURER SPECIFIC MODE(1)	0xA6	Returns a 'YES' when the operating mode is within the range of 0x80 - 0xFF
QUERY NEXT DEVICE TYPE(1)	0xA7	Determines if the control gear has more than one feature, and if so, return the first/next device type or feature

QUERY EXTENDED FADE TIME(1)	0xA8	Returns a byte in which bits 6-4 is the value of the extended fade time multiplier and the lower nibble is the extended fade time base
QUERY CONTROL GEAR FAILURE(1)	0xAA	Determines if a control gear has failed
QUERY SCENE LEVEL	0xB0	Returns the level value of scene 'x'
QUERY GROUPS 0-7	0xC0	Returns a byte in which each bit represents a member of a group. A '1' represents a member of the group
QUERY GROUPS 8-15	0xC1	Returns a byte in which each bit represents a member of a group. A '1' represents a member of the group
QUERY RANDOM ADDRESS H	0xC2	Returns the upper byte of a randomly generated address
QUERY RANDOM ADDRESS M	0xC3	Returns the high byte of a randomly generated address
QUERY RANDOM ADDRESS L	0xC4	Returns the low byte of a randomly generated address
READ MEMORY LOCATION	0xC5	Returns the content of the memory location stored in DTR0 that is located within the memory bank listed in DTR1
QUERY EXTENDED VERSION NUMBER	0xFF	Returns the version number belonging to the device type or feature
SPECIAL COMMANDS		
TERMINATE	0xA1	Stops the control gear's initilization
DTR0 DATA	0xA3	Loads a data byte into DTR0
INITIALISE	0xA5	Initializes a control gear, command must be issued twice
RANDOMIZE	0xA7	Generates a random address value, command must be issued twice
COMPARE	0xA9	Compares the random address variable to the search address variable
WITHDRAW	0xAB	Changes the initialization state to reflect that a control gear had been identified but remains in the initialization state
PING(1)	0xAD	Used by control devices to indicate theirm presence on the bus
SEARCH ADDRH	0xB1	Determines if an address is present on the bus

SEARCH ADDRM	0xB3	Determines if an address is present on the bus
SEARCH ADDRL	0xB5	Determines if an address is present on the bus
PROGRAM SHORT ADDRESS	0xB7	Programs a control gear's short address
VERIFY SHORT ADDRESS	0xB9	Verifies if a control gear's short address is correct
QUERY SHORT ADDRESS	0xBB	Queries a control gear's short address
ENABLE DEVICE TYPE	0xC1	Enables a control gear's device type function
DTR1 DATA	0xC3	Loads a data byte into DTR1
DTR2 DATA	0xC5	Loads a data byte into DTR2
WRITE MEMORY LOCATION	0xC7	Writes data into a specific memory location and returns the value of the data written
WRITE MEMORY LOCATION NO REPLY(1)	0xC9	Writes data into a specific memory location but does not return a response

Note 1: Addition commands introduced in DALI 2.0.

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