Programmable Gain Amplifier (PGA)

HIGHLIGHTS

This section of the manual contains the following major topics:

> **Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.
>
> Please consult the note at the beginning of the **"Programmable Gain Amplifier (PGA)"** chapter in the current device data sheet to check whether this document supports the device you are using.
>
> Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

1.0 INTRODUCTION

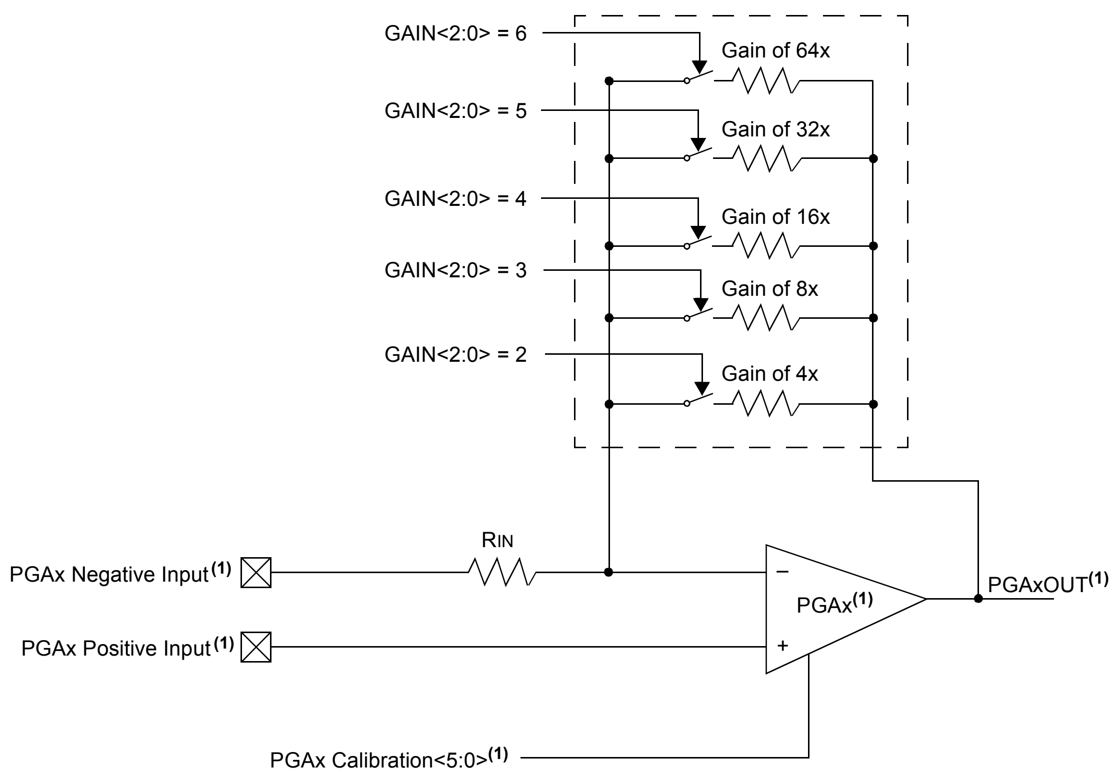
The Programmable Gain Amplifier (PGA) is essentially a non-inverting amplifier with user-programmable gains. The output of the PGA can be connected to a number of dedicated Sample-and-Hold (S&H) inputs of the Analog-to-Digital Converter (ADC) and/or to the high-speed analog comparator module. The PGA has five selectable gains and may be used as a ground referenced amplifier (single-ended) or as an amplifier with an independent ground reference.

The major features of the PGA are as follows:

- Selectable operation: single-ended with internal ground or operation with independent ground reference
- Selectable gains: 4x, 8x, 16x, 32x and 64x
- High gain bandwidth product (40 MHz)
- Rail-to-rail output voltage
- Wide input voltage range (AVSS – 0.3, AVDD + 0.3)

A simplified block diagram of the PGA module is shown in Figure 1-1.

Figure 1-1: PGAx Module Block Diagram



Note 1: x = 1 and 2.

2.0 CONTROL REGISTERS

Note:	Each dsPIC33/PIC24 family device variant may have one or more PGA modules. An ‘x’ used in the names of pins, control/status bits and registers denotes the particular PGA module number. Refer to the **“Programmable Gain Amplifier (PGA)”** chapter of the specific device data sheet for more details.

This section outlines the specific functions of each register that controls the operation of the PGA module. The registers are as follows:

- **PGAxCON: PGAx Control Register**
  - Enables or disables the PGA module
  - Positive input selection
  - Negative input selection
  - Gain selection
- **PGAxCAL: PGAx Calibration Register**
  - Stores the calibration value

Register 2-1: PGAxCON: PGAx Control Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	GAIN2	GAIN1	GAIN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PGAEN:** PGAx Enable bit
1 = PGAx module is enabled
0 = PGAx module is disabled (reduces power consumption)

bit 14 **PGAOEN:** PGAx Output Enable bit
1 = PGAx output is connected to the DACOUTx pin
0 = PGAx output is not connected to the DACOUTx pin

bit 13-11 **SELPI<2:0>:** PGAx Positive Input Selection bits
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = PGAxP4
010 = PGAxP3
001 = PGAxP2
000 = PGAxP1

bit 10-8 **SELNI<2:0>:** PGAx Negative Input Selection bits
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = Ground (Single-Ended mode)
010 = PGAxN3
001 = PGAxN2
000 = Ground (Single-Ended mode)

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **GAIN<2:0>:** PGAx Gain Selection bits
111 = Reserved
110 = Gain of 64x
101 = Gain of 32x
100 = Gain of 16x
011 = Gain of 8x
010 = Gain of 4x
001 = Reserved
000 = Reserved

Register 2-2: PGAxCAL: PGAx Calibration Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PGACAL<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PGACAL<5:0>:** PGAx Offset Calibration bits

The calibration values for the PGA1 and PGA2 bits have to be copied from Flash addresses, 0x800E48 and 0x800E4C, respectively, before the module is enabled. For more information, refer to the Calibration Data Address table in the “**Special Features**” chapter in the specific device data sheet.

3.0 MODULE APPLICATION

3.1 Module Description

The Programmable Gain Amplifiers are used as voltage amplifiers; for example, amplification of voltage across burden resistors or shunt resistors for current sensing. The Programmable Gain Amplifiers' output voltage can be read by any of the dedicated Sample-and-Hold circuits on the ADC module. The PGA's output voltage may also be used as the input to the comparator module for overcurrent/voltage protection.

3.2 Basic Operation

The PGAx module is enabled by setting the PGAEN (PGAxCON<15>) bit to one. When the module is disabled (PGAEN = 0), the output is placed in a high-impedance state.

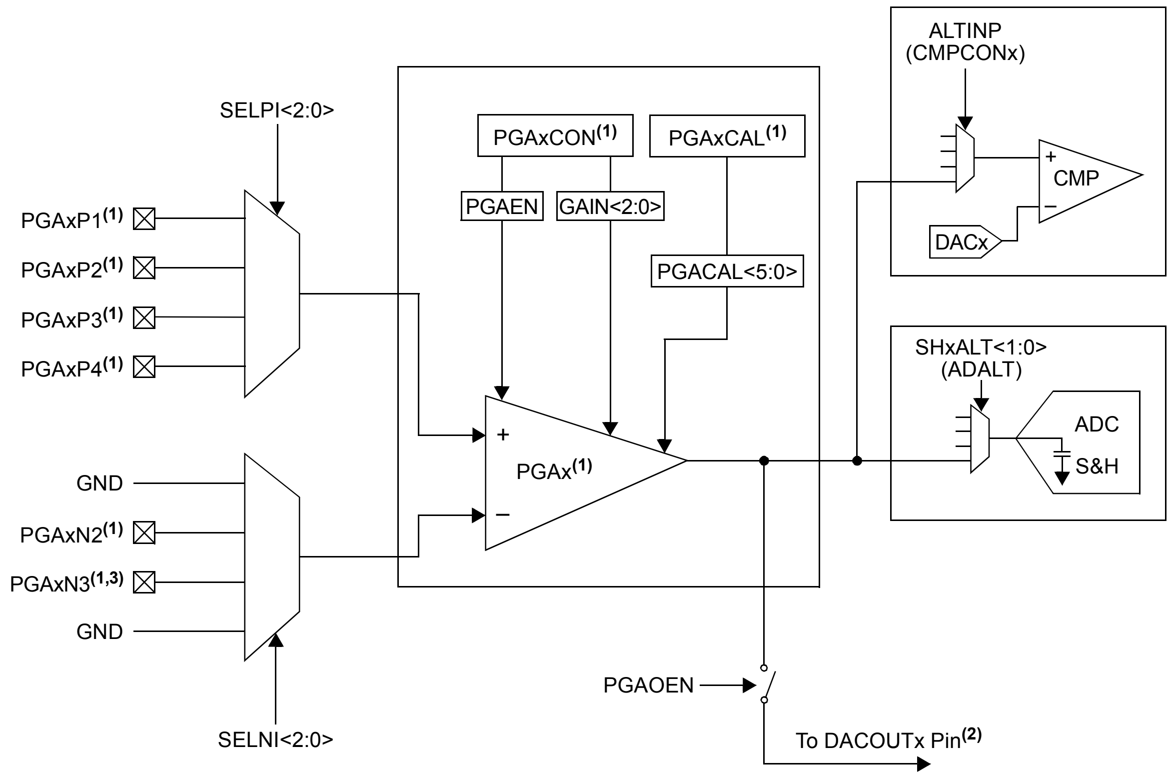
The gain of the PGAx module is selectable through the GAIN<2:0> bits in the PGAxCON register. There are five selectable gains, ranging from 4x to 64x. The SELPI<2:0> and SELNI<2:0> bits in the PGAxCON register select one of four positive or negative inputs to the PGAx module.

For single-ended applications, the SELNI<2:0> bits will select the ground as the negative input source. To provide an independent ground reference, the PGAxN2 and PGAxN3 pins are available as the negative input source to the PGAx module.

The output voltage of the PGAx module can be connected to the DACOUTx pin by setting the PGAOEN bit in the PGAxCON register. When the PGAOEN bit is enabled, the output voltage of PGA1 is connected to DACOUT1 and PGA2 is connected to DACOUT2. For devices with a single DACOUT pin, the output voltage of PGA2 can be connected to DACOUT1 by configuring the DBCC bit (FDEVOPT<6>) in the Configuration register. If both the DAC output voltage and PGA output voltage are connected to the DACOUT pin, the resulting output voltage would be a combination of the two signals. There is no assigned priority between the PGAx module and the DACx module.

To achieve the desired offset voltage specifications, calibration values are fed into the PGAxCAL register. This calibration data is stored in program memory (Flash).

Figure 3-1: PGAx Module Interconnection Block Diagram



Note 1: x = 1 and 2.
2: DACOUTx pin is not available on all devices, refer to the specific device data sheet for more information.
3: PGAxN3 pin is not available on all devices, refer to the specific device data sheet for more information.

Example 3-1 provides a code sequence to set up the PGA1 module with an independent ground reference.

Example 3-1: Configuring PGA with Independent Ground Reference

```
PGA1CONbits.PGAEN = 0;        //Disable PGA1
PGA1CONbits.SELPI = 0;        //PGA1P1 as positive input
PGA1CONbits.SELNI = 1;        //PGA1N2 as negative input
PGA1CONbits.GAIN = 3;         //8x PGA Gain
PGA1CONbits.PGAEN = 1;        //Enable PGA1
```

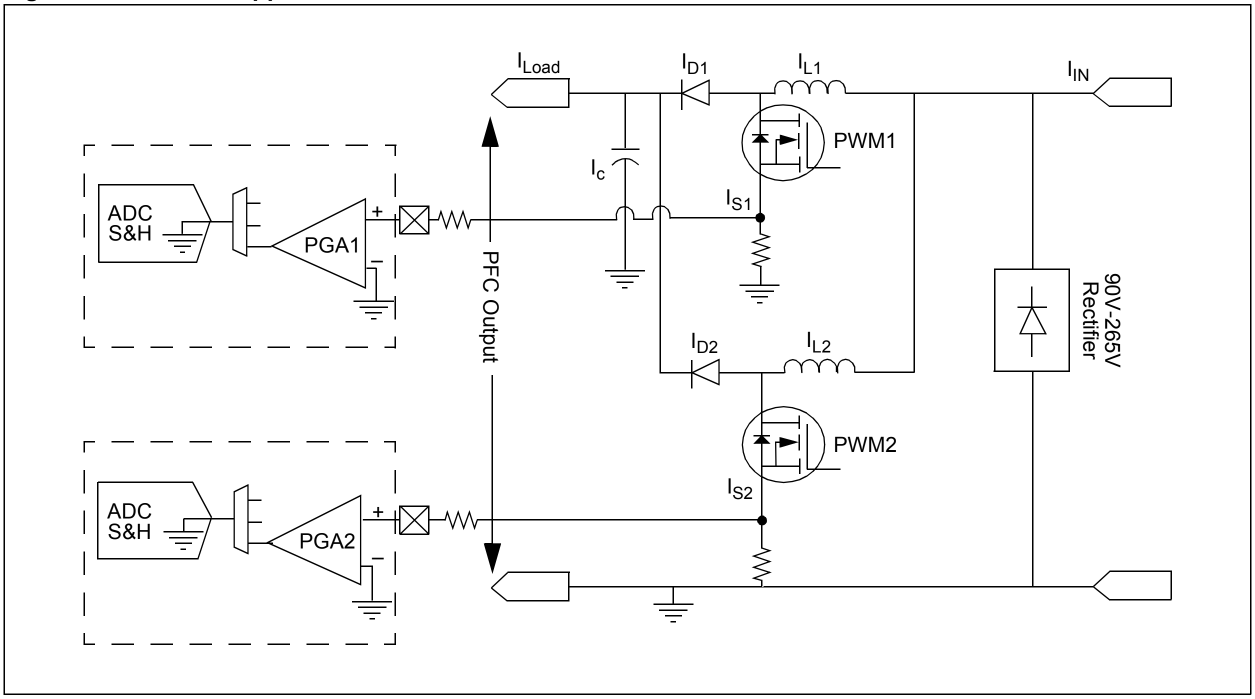
Example 3-2 provides a code sequence to set up the PGA1 module in Single-Ended mode.

Example 3-2: Configuring PGA In Single-Ended Mode

```
PGA1CONbits.PGAEN = 0;        //Disable PGA1
PGA1CONbits.SELPI = 0;        //PGA1P1 as positive input
PGA1CONbits.SELNI = 0;        //Negative input is grounded
PGA1CONbits.GAIN = 2;         //4x PGA Gain
PGA1CONbits.PGAEN = 1;        //Enable PGA1
```


Figure 3-2 illustrates an example of an SMPS application using the PGA module. In this example, the PGA amplifies the current through the shunt resistors, with the output of the PGA connected directly to the ADC module and the PGA configured in Single-Ended mode.

Figure 3-2: PGA Application in Interleaved PFC



4.0 REGISTER MAPS

A summary of the registers associated with the PGA module is provided in Table 4-1.

Table 4-1: Programmable Gain Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PGAxCON	PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	—	—	—	—	—	GAIN2	GAIN1	GAIN0	0000
PGAxCAL	—	—	—	—	—	—	—	—	—	—	PGACAL<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

5.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 device families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the PGA module are:

Title	Application Note #
No related application notes are available at this time.	N/A

> **Note:** Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33/PIC24 families of devices.

6.0 REVISION HISTORY

Revision A (March 2014)

This is the initial released version of this document.

Revision B (March 2015)

Removes all references to differential operation throughout the document. These are replaced with “operation with independent ground reference” or “independent ground reference”, depending on context.

Resizes Figure 1-1 to place it with the introductory discussion on page 2; the diagram is otherwise unchanged.

Other minor corrections throughout the document.

NOTES:

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