# dsPIC33FJ(06/16)GSXXX to dsPIC33EPXXGS50X Migration and Performance Enhancement Guide

## INTRODUCTION

The *"dsPIC33FJ(06/16)GSXXX to dsPIC33EPXXGS50X Migration and Performance Enhancement Guide"* provides an overview of considerations for migrating from the dsPIC33F "GS" devices to the dsPIC33E "GS" devices.

The code developed for the dsPIC33F "GS" devices can be ported to the dsPIC33E "GS" devices after making the appropriate changes, as described in this document. The dsPIC33E devices are based on a new architecture, and feature many improvements and new capabilities over dsPIC33F "GS" devices, such as:

- The maximum operating frequency has increased from 40 MIPS to 60 MIPS @ +125ºC and 50 MIPS to 70 MIPS @ +85ºC
- Dual Partition Flash programming supports live updates
- On certain devices, the Flash has increased from 16 Kbytes on dsPIC33F "GS" devices to 64 Kbytes on dsPIC33E "GS" devices
- On certain devices, the RAM has increased from 2 Kbytes on dsPIC33F "GS" devices to 8 Kbytes on dsPIC33E "GS" devices
- Two sets of alternate Working registers to reduce context switching and improve throughput of control loops
- New Programmable Gain Amplifiers (PGA)
- New 12-bit Analog-to-Digital Converter (ADC)
- New 12-bit Digital-to-Analog Converter (DAC)
- Increased number of virtual pins from four to six
- An enhanced $I^2C$™ module for supporting PMBus™ communication
- Improved FRC accuracy
- New security features for Dual Partition Operating modes
- Increased number of Pulse-Width Modulation (PWM) generators from four to five
- Number of input capture and output compare modules increased from two on dsPIC33F "GS" devices to four on dsPIC33E "GS" devices
- Replaced fuse-based configuration with the Flash-based device configuration
- Number of Serial Peripheral Interfaces (SPIs), Universal Asynchronous Receiver Transmitters (UARTs) and $I^2C$ modules increased from one to two
- Number of timers increased from three to five
- Additional 10 μA current source has been added

**Note:** Device data sheets and errata are available for download from the Microchip Worldwide Web site at: http://www.microchip.com.

**Note:** This migration document details the transition to the dsPIC33EPXXGS50X devices but can also be used for migrating to the dsPIC33EPXXGS202 devices. Just note that some features may not be available. Refer to device-specific data sheet for more details.

## MIGRATION OVERVIEW

This migration and performance enhancement guide discusses several enhancements, changes and application migration considerations related to the dsPIC33E "GS" devices. The following are the key migration considerations:

- Operates up to 70 MIPS. The migration to less than 40 MIPS will affect the peripheral clocks and operational characteristics.
- Minor pinout differences and new packages.
- Minor instruction set enhancements.
- Instruction pipeline differences, resulting in changes to application execution cycle counts.
- New Program Space Visibility (PSV) access method.
- Increased Special Function Register (SFR) space.
- Increased Flash program memory size and changes to Flash access latency.
- Increased Run-Time Self-Programming (RTSP) page and row sizes with changes in methodology, and changes in erase/programming times.
- Changes to the Interrupt Vector Table (IVT) and Alternate Interrupt Vector Table (AIVT).
- Interrupt register changes.
- I/O port analog/digital selection and Change Notification Control register changes.
- Device Configuration register updates.
- New peripherals:
  - PGA
  - 10 μA current source
- Included enhanced peripherals:
  - $I^2C$
  - Analog comparator
  - ADC
  - Input capture/output compare
  - SPI
- More instantiations of individual peripherals.

## Operating Range

The operating frequency of dsPIC33E devices is up to 70 MIPS. The VCAP voltage in dsPIC33E devices is 1.8V, which is provided by an internal voltage regulator.

## Packaging Migration Considerations

The 28-pin and 44-pin variants are peripheral pin compatible with the 28-pin and 44-pin variants of the dsPIC33FJ06/16GSXXX devices. The following additional features added to the dsPIC33FJ06/16GSXXX devices may impact the code migration:

- Additional ADC ANx inputs have been added which may require a clearing of the appropriate ANSELx bit to use the I/O pin as a digital I/O
- The RPn pin numbering is different
- The virtual RPn pins are now numbered as RP176-RP181
- Certain device pins are no longer 5V tolerant due to analog inputs
- Additional $I^2C$ communication is multiplexed on certain device pins

| **Note:** | The 64-pin variants are not peripheral pin compatible with the 64-pin dsPIC33FJ32/64GSXXX devices. |
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## CPU Architecture and Instruction Set

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Instruction Set
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The dsPIC33E architecture supports a faster maximum CPU execution speed of 70 MIPS.

The instruction execution pipeline in dsPIC33E devices differs from the dsPIC33F devices due to a three-cycle Flash program memory access time. While migrating from a dsPIC33F user application to the dsPIC33E user application, the program execution times and cycle counts will change.

For more information, refer to the instruction flow timing diagrams, that illustrate different instruction flow types, in **"Section 8.0 Instruction Flow Types**" in the **"dsPIC33E Enhanced CPU"** (DS70005158) chapter of the "*dsPIC33/PIC24 Family Reference Manual*".

The Program Space Visibility Page Address (PSVPAG) register has been replaced by a pair of registers (Data Space Read Page register, DSRPAG, or Data Space Write Page register, DSWPAG), which enables unified support for the new Extended Data Space (EDS) feature as well as for the existing PSV access functionality.

### INSTRUCTION SET

Any read operations (including bit operations, such as BSET/BCLR/BTG) on peripheral SFRs require two instruction cycles in dsPIC33E devices instead of one instruction cycle.

Program flow change instructions, such as branches and subroutine calls, take four instruction cycles in dsPIC33E devices instead of two instruction cycles.

The RETURN, RETFIE, and RETLW instructions require up to six instruction cycles in dsPIC33E devices instead of three instruction cycles.

Besides signed and unsigned multiplications, DSP multiplier-based instructions in dsPIC33E devices support mixed-sign multiplication operations.

MCU multiplication (MUL) instructions in dsPIC33E devices include an option to write the 32-bit multiplication result into Accumulator A or B instead of writing the result to a pair of W registers.

The instruction encoding of the Compare/Skip instructions, such as, CPSEQ, CPSNE, CPSGT and CPSLT, as well as the RCALL Wn and GOTO Wn instructions, has changed in the dsPIC33E devices.

The size of the literal value specifying the loop count in DO and REPEAT instructions has been increased from 14 bits to 15 bits.

The size of the variable (W register) value specifying the loop count in DO and REPEAT instructions has been increased from 14 bits to 16 bits in dsPIC33E devices.

The size of the literal value specifying the comparison reference value in the CP and CPB instructions has been increased from 5 bits to 8 bits in dsPIC33E devices.

The number of DO loop nesting levels for which the CPU automatically manages register context save/restore has been increased from one to three in dsPIC33E devices.

The 8-level DO loop shadow methodology in the dsPIC33F architecture has been replaced with a 4-level DO loop hardware stack in the dsPIC33E devices. Migrating an application from the dsPIC33F device family requires changes to the user software if more than four DO Loops are being used concurrently with the software.

On dsPIC33E devices, the first instruction in a DO loop cannot be a PSV read or Table Read operation.

To support fast literal value and register writes to the TBLPAG, DSRPAG and DSWPAG registers, the dsPIC33E architecture supports a new base instruction named MOVPAG.

A base instruction, known as MULW, has been added to the dsPIC33E devices. This instruction performs a 16x16 multiplication and it generates a 16-bit result.

The new CALL.L instruction allows indirect subroutine calls with 24-bit offsets.

New Conditional Compare/Branch instructions, such as CPBEQ, CPBNE, CPBGT and BPBLT, have been added for dsPIC33E devices.

The TBLRDL/TBLRDH instructions require five instruction cycles in the dsPIC33E devices.

A Context Swap instruction, CTXTSWP, has been added for manually switching between the alternate Working registers.

A Boot Swap instruction, BOOTSWP, has been added for devices that feature dual Flash partitions. This instruction will swap the active and inactive Flash partitions without the need for a device Reset. This instruction must be followed by a CALL instruction.

| **Note:** | For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157). |
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## REGISTERS

The PSV bit (CORCON<2>) has been replaced by the new Stack Frame Active (SFA) bit in the dsPIC33E devices. The SFA status bit, when set, indicates that a stack frame is active, and W14 and W15 will not use EDS.

The US bit (CORCON<12>) has been expanded with the dsPIC33E devices to the US<1:0> bits (CORCON<13:12>). When US1 is clear, the US0 bit selections are backward-compatible. Setting the US<1:0> bits to a value of '10' enables the new DSP Mixed-Sign Multiplication mode.

A new bit, VAR (CORCON<15>), has been added in the dsPIC33E devices. The VAR bit determines if interrupt processing will use a fixed latency or a variable latency.

The SA bit (SR<13>), SB bit (SR<12>) and SAB bit (SR<10>) need not be cleared manually in software in the dsPIC33E devices. Any subsequent instruction that affects these Status bits, that did not cause a corresponding accumulator saturation condition, will clear the bits. In addition, these bits can now be set in software, enabling efficient context state switching.

The DOSTARTH and DOSTARTL registers are read-only in dsPIC33E devices.

## Flash Program Memory

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Memory Size and Organization
- Registers
- Electrical Characteristics
- Run-Time Self-Programming

### dsPIC33E FEATURE ENHANCEMENTS

The Flash program memory module on the dsPIC33E devices has several enhancements and new features. This section details the high-level improvements:

The dsPIC33E devices differ from the dsPIC33F devices in the program memory organization, the time required to access the program memory and the mechanism for accessing constants located in program memory using PSV.

The PSV mechanism to access constants stored in program memory is different in dsPIC33E devices. The PSV mechanism access utilizes the new DSRPAG register instead of the PSVPAG register for generating the read address. The PSV bit and the PSVPAG register have been removed in the dsPIC33E devices. On dsPIC33E devices, the PSV mechanism can be used to access all three bytes of a program memory word, unlike dsPIC33F devices, where the PSV can only access the lower 16 bits of a program memory word. The PSV accesses require five instruction cycles instead of two instruction cycles.

For devices operating in Dual Partition Flash mode, the code execution from the active Flash partition does not stall when performing RTSP operations on the inactive Flash partition.

For more information on the Flash Program Memory, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, "**Dual Partition Flash Program Memory**" (DS70005156).

### MEMORY SIZE AND ORGANIZATION

The dsPIC33E devices contain up to 64 Kbytes of Flash program memory, whereas the dsPIC33F devices have up to 16 Kbytes of Flash memory.

The IVT and the AIVT in the dsPIC33E devices are twice as large as the IVT and AIVT in the dsPIC33F devices.

### REGISTERS

The dsPIC33E devices have a new NVMSIDL bit (NVMCON<12>), which can be used to discontinue the primary Flash program memory operation when the device is in Idle mode.

The ERASE bit (NVMCON<6> in dsPIC33F) has been deleted in dsPIC33E devices.

### ELECTRICAL CHARACTERISTICS

The Flash program memory erase and programming times in the dsPIC33E devices are different from the dsPIC33F devices. For Program Memory specifications, refer to the "**Electrical Characteristics**" chapter in the specific device data sheet.

### RUN-TIME SELF-PROGRAMMING

The Run-Time Self-Programming (RTSP) changes between the dsPIC33F and the dsPIC33E devices are listed in Table 1.

**TABLE 1: RTSP CHANGES BETWEEN dsPIC33F AND dsPIC33E DEVICES**

| Parameter | dsPIC33FJ06/16GSXXX | dsPIC33EPXXGS50X |
|---|---|---|
| Smallest program memory word program size | One word – 1 instruction or 3 bytes | An even-odd pair of words – 2 instructions or 6 bytes |
| NVMOP<3:0> bit (NVMCON<3:0>) settings | If ERASE = 1:<br>1111 = Memory bulk erase operation<br>1101 = Erase General Segment<br>0011 = No operation<br>0010 = Memory page erase operation<br>0001 = No operation<br>0000 = Erase a single Configuration register byte<br>If ERASE = 0:<br>1111 = No operation<br>1101 = No operation<br>0011 = Memory word program operation<br>0010 = No operation<br>0001 = Memory row program operation<br>0000 = Program a single Configuration register byte | 1111 = Reserved<br>•<br>•<br>•<br>0101 = Reserved<br>0100 = Inactive partition memory erase operation<br>0011 = Memory page erase operation<br>0010 = Memory row program operation<br>0001 = Memory double-word program operation<br>0000 = Reserved |
| Location of program memory latches for RTSP | Same addresses as the program memory locations to be programmed | Dedicated write latches located at addresses, 0xFA0000 and 0xFA0002, in configuration memory space |
| Method of specifying the program memory row/word or Configuration register to be written by RTSP operation | The destination address of the most recent Table Write instruction defines the row or word to be written | The NVMADR/NVMADRU registers specify the location to program in program Flash and the NVMSRCADR register specifies the RAM address of the data to be programmed into Flash for row programming |

## Interrupt Controller

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Memory Size and Organization
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The interrupt controller module on the dsPIC33E devices has several enhancements and new features. This section details the high-level improvements.

Two new traps have been added in the interrupt controller, such as a generic hard trap at address, 0x000008, and a generic soft trap at address, 0x000010. Both the generic hard trap and soft trap can be triggered manually by user software, which provides software traps for debugging or task switching purposes.

A new NVM write complete interrupt vector has been inserted at address, 0x000032, which was a reserved vector in the dsPIC33F devices.

Several new interrupt vectors have been added in the previously reserved locations, as well as at addresses beyond 0x0000FC, reflecting the new peripheral instances and features present in dsPIC33E "GS" devices.

The AIVT is only available when the Boot Segment (BS) has been defined and the AIVT has been enabled. To enable the AIVT, the Configuration bit, AIVTDIS in the FSEC register, must be programmed and the AIVTEN bit must be set (INTCON2<8> = 1). The AIVT begins at the start of the last page of the Boot Segment, defined by the BSLIM<12:0> bits. The second half of the page is no longer usable space. The Boot Segment must be at least two pages to enable the AIVT.

### MEMORY SIZE AND ORGANIZATION

The IVT and AIVT in the dsPIC33E devices is twice as large as the IVT and AIVT in the dsPIC33F devices. The AIVT address location is defined by the BSLIM<12:0> bits and it requires a Boot Segment to be enabled.

As a result of the insertion of new traps, the addresses of the stack error trap and math error trap vectors have changed to 0x00000A and 0x00000C, respectively.

### REGISTERS

The Interrupt Flag Status registers (IFSx), Interrupt Enable Control registers (IECx) and Interrupt Priority Control registers (IPCx) have been changed relative to the dsPIC33F devices. The locations of the interrupt flag status bits, interrupt enable control bits and interrupt priority control bits are moved across the IFSx, IECx and IPCx registers. For more information on the specifics of these bit locations, refer to the "**Interrupt Controller"** chapter in the specific device data sheet.

The ADC module on the dsPIC33E devices converts individual ANx channels as compared to the dsPIC33F pair conversion. As a result, the ADC Pair Interrupt bits, ADCPxIF, ADCPxIE and ADCPxIP, are now relabeled as ADCANxIF, ADCANxIE and ADCANxIP.

A new bit, VAR (CORCON<15>), has been added in dsPIC33E devices. This bit determines if interrupt processing will use a fixed latency (13 instruction cycles) or variable latency (9 to 13 instruction cycles).

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| **Note:** | For more information on interrupt processing, refer to **"Section 3.0 Interrupt Processing Timing"** in the **"Interrupts"** (DS70000600) chapter of the *"dsPIC33/PIC24 Family Reference Manual"*. |

The ALTIVT bit (INTCON2<15>) has been replaced by the new Global Interrupt Enable bit (GIE), which allows the user to enable/disable all interrupts without having to explicitly raise the CPU interrupt priority in real time.

A new Software Trap Enable (SWTRAP) bit (INTCON2<13>) has been added.

The register, INTCON3, which contains the NVM Address Error Soft Trap (NAE), Auxiliary PLL Loss of Lock Soft Trap (APLL) and DO Stack Overflow Soft Trap (DOOVR) status bits, has been added.

The register, INTCON4, which contains the Software Generated Hard Trap (SGHT) status bit, has also been added.

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| **Note:** | When migrating dsPIC33F software to dsPIC33E devices, ensure that your application software is using the correct device-specific linker scripts and compiler/assembler include files. |

## I/O Ports

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Registers
- Electrical Characteristics
- Pinouts

### dsPIC33E FEATURE ENHANCEMENTS

The Input/Output (I/O) module on the dsPIC33E devices has several enhancements and new features. The I/O pins in dsPIC33E devices have a Change Notification (CN) function and internal weak pull-down resistors associated with every available I/O port pin.

### REGISTERS

The CNEN1, CNEN2, CNPU1 and CNPU2 registers have been replaced by the registers, CNENA through CNEND, CNPUA through CNPUD and CNPDA through CNPDD, to correspond with the actual port nomenclature, PORTA through PORTD.

The ADPCFG register, which was used for the ANx pins, does not exist in the dsPIC33E devices. This functionality is now performed by the ANSELA through ANSELD registers, which are part of the corresponding I/O port.

Several new input sources have been added to the selectable input sources for the Peripheral Pin Select (PPS) module. These include additional communication inputs, SPI and UART, and additional input capture inputs. The PWM Faults and synchronization source mapping have changed. The bit fields are extended to 8 bits to include all possible RPn pins.

The output selection sources for remappable pins have changed due to the added communication, like SPI and UART, and additional output compare modules and additional PWM module. The value of the RPORx<5:0> bit field (definition) corresponding to the peripheral has changed for all functions. For more Information, refer to the specific device data sheet.

### ELECTRICAL CHARACTERISTICS

Due to the additional ADC inputs, some of the I/O pins that are 5V tolerant on the dsPIC33F devices are not 5V tolerant on the corresponding dsPIC33E devices:

- 28-Pin SOIC devices: Pin 17 and Pin 18 are not 5V tolerant
- 28-Pin QFN devices: Pin 14 and Pin 15 are not 5V tolerant
- 44-Pin TQFP/QFN devices: Pin 1 through Pin 4 and Pin 44 are not 5V tolerant

In addition, there may be changes in the $V_{IH}$, $V_{IL}$, $V_{OH}$ and $V_{OL}$ specifications, and other electrical characteristics of the I/O pins. Refer to the "**Electrical Characteristics**" chapter of the specific device data sheet for I/O pin input/output specifications. When migrating from a dsPIC33F device to a dsPIC33E device, ensure that all the supporting circuitry is compatible with the source/sink capability of the dsPIC33E device.

### PINOUTS

The numbering of the Peripheral Pin Select (PPS) pins (RPn) has changed on the dsPIC33E devices. The Peripheral Pin Select pins are numbered from RP34 to RP63, with the virtual pins at RP176 through RP181.

When migrating from the 44-pin dsPIC33F devices, the following device pins have added functionality:

- Added Analog (ANx) inputs on Pins 1-4, 19, 20, 34, 43 and 44
- Added dedicated Fault inputs on Pins 14 and 15
- Added alternate $I^2C$™ input on Pins 37 and 38
- Added second $I^2C$ input on Pins 41 and 42

When migrating from the 28-pin dsPIC33F devices, the following device pins have added functionality:

- Added Analog (ANx) inputs on Pin 8 and Pins 13-15
- Added second $I^2C$ input on Pins 11 and 12

## Oscillator Configuration

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Electrical Characteristics

### dsPIC33E FEATURE ENHANCEMENTS

The oscillator configuration module on the dsPIC33E devices has several enhancements and new features.

The internal Fast RC (FRC) oscillator accuracy has improved to ±0.9% from ±2% for industrial temperature devices and improved to ±2% from ±5% for extended temperature devices.

The FRC oscillator tuning deviation has changed to ±1.45% from ±11.625%.

### ELECTRICAL CHARACTERISTICS

The primary PLL FVCO output range has changed from 100 MHz-200 MHz to 120 MHz-340 MHz.

The maximum system clock frequency (FOSC) permitted has changed from 80 MHz to 140 MHz, reflecting the 70 MIPS capability of the dsPIC33E device family.

For more examples on setting up the Oscillator and PLL Control registers for the desired functioning oscillator, refer to the "**Oscillator Configuration**" chapter in the specific device data sheet.

## Reset

This section includes the following topics:

- Registers
- Electrical Characteristics

### REGISTERS

A new VREGSF bit (RCON<13>) has been added in dsPIC33E devices. This bit, when set, enables the user application to power down the Flash program memory when the device is in Sleep mode.

Several SFR Reset values are changed relative to the dsPIC33F devices, mainly as a result of the SFR bit changes. To determine the exact default value of each SFR used by the application, refer to the specific device data sheet. While porting application software from dsPIC33F devices, it is highly recommended to explicitly initialize every relevant SFR instead of assuming the default states.

### ELECTRICAL CHARACTERISTICS

The Brown-out Reset (BOR) voltage limits have changed relative to dsPIC33F devices. For more information, refer to the **"Electrical Characteristics"** chapter in the specific device data sheet.

## Power-Saving Modes

### REGISTERS

In dsPIC33E devices, the DOZE<2:0> bits can only be written to when the DOZEN bit (CLKDIV<11>) is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored. Also, the DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by the user software to set the DOZEN bit is ignored.

Additional PMDx bits have been added, reflecting the enhanced peripheral set in the dsPIC33E devices.

For more information on the SFR, refer to the specific device data sheet.

## Input Capture

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The input capture module on the dsPIC33E devices has several enhancements and new features.

The dsPIC33E devices contain up to four input capture channels, unlike the maximum of two input capture channels provided by the dsPIC33F devices.

Timer1 through Timer5 are used as the time base for any input capture channel. Alternatively, the system clock can be the time base for any input capture channel.

The dsPIC33E devices support Cascaded mode, where an even/odd pair of Input Capture timers can be used in a concatenated 32-bit configuration.

The dsPIC33E devices support Triggered mode, where any Input Capture channel can be held in its Reset state until it receives a trigger signal from any of the following peripheral modules:

- Timer1 through Timer5
- Comparator 1 through Comparator 4
- Input Capture Channels 1 to 4
- Output Compare Channels 1 to 4

The dsPIC33E devices support Synchronized mode, where any Input Capture Channel can be reset when it receives a synchronizing signal from any of the following peripheral modules:

- Timer1 through Timer5
- Comparator 1 through Comparator 4
- Input Capture Channels 1 to 4
- Output Compare Channels 1 to 4

### REGISTERS

Table 2 summarizes the dsPIC33E device-specific differences for the Input Capture registers.

**TABLE 2: SFR DIFFERENCES FOR dsPIC33E INPUT CAPTURE MODULE**

| SFR | Differences from dsPIC33F | Data Sheet Chapter |
|---|---|---|
| ICxCON1 | The ICxCON register in dsPIC33F devices is renamed as ICxCON1 in dsPIC33E devices. The following bits are changed:<br>• The ICTMR bit (ICxCON<7>) is relocated and renamed as the ICTSEL<2:0> bits (ICxCON1<12:10>)<br>• The ICTSEL<2:0> bit selections are changed to include Timer1 through Timer5, and the system clock (TCY), as possible input capture time bases | **"Input Capture"** |
| ICxCON2 | The ICxCON2 register in the dsPIC33E devices contains the IC32, ICTRIG, TRIGSTAT and SYNCSEL<4:0> bits to enable and configure the new Trigger, Synchronization and Cascaded modes.<br>This register must be explicitly initialized, even if these new features are not being used. | |

## Output Compare

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The output compare module on the dsPIC33E devices has several enhancements and new features. This section details the high-level improvements.

The dsPIC33E devices contain up to four output compare channels, whereas the dsPIC33F devices have a maximum of two output compare channels.

Timer1 through Timer5 can be used as the time base for any output compare channel. The system clock can also be the time base for any output compare channel.

The dsPIC33E devices support Cascaded mode, where an even/odd pair of output compare timers can be used in a concatenated 32-bit configuration.

The dsPIC33E devices support Triggered mode, where any output compare channel can be held in its Reset state until it receives a trigger signal from any of the following peripheral modules:

- Timer1 through Timer5
- Comparator 1 through Comparator 4
- Input Capture Channels 1 through 4
- Output Compare Channels 1 through 4

The dsPIC33E devices support Synchronized mode, where any output compare channel can be reset when it receives a synchronizing signal from any of the following peripheral modules:

- Timer1 through Timer5
- Comparator 1 through Comparator 4
- Input Capture Channels 1 through 4
- Output Compare Channels 1 through 4

Optional polarity inversion or tri-stating of each output compare pin is supported in the dsPIC33E devices.

The dsPIC33E devices have the following additional functionalities for the Output Compare Fault pin, OCFA:

- Cycle-by-Cycle and Latched Fault modes
- Configurable output compare pin state on a Fault event
- Optional tri-stating of PWM output on a Fault event

### REGISTERS

Table 3 summarizes the dsPIC33E device-specific changes made to the Output Compare registers.

**TABLE 3: SFR DIFFERENCES FOR dsPIC33E OUTPUT COMPARE MODULE**

| SFR | Differences from dsPIC33F | Data Sheet Chapter |
|---|---|---|
| OCxCON1 | The OCxCON register in dsPIC33F devices has been renamed as OCxCON1 in the dsPIC33E devices and the following bits are changed:<br>• The OCTSEL bit (OCxCON<3>) from the dsPIC33F devices has been relocated and expanded to the OCTSEL<2:0> bits (OCxCON1<12:10>)<br>• The OCTSEL<2:0> bit selections have changed to include Timer1 through Timer5, and the system clock, as possible output compare time bases<br>• The OCFLT bit (OCxCON<4>) from the dsPIC33F devices has been removed<br>• New ENFLTA control bit (OCxCON1<7>) to enable individual Faults<br>• New OCFLTA status bit (OCxCON1<4>) to indicate individual Fault conditions<br>• New Trigger Status Mode Select (TRIGMODE) bit (OCxCON1<3>)<br>• The mode selections for OCM<2:0>(OCxCON<2:0>) = 110 and 111 have changed in the dsPIC33E devices | **"Output Compare"** |
| OCxCON2 | The OCxCON2 register in the dsPIC33E devices contains the FLTMD, FLTOUT, FLTTRIEN, OCINV, OC32, OCTRIG, TRIGSTAT, OCTRIS and SYNCSEL<4:0> bits to enable and configure the new trigger, synchronization and cascaded modes, and the other new features listed previously. This register must be explicitly initialized, even if these new features are not being used. | |
| OCxRS(1) | The OCxRS register is used to specify the period in PWM mode in the dsPIC33E devices, whereas in dsPIC33F devices, this register is used to specify the duty cycle in PWM mode. | |
| OCxR(1) | The OCxR register is used to specify the duty cycle in PWM mode on dsPIC33E devices, whereas in dsPIC33F devices, this register is unused in PWM mode. | |

**Note 1:** The OCxRS and OCxR registers are double-buffered in the dsPIC33E devices.

## High-Speed PWM

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The high-speed PWM module on the dsPIC33E devices has several enhancements and new features. The following lists the high-level improvements:

- Additional PWM generator
- Second master time base
  - Special event compare for secondary master time base
- PWM Chop mode
- Write protection for the IOCONx and FCLCONx registers (PWMLOCK, FDEVOPT0)
- PWM high-resolution enable/disable bits
- PWM state blanking of current-limit or Fault signal

### REGISTERS

Table 4 summarizes the dsPIC33E device-specific changes made to the PWM registers.

**TABLE 4: SFR DIFFERENCES FOR dsPIC33E PWM MODULE**

| SFR | Differences from dsPIC33F | Data Sheet Chapter |
|---|---|---|
| PTCON | PWM Sync source bit field has expanded (SNYNCSRC<2:0>). | **"High-Speed PWM"** |
| STCON | The STCON register in the dsPIC33E devices contains the SESTAT, SEIEN, EIPU, SYNCPOL, SYNCOEN, SYNCEN, SYNCSRC<2:0> and SEVTPS<2:0> bits for the secondary master time base. | |
| STCON2 | The STCON2 register in the dsPIC33E devices contains the PCLKDIV<2:0> bits, which are the clock divider bits for the secondary master time base. | |
| STPER | The STPER register in the dsPIC33E devices contains the STPER<15:0> bits for the secondary master time base period value. | |
| SSEVTCMP | The SSEVTCMP register in the dsPIC33E devices contains the SSEVTCMP<12:0> bits for the secondary special event compare value. | |
| CHOP | The CHOP register in the dsPIC33E devices contains the CHPCLKEN and CHOPCLK<6:0> bits for the PWM CHOP feature. | |
| PWMKEY | The PWMKEY register in the dsPIC33E devices, which is used to lock and unlock writes to the IOCONx and FCLCONx registers. | |
| PWMCONx | The MTBS (PWMCONx3) bit has been added for selecting the master time base. | |
| IOCONx | The Reset state of the PENH and PENL bits has changed to a '1' to give the PWM module ownership of the I/O pins at Reset. | |
| FCLCONx | The bits, CLSRC<4:0> and FLTSRC<4:0>, which handle signal source select changes in the dsPIC33E devices. The 0b00000 corresponds to a reserved location and the analog comparator inputs are added. | |
| LEBCONx | State blanking bits, BCH, BCL, BPHH, BPHL, BPLH and BPLL, have been added to the LEBCONx register. | |
| LEBDLYx | The LEBDLYx register in the dsPIC33E devices contains the Leading-Edge Blanking (LEB<8:0>) bits. The bit field has been expanded by two bits. | |
| AUXCONx | The AUXCONx register in the dsPIC33E devices contains the HRPDIS, HRDDIS, BLANKSEL<3:0>, CHOPSEL<3:0>, CHOPHEN and CHOPLEN bits. These bits enable/disable high resolution for the PWM module, as well as selecting the state blanking and CHOP clock source, and enable/disable PWM chopping. | |

## High-Speed Analog Comparator

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The high-speed analog comparator module on the dsPIC33E devices has several enhancements and new features. The following lists the high-level improvements:

- Rail-to-rail inputs
- DAC increased to 12 bits
- Additional DACOUT pin on 64-pin devices
- Additional external reference input
- Hysteresis control

### REGISTERS

Table 5 summarizes the dsPIC33E device-specific changes made to the Analog Comparator registers.

**TABLE 5: SFR DIFFERENCES FOR dsPIC33E ANALOG COMPARATOR MODULE**

| SFR | Differences from dsPIC33F | Data Sheet Chapter |
|---|---|---|
| CMPxCON | The following bits have been added in the dsPIC33E devices: HYSSEL<1:0>, FLTREN, FCLKSEL, HYSPOL and ALTINP. These bits add control for hysteresis, selection of PGA inputs to the comparator and pulse stretcher logic. | **"High-Speed Analog Comparator"** |
| CMPxDAC | The bit field has increased to 12 bits. | |

## High-Speed Analog-to-Digital Converter (ADC)

The high-speed Analog-to-Digital Converter (ADC) module on the dsPIC33E devices has some similarities to the dsPIC33F devices, as far as having dedicated and shared Sample-and-Hold circuits, and dedicated result buffers for every analog input. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual",* "**12-Bit High-Speed, Multiple SARs A/D Converter (ADC)**" (DS70005213).

The following lists the enhancements and the new features of the dsPIC33E devices:

- Five Successive Approximation Register (SAR) ADCs with 12 bits of resolution
- Reduced latency (higher throughput)
- Single-Ended or Differential mode
- More analog inputs
- Two oversampling filters with dedicated interrupts
- Two digital comparators with dedicated interrupts
- External ADC trigger event
- Additional trigger source selections
- ADC results are no longer converted in pairs and each analog input has its own dedicated ISR

| **Note:** | The dedicated S&H circuits are now associated with AN0-AN3. |
|---|---|

## Inter-Integrated Circuit™ ($I^2C$™)

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The Inter-Integrated Circuit™ ($I^2C$™) module on the dsPIC33E devices has several enhancements and new features. The following lists the high-level improvements:

- The number of $I^2C$ modules in the dsPIC33E devices is increased from one to two
- Alternate inputs are added and are selected by the ALTI2C1 and ALTI2C2 bits in the FDEVOPT Configuration register
- Interrupt on Start/Stop conditions
- Selectable data hold time
- State of port pins are readable while peripheral is enabled
- Not all $I^2C$ pins are 5V tolerant

### REGISTERS

Table 6 summarizes the dsPIC33E device-specific differences for the $I^2C$ registers.

**TABLE 6: SFR DIFFERENCES FOR dsPIC33E $I^2C$™ MODULE**

| SFR | Differences from dsPIC33F | Data Sheet Chapter |
|---|---|---|
| I2CxCON1 | The I2CxCON register is renamed as I2CxCON1 in the dsPIC33E devices and the IPMIEN bit is renamed as STRICT. | **"Inter-Integrated Circuit ($I^2C$)"** |
| I2CxCON2 | The I2CxCON register in the dsPIC33E devices contains the bits: PCIE, SCIE, BOEN, SDAHT, SBCDE, AHEN and DHEN. These bits enable/disable interrupts on Stop/Start conditions, select the data hold time and address/data hold enable bits. | |
| I2CxSTAT | New Acknowledge Time (ACKTIM) status bit has been added to the I2CxSTAT register. | |

## Serial Peripheral Interface

This section includes the following topics:

- dsPIC33E Feature Enhancements
- Registers

### dsPIC33E FEATURE ENHANCEMENTS

The Serial Peripheral Interface (SPI) module on the dsPIC33E devices has several enhancements and new features.

The number of SPI modules in the dsPIC33E devices has increased from one to two. Each SPI module in the dsPIC33E devices supports Enhanced Buffer mode, which uses an 8-word deep, hardware transmit/receive FIFO buffer.

### REGISTERS

Table 7 summarizes the dsPIC33E device-specific differences for the SPI registers

**TABLE 7: SFR DIFFERENCES FOR dsPIC33E SPI MODULE**

| SFR | Differences from dsPIC33F | Data Sheet Chapter |
|---|---|---|
| SPIxCON1 | Do not set PPRE<1:0> and SPRE<2:0> to '11' and '111', respectively. | **"Serial Peripheral Interface (SPI)"** |
| SPIxCON2 | New SPIBEN bit (SPIxCON2<0>) is used to enable/disable the Enhanced Buffer mode. | |
| SPIxSTAT | SPIxSTAT SFR changes:<br>• In Enhanced Buffer mode, the SPITBF or SPIRBF bits (SPIxCON2<1:0>) get set only when the entire transmit/ receive FIFO buffer is full<br>• New SPIBEC<2:0> (SPIxSTAT<10:8>), SRMPT (SPIxSTAT<7>) and SRXMPT (SPIxSTAT<5>) status bits have been added specific to the Enhanced Buffer mode<br>• New SISEL<2:0> control bits (SPIxSTAT<4:2>) to specify the Buffer Interrupt mode in Enhanced Buffer mode | |

## CodeGuard™ Security

The code protection features are controlled by the Configuration registers, FSEC and FBSLIM. The FSEC register controls the code-protect level and write protection for each segment. The size of the BS and GS will depend on the BSLIM<12:0> bits setting, and if the AIVT is enabled. The BSLIM<12:0> bits define the number of pages for the BS with each page containing 512 IW. The smallest BS size is one page, which consists of the Interrupt Vector Table (IVT) and 256 IW of code protection.

Additional security has been added to the configuration data, called Configuration Segment (CS). This segment can be write-protected and has three different security levels.

For more information, refer to the "**CodeGuard™ Intermediate Security"** (DS70005182) chapter of the *"dsPIC33/PIC24 Family Reference Manual"*.

## PERFORMANCE ENHANCEMENT TECHNIQUES

In any microcontrollers, there are various techniques that can be utilized by code developers to improve the performance of an application. This section will explore how to take advantage of the dsPIC33E devices' architectural features to enhance the performance of a user application and increase the effective bandwidth of the CPU.

This section includes the following topics:

- Code Constant Storage
- XC16 C Compiler Optimization Options
- Coding Guidelines

### Code Constant Storage

The data constants must always be placed in RAM instead of Flash memory.

#### FLASH VERSUS RAM VARIABLE STORAGE

The PSV and the Flash data constant access can take up to five instruction cycles, compared to one for data RAM accesses. If certain Flash constants are frequently accessed, or the application has large-to-medium segments of constant tables that are being accessed, if feasible, consider placing them in RAM instead of Flash.

**Note:** DSP constants, such as FFT coefficients that may be placed in Flash by the user, are automatically handled by the DSP library functions. The DSP library functions, when appropriate, copy Flash data into the RAM stack space during execution, resulting in higher performance. User intervention is normally not required, although the process can be tuned by the user for maximum performance. Refer to the "**Stack Guard Function**" in the DSP Library Help for more information.

#### RAM SIZE LIMITATIONS

If there is insufficient RAM to hold large Flash constant value tables, consider using the `REPEAT` instruction with the indirect auto-increment `MOV` instruction to copy smaller segments of Flash data into a user-defined scratch pad RAM area for application access (see Example 1). The `REPEAT` copy instructions will execute two and a half times faster than normal Flash read accesses. Copying Flash data into a RAM, utilizing this technique for segments larger than approximately 20 words, will yield positive performance boosts. The larger the data segment being copied into RAM, the larger the performance gains.

**EXAMPLE 1:**

```
__psv__ __attribute__((space(auto_psv))) unsigned int my_constants[10];  //Flash data constants

unsigned int my_scratchpad[10];                         //Scratch pad ram area
unsigned int *p = my_scratchpad;                        //Scratch pad pointer

int main(void)
{
  DSRPAG = (int) __builtin_psvpage(&my_constants);      //dsPIC33E family - select psv page
  //PSVPAG = (int) __builtin_psvpage(&my_constants);    //dsPIC33F family - select psv page

  //---------------------------------------------------------------------------//
  //    Copy flash table data from "my_constants" to user scratch pad          //
  //    data ram array "my_scratchpad".                                        //
  //  NOTE:    Memcopy function encodes a REPEAT instruction with indirect     //
  //           memory move instruction with auto post increment for both       //
  //           source and destination address.                                 //
  //---------------------------------------------------------------------------//

  memcpy(p,(int unsigned *) __builtin_psvoffset(&my_constants),sizeof(my_scratchpad)/sizeof(char));
}
```

### MAPPING FLASH INTO PSV

If placing whole constants tables, or copying partial Flash data constants tables as needed into RAM, is not feasible, the PSV page method can be used to map Flash into the PSV virtual data memory space. This is done to utilize the indirect data memory access suite of instructions. Avoid using the non-PSV Table Read instructions for accessing Flash data as they are considerably slower.

## XC16 C Compiler Optimization Options

Use the MPLAB® XC16 C Compiler optimization features.

### XC16 C COMPILER OPTIMIZATION

For user-enabled, full-featured XC16 C compilers, use the Level 02 or 03 optimization settings in the MPLAB XC16. This will have a significant effect on the general performance of C code execution. Compiler optimization settings have no effect on either precompiled library files or assembly language files.

### OPTIMIZATION LEVEL 02

The XC16 C Compiler optimization Level 02, by default, turns on all optional optimizations with the exception of:

- Loop unrolling (`-funroll-loops`)
- Function in-lining (`-finline-functions`)
- Strict aliasing optimizations (`-fstrict-aliasing`)

It also turns on:

- Force copy of memory operands (`-fforce-mem`)
- Frame Pointer elimination (`-fomit-frame-pointer`)

### OPTIMIZATION LEVEL 03

The XC16 C compiler optimization Level 03 turns on all optimizations specified by the Level 02 default setting and also the `in-line-functions` option. This boosts application performance even more, but at the cost of increasing the code size footprint.

| | |
|---|---|
| **Note:** | For optimized enabled versions of the XC16 C compiler, users can mix or incrementally add optimization options to any of the various compiler base default optimization levels by using C command line options. For more information, refer to the **"Options for Controlling Optimizations"** chapter in the *"MPLAB® XC16 C Compiler User's Guide"* (DS50002071). |

### COMPILER DATA MODEL OPTION

Use the large data model with the small scalar model compiler option. Using this combination forces arrays and structures into far memory, which is acceptable since Indirect Addressing is required. However, enabling the small scalar model compiler option forces everything else into near memory. As previously mentioned, using the large data model option forces all variable accesses to use Indirect Addressing by implementing the Working Register Pointers. This may double and sometimes triple both the code size and the speed of the executable in comparison to the dsPIC33F family for reading or writing to a specific data RAM variable. For more information, refer to the "*MPLAB® XC16 C Compiler User's Guide*" (DS50002071).

## Coding Guidelines

Maximize continuous, non-branching sequential code sequencing and use zero overhead hardware loops when feasible in place of software loops.

### BUILT-IN C MACROS

Use the built-in C macros when possible and consider a bit complement C construct.

For example, instead of:

```
LATBbits.LATB5 = !LATBbits.LATB5;
```

Use the built-in:

```
__builtin_btg(&LATB,5);
```

The bit complement built-in offers a significant code size and speed performance improvement. This means fewer instructions and no conditional branching that would flush and force a reload of the instruction fetch pipeline unit.

### NEAR VERSUS FAR RAM MEMORY

The first 8K of data RAM space is considered “near” memory. Space above that is considered “far” memory. By default, the compiler sets all user data RAM variables and declarations to near memory as it sequentially encounters variables in the code in the order that the C file(s) are compiled. However, when near memory space is full, the compiler will generate compiler errors, indicating that it cannot allocate variable(s). This requires the user to either manually allocate the remaining variables using the far attribute or select the large data model compile option. The special significance of near versus far to the compiler is that near data memory accesses are encoded in only one instruction, using Direct Addressing, while accesses to data variables in far space require two to three instructions using Indirect Addressing.

For this reason, the user must ensure that frequent or commonly used data variables are placed in near memory, while seldom or less frequently used variables are forced into far memory, if near memory is full, using the C compiler far attribute.

### SEQUENTIAL CODE GROUPING

Group as much sequential executable code in the largest contiguous sections possible that are undisturbed by any program flow instructions, such as branches, `CALL`s, `GOTO`s, etc. Defer or group C flow control statements, such as `if`, `else`, `for` and `while`, as much as possible in relation to straight-line code. This will insure the instruction pipeline is efficient and is disturbed as little as possible so it is not flushed and stalled while reloading. Program flow instructions always flush the instruction pipeline and add additional instruction cycles.

### OPTIMIZING CPU INTERRUPTS

Minimize the frequency of peripheral CPU interrupts for those peripherals with data buffers. Peripherals with four to eight-byte/word receive or transmit FIFO buffers allow the user to select interrupts based on the amount of data in the FIFO. Whenever possible, set the interrupt based on when the FIFO is fuller rather than on the first byte/word. This will minimize the number of interrupts, and the overhead associated with interrupt latency and suspension of the interrupted code. Interrupt latency for the dsPIC33E family of devices is nine to 13 instruction cycles and five instruction cycles for the dsPIC33F family of devices. Due to their higher MIPS rating, the instruction cycle time for dsPIC33E devices is much less than that of dsPIC33F devices.

| **Note:** | The dsPIC33E family of devices can have either 13 fixed or nine to 13 variable latency (user-selectable) instruction cycles. |
|---|---|

### ISR C FUNCTION CALL LIMITATIONS

Do not call C functions from within an Interrupt Service Routine (ISR). Since the compiler can make no assumptions about registers that may be affected by a subroutine, called from within a hardware triggered event, it causes the compiler to save all the Working registers (plus a few others) on the stack. This adds considerably more overhead and latency to the ISRs. If absolutely necessary, consider copying the subroutine code directly into the ISR.

# APPENDIX A: REVISION HISTORY

## Revision A (February 2015)

This is the initial released version of this document.

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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