



Power and Reset Requirements for the KSZ84xx EtherSynch® Family

Revision 1.0

Introduction

This application note describes the power supply and power-up sequencing requirements of the KSZ84xx family of devices. It also explains the requirements for reset. It applies to the following devices:

- KSZ8441HLI
- KSZ8462HLI
- KSZ8463MLI
- KSZ8463RLI
- KSZ8852HLI

Power Supply Requirements

These devices are designed so that they can be powered from a single 3.3V supply, yet there are actually three voltage domains inside the chip. The transceiver block always requires 3.3V, as supplied via the VDD_A3.3 pin. The digital I/O block is powered via the VDD_IO pins, which may be 3.3V, 2.5V or 1.8V. Lastly, an internal linear voltage regulator, which takes current from VDD_IO, supplies approximately 1.32V to the low-voltage core. These three voltage domains provide some flexibility in how the devices are powered.

Figure 1 shows the three domains and demonstrates the 3.3V-only configuration, with a single 3.3V supply used for both VDD_A3.3 and VDD_IO. An external connection is required between the low-voltage regulator output pins (VDD_L) and the analog low-voltage input pins (VDD_COL and VDD_AL), and this connection should be filtered with capacitors and a ferrite bead as shown in Figure 2. A suggested ferrite is the Laird HI1206N101R-10, though any ferrite that is roughly similar should be adequate.

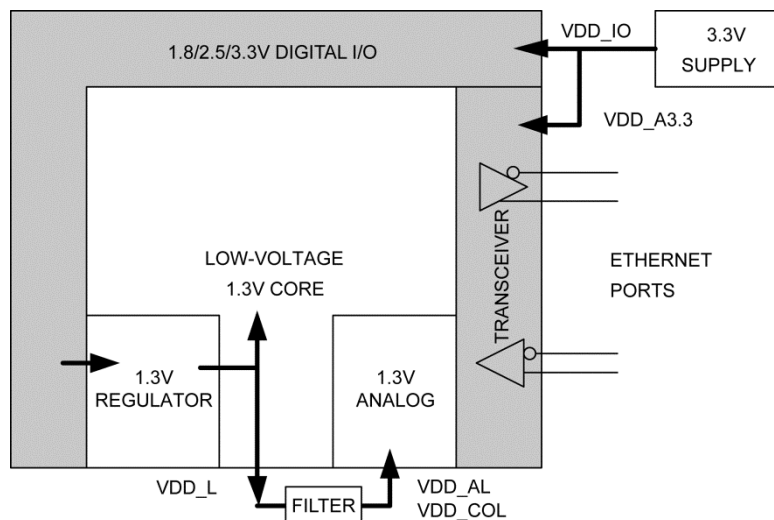


Figure 1. Power Domains and Powering with a Single 3.3V Supply

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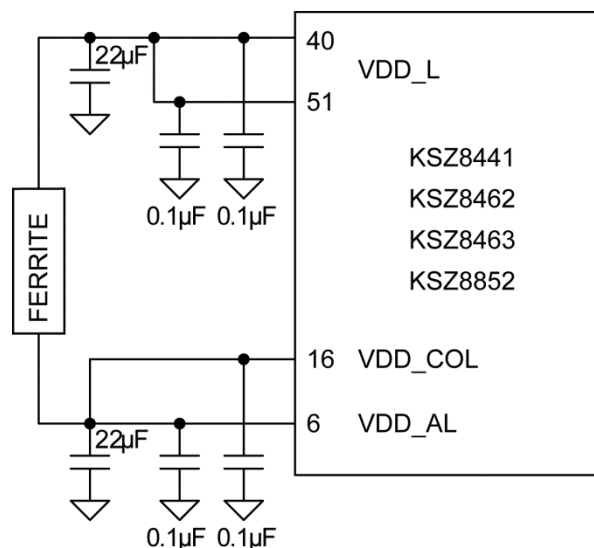


Figure 2. Filtering for 1.3V Pins

With good power supply design, either a switching or a linear supply may be used. Ripple on all supply pin should be limited to 50mV.

For flexibility in interfacing to other devices, it may be desirable to operate the digital I/Os at a voltage other than 3.3V. As shown in [Figure 3](#), the alternate VDD_IO choices are 2.5V or 1.8V. Note that the internal low-voltage regulator requires a minimum supply voltage (on the VDD_IO pins), as determined by the dropout voltage of the regulator. This may limit the ability to utilize 1.8V I/O and the internal regulator at the same time (see the product datasheet for full details). Any such limitation would not apply if an external 1.3V supply is used, as described below.

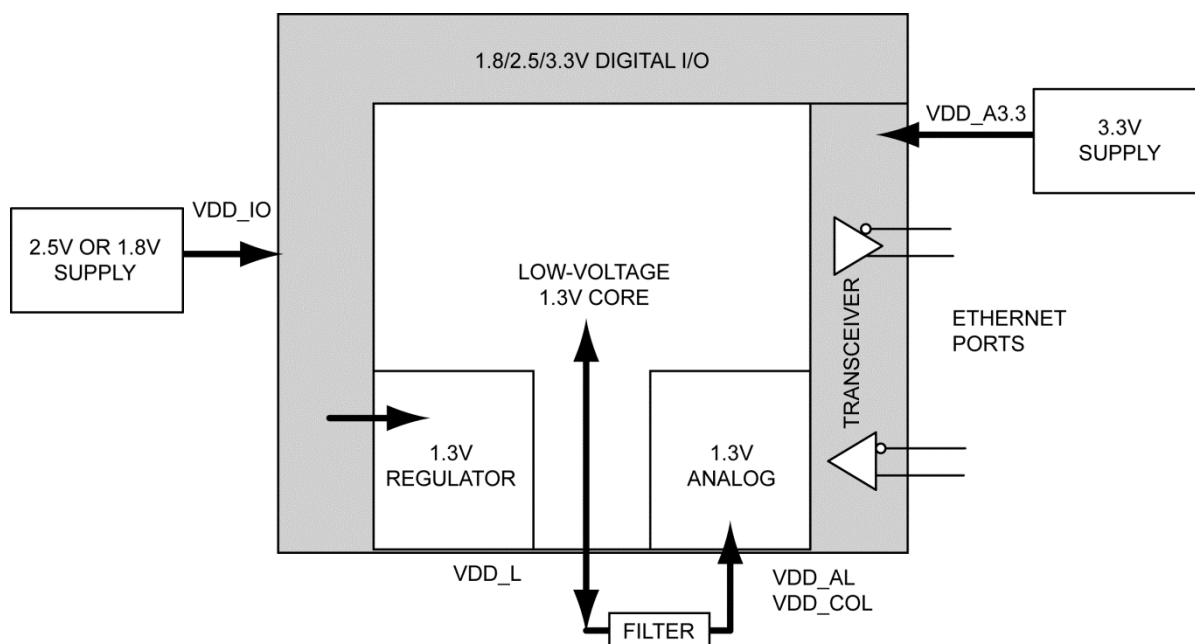


Figure 3. Low-Voltage Digital I/O Configuration

Reducing the VDD_IO voltage also has the advantage of reducing internal power dissipation. The VDD_IO current reduction at reduced VDD_IO is minimal (approximately 2mA for 2.5V and 4mA for 1.8V, relative to 3.3V) because the internal linear regulator draws a relatively constant current. Power dissipation from VDD_IO is therefore essentially linear with the VDD_IO voltage. Power reduction is further discussed in the sections that follow.

Optional External Power for the 1.3V Core

An option is provided to turn off the internal 1.3V regulator – via software – which allows all 1.3V circuits to be powered from an external 1.3V supply. This option is useful for reducing on-chip power consumption, or to enhance RF noise immunity in very noisy environments. Since the internal 1.3V regulator takes its power from the VDD_IO supply, the VDD_IO current drops significantly when the internal regulator is turned off, reducing total power dissipation by approximately 150 to 190mW (at VDD_IO = 3.3V).

As shown in Figure 4, the external low-voltage supply connects to the VDD_L pins and (through a filter) to the VDD_AL and VDD_COL pins. The filtering requirement is unchanged from the internal regulator configuration, and is shown in Figure 2.

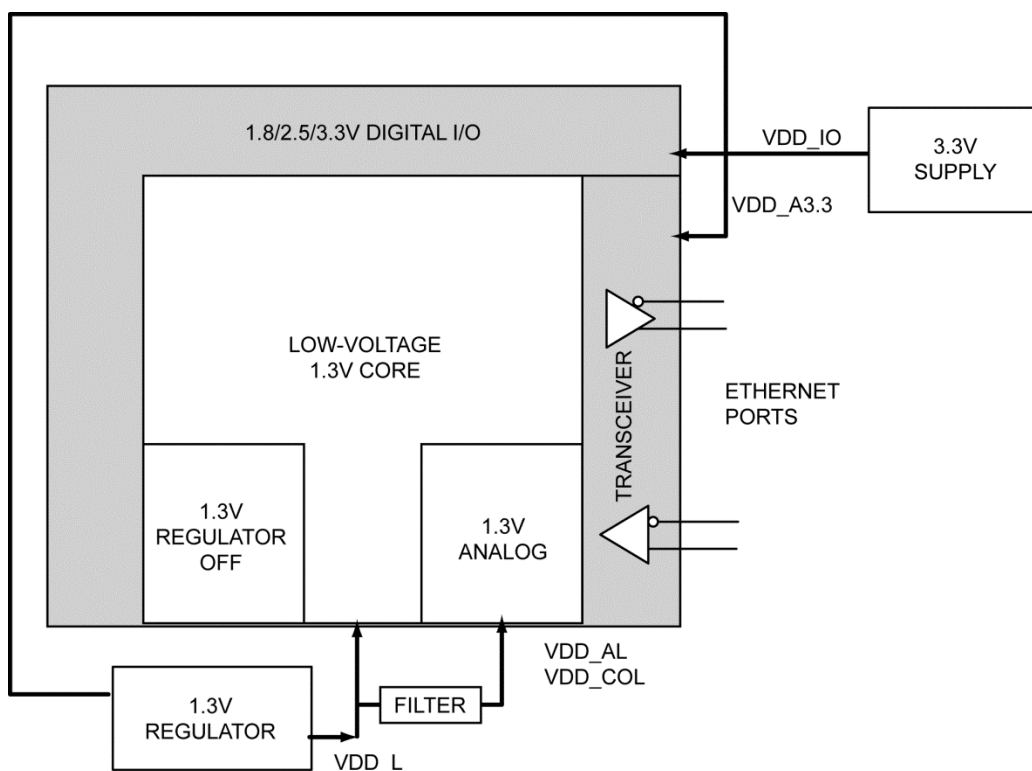


Figure 4. Powering the Low-Voltage Core with an External Regulator

As with the other supply pins, it is suggested that ripple noise be limited to 50mV on the 1.3V supply pins. A linear voltage regulator may be used to supply 1.3V since this will provide the quietest power to the 1.3V analog circuits and easily satisfies the power sequencing requirements. A switching regulator may also be used as long as the ripple noise requirement is met. The regulator should be rated for 150mA or more, and it needs to be adjustable in order to closely match the voltage of the internal regulator. The Micrel MIC5308Y is an example of an adjustable LDO that is well suited to this application. See the VDD_L, VDD_AL and VDD_COL voltage range specification in the device datasheet.

The internal 1.3V regulator turns on automatically once the VDD_A3.3 and VDD_IO supply voltages are up. When using an external 1.3V supply, software should turn off the internal regulator by setting bit [7] in the ANA_CNTRL_1 register (address 0x748).

From start-up until the time that the internal regulator is disabled, the 1.3V supply pins will not act like a typical passive load from the point of view of the external supply. Because the chip can source current from these pins, it is suggested to avoid using an external 1.3V supply with current sinking capability. This is a concern under two scenarios: 1) the external supply voltage is less than the internal regulator voltage, and 2) if the external regulator is off for any appreciable amount of time, will it act as a current sink (e.g. low impedance to ground)? Some current sinking by the external supply is acceptable, but it must be limited to 50mA. (When shorted to ground, the 1.3V supply pins of the chip will source approximately 150mA. Such a current is unacceptable.)

If the situation is reversed and the external supply voltage is greater than 1.3V, there is no concern because the internal regulator has no current sinking capability.

Power Options Summary

Table 1 summarizes the power configuration options described in the sections above. They range from one to three supplies.

Table 1. Power Configuration Options

Power Configuration Options		Low-Voltage (1.3V) Supply	1.8V or 2.5V Supply	3.3V Supply
1	VDD_IO = 3.3V; Internal Low-Voltage Regulator On	None. Derived Internally from VDD_IO; Output On VDD_L	None	VDD_A3.3, VDD_IO
2	VDD_IO = 2.5V or 1.8V; Internal Low-Voltage Regulator On	None. Derived Internally from VDD_IO; Output On VDD_L	VDD_IO	VDD_A3.3
3	VDD_IO = 3.3V; Internal Low-Voltage Regulator Off	VDD_L, VDD_AL, VDD_COL	None	VDD_A3.3, VDD_IO
4	VDD_IO = 2.5V or 1.8V; Internal Low-Voltage Regulator Off	VDD_L, VDD_AL, VDD_COL	VDD_IO	VDD_A3.3

Power Consumption

Table 2 summarizes the power consumption for each device, with and without an external low voltage supply. The VDD_IO voltage is 3.3V. When using the internal regulator, subtract 4mA for VDD_IO at 1.8V, or 2mA for VDD_IO at 2.5V.

Table 2. Typical Power Consumption (Ports 1 and 2 at Full Speed, Nominal Voltages, 25°C)

Part Number	Internal Regulator/ External Supply	VDD_IO (3.3V)	VDD_A3.3	VDD_L	VDD_AL VDD_COL	Total Power
KSZ8441HLI	Internal 1.3V Regulator	78mA	23mA	N/A	N/A	335mW
	External 1.32V Supply	2mA	23mA	68mA	10mA	185mW
KSZ8462HLI	Internal 1.3V Regulator	82mA	40mA	N/A	N/A	400mW
	External 1.32V Supply	2mA	40mA	70mA	12mA	245mW
KSZ8463MLI	Internal 1.3V Regulator	100mA	40mA	N/A	N/A	460mW
	External 1.32V Supply	10mA	40mA	77mA	11mA	280mW
KSZ8463RLI	Internal 1.3V Regulator	102mA	40mA	N/A	N/A	470mW
	External 1.32V Supply	10mA	40mA	77mA	12mA	280mW
KSZ8852HLI	Internal 1.3V Regulator	82mA	40mA	N/A	N/A	400mW
	External 1.32V Supply	2mA	40mA	70mA	12mA	245mW

Power Sequencing and Ramp Rate Requirements

At power-on, the supplies do not need to turn on in any particular sequence. For simplicity, it is suggested to turn them all on at the same time. The same is true for power-down. To ensure correct device operation, the Reset input must see a rising edge after all of the power supplies are up and stable – as described in the next section.

The following points address all issues relating to excessive currents which may arise if the supplies are not turned on and off in unison.

- AVDD_A3.3 is electrically isolated from the other voltages, so there are no power sequencing requirements between VDD_A3.3 and all other supplies. VDD_A3.3 may turn on or off at any time, with no timing restrictions.
- Thus if VDD_A3.3 and VDD_IO are the only supplies used, there are no power sequencing restrictions.

When using an external 1.3V supply, the interaction between it and VDD_IO must be considered, as follows.

- The 1.3V supply may turn-on any time before VDD_IO, with the restriction that the VDD_IO supply does not sink more than 50mA of current when it is off. If the VDD_IO supply sinks more current when off, then the 1.3V supply must not turn-on before VDD_IO.
- The VDD_IO supply may turn on any time before the 1.3V supply, with the restriction that the 1.3V supply does not sink more than 50mA of current when it is off. If the 1.3V supply sinks more current when off, then the VDD_IO supply should not turn-on before 1.3V.
- If both the 1.3V and VDD_IO supplies sink more than 50mA when off, or if the current sinking characteristics of the two supplies are unknown, then VDD_IO should turn on first, with the 1.3V turning on within 10ms afterwards. For power-down, the timing is reversed: 1.3V should turn off first, with VDD_IO turning off within 10ms afterwards.

There are no minimum or maximum ramp rate requirements for any of the power supplies, but the turn-on must always be non-monotonic.

Reset

The RSTN (active-low reset) input pin is used to reset the entire device to a known state. To reset properly, a rising edge of RSTN must occur after all of the power supplies have reached their minimum required levels, plus an additional minimum time t_{SR} , (10ms). The timing is shown in Figure 5, as well as in the datasheet. There is no restriction on the ramp rate of RSTN or on the behavior of RSTN during the actual ramping of the power supplies.

Since RSTN does not need to see a sharp rising edge, the easiest way to implement the reset function is with an RC circuit, as implemented on the KSZxx evaluation boards. Figure 6 shows such a circuit, plus an optional connection to a CPU-driven reset circuit. A 10kΩ resistor and 10μF capacitor are suggested values, which will work with even slow ramping power supplies. Numerous specialized reset devices are available for combining power-on reset, manual reset and processor controlled reset functionalities. They also provide a cleanly switched rising edge for reset, which may be helpful for overall system timing.

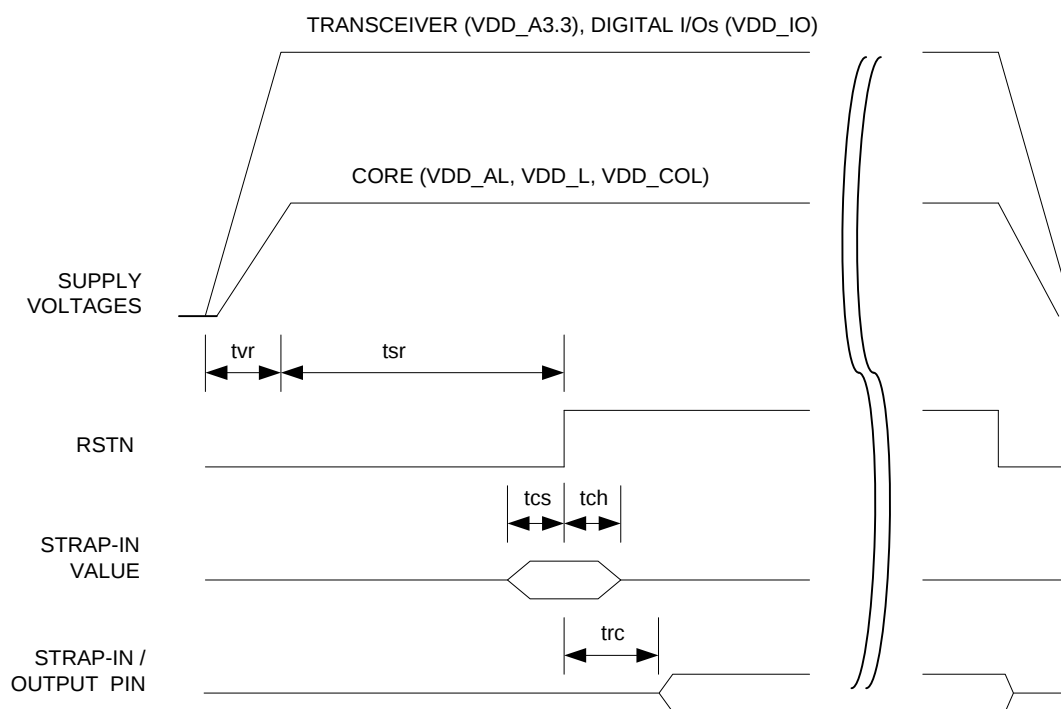


Figure 5. Reset Timing

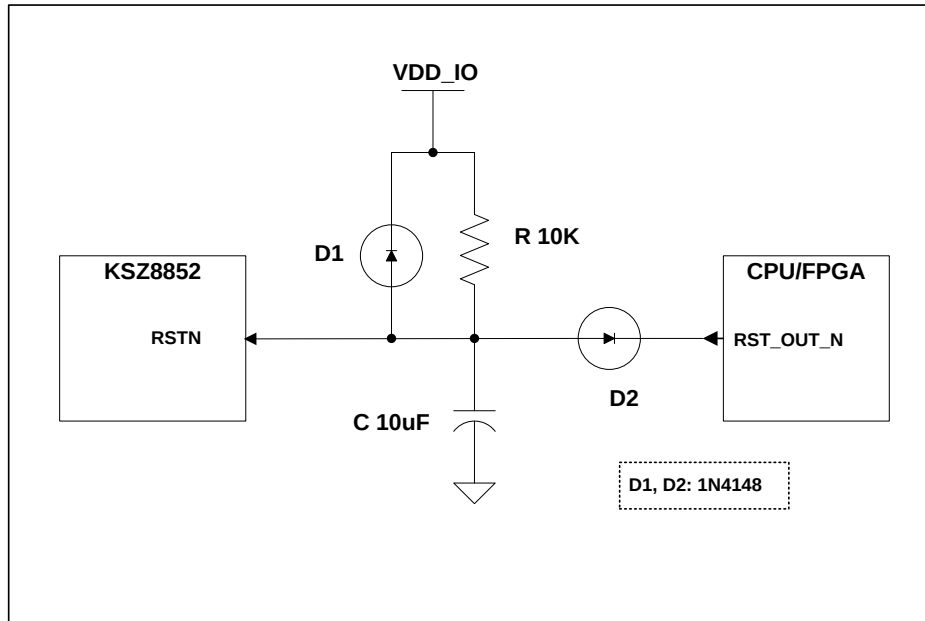


Figure 6. Sample Reset Circuit with Optional CPU Driven Reset

When RSTN is low, all outputs (except TX_CLK and RX_CLK on the MII interface of the KSZ8463MLI) are in a high-Z state. At the rising edge of reset, some specified output pins are sampled to set modes of operation for the device. These are referred to as strapping options. Setup and hold times must be met as specified in the datasheet. These strapping pins have a weak internal pull-up or pull-down resistor, but these may be overridden (or reinforced) with external pull-up or pull-down resistor of 1k Ω to 10k Ω . Once RSTN reaches a high level (approximately 50 to 60% of VDD_IO), the outputs will turn on. The time between these events is given as t_{RC} in the datasheets. Because this time is small, users must take care with their timing if they chose to actively drive the strapping pins from another chip. In such a case, it would be essential to have RSTN actively driven as an LVCMOS signal rather than using an RC circuit which is timed in micro- or milliseconds.

Software-Controlled Power Management

The KSZ84xx family offers several options for software controlled reset and power modes. Full details are given in the datasheets. The Global Reset Register (0x126) allows a reset of the whole chip, or only the Precision Time Protocol (PTP) module. Additionally, the Queue Management Unit (QMU) in the KSZ8441, KSZ8462 and KSZ8852 can be reset via this register.

[Table 3](#) summarizes the power management options that are available. Global soft power down is the simplest, and it achieves the lowest power consumption. It is entered by writing the appropriate bits in the PMCTRL register, and is exited when the host reads any register. In this mode, the device is unable to detect Ethernet link activity, so the host processor must decide on its own when global power down is appropriate for the KSZ84xx. Global power down also clears all registers in the KSZ8463. In the KSZ8441, KSZ8462 and KSZ8852, it clears all registers except those associated with the QMU.

Table 3. Power Management Capabilities

Power Feature	Devices	Registers	Summary
Global Soft Power Down	All	PMCTRL [1:0]	Host turns on and off.
Port Power-Down	All	P1CR4 [11] P2CR4 [11]	Host turns on and off.
Energy Detect Power-Down	All	PMCTRL [1:0] GST [7:0]	Global enable; each port powers down individually when inactive.
Energy Efficient Ethernet	All	P1EEEECS [15] P2EEEECS [15]	Individual port enable; auto-negotiated; specific protocol.
Wake-On-LAN	KSZ8441 KSZ8462 KSZ8852	IER [4] PMCTL [4] PMEE [2]	Sense magic packet or other conditions; triggers PME or INTRN pin to signal host CPU.

Energy detect mode is enabled via the same register bits. In this mode, each non-host port can power down independently if it detects that it is not connected to an active link partner. The time delay before entering sleep is the Go Sleep Time and is selectable in the GST register. While powered-down, it will still transmit a short pulse once per second in order to avoid deadlock between similarly configured ports. Upon detection of activity on the receive lines, the port will wake up within 100ns.

Energy Efficient Ethernet (EEE) is also supported, and can be enabled on a port-by-port basis (excluding the host port). To be fully enabled, it must be enabled via the appropriate register bit, and it must be enabled via auto-negotiation with the link partner. If the link partner doesn't support EEE, then it can't be activated. EEE, which is described in IEEE 802.3az, allows an individual PHY to enter a low power idle (LPI) state upon receiving a special signal from its link partner.

Wake-On-LAN (WOL) is supported by the KSZ8441, KSZ8462 and KSZ8852, but not the KSZ8463. With WOL, the device can detect a special magic packet, which is used to remotely manage network nodes. When received, the Power Management Event (PME) pin or interrupt (INTRN) pin can be asserted. They can also be configured to assert upon receipt of a network wake-up frame, or when the Ethernet port link goes up or down. PME or INTRN is used to signal the host processor to manage power from a software level.

Summary

This application note has covered the power and reset requirements for board designs using the KSZ84xx family of devices. The design is quite simple when the internal regulator is used. Alternatively, on-chip power and total system power may be saved by means of an external low voltage supply. The reset requirements are also very flexible. We concluded with a brief outline of the many power management features that the devices offer. Full details of these features are available in the datasheets.

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