IGLOO 2 Device Errata

Introduction

This Errata sheet contains information about known Errata specific to the IGLOO® 2 device family, as listed in the following table, and provides available fixes and solutions.

Table 1. Revisions Released per Device

Silicon Devices	Revisions	Device Status
M2GL005 (S)	All Temperature Grades	Production
M2GL010 (S, T, TS)	All Temperature Grades	Production
M2GL025 (T, TS)	All Temperature Grades	Production
M2GL060 (T, TS)	All Temperature Grades	Production
M2GL090 (T, TS)	All Temperature Grades	Production
M2GL150 (T, TS)	All Temperature Grades	Production

Table of Contents

Introduction....1

1. Errata for IGLOO 2 Devices....4

2. Errata Descriptions and Solutions....6
   - 2.1. VPP Must Be Set to 2.5V When Programming or Writing the eNVM at Industrial Temperature Range....6
   - 2.2. Overvoltage Support on MSIOs During Flash*Freeze Mode....6
   - 2.3. Verification of the FPGA Fabric at Junction Temperatures Higher than 50°C Erroneously Indicates a Failure....6
   - 2.4. DDR_OUT and I/O-Reg Functional Errata due to a Software Bug....6
   - 2.5. Dedicated Differential I/O Driving the Reference Clock of the CCC May Cause a Functional Failure Due to a Software Bug....6
   - 2.6. Power-Up Digest is Not Supported....7
   - 2.7. Programming of the eNVM Must Only Occur as Part of a Bitstream Containing the FPGA Fabric....7
   - 2.8. Updating eNVM from the FPGA Fabric Requires Changes in the FREQRNG Register....7
   - 2.9. SYSCTRL_RESET_STATUS Macro is Not Supported....7
   - 2.10. Zeroization is Not Supported....7
   - 2.11. The System Controller RC Oscillator Runs at 25 MHz After a Programming Recovery Operation....7
   - 2.12. ECC Point-Multiplication Service and ECC Point-Addition System Service are Not Supported....7
   - 2.13. Programming the FPGA Fabric Can Occur Only at Room Temperature....7
   - 2.14. Programming the eNVM Blocks Needs to Occur Independent of the Fabric....7
   - 2.15. PCIe Hot Reset Support Requires a Soft Reset Solution....7
   - 2.16. eNVM1 Becomes Inaccessible to FPGA Fabric Master After Executing SRAM-PUF Services....8
   - 2.17. After Successful Completion of 2-step IAP, User Design/Logic Cannot Access the Fabric SRAM (LSRAM and uSRAM) Blocks....8
   - 2.18. SRAM-PUF System Services may Take Two to Three Seconds to Complete....9
   - 2.19. The I/Os State during Programming is Changed from Z to Weak Pull-Up....9
   - 2.20. For S (Security) Grade Devices, User Must Not Enable Write Protection for Protected 4 K Regions, Also Known as Special Sectors in the eNVM....9
   - 2.21. Users Must Not Set Page Lock in eNVM0 for the 060 Device and eNVM1 for 090/150 Devices....9
   - 2.22. PCIe Hard IP Core Receive FIFO May Reach the Full Condition Resulting in Incorrect Data Passed to PCIe Subsystem and Cause the PCIe Core to Ignore Subsequent PCIe Traffic....9

3. Usage Guidelines for IGLOO 2 Devices....10
   - 3.1. Programming Support....10
   - 3.2. SHA-256 System Service....11
   - 3.3. Accessing the PCIe Bridge Register in the High-speed Serial Interface....11

4. Revision History....12

Microchip FPGA Support....13

Microchip Information....13
   - The Microchip Website....13
   - Product Change Notification Service....13
   - Customer Support....13
   - Microchip Devices Code Protection Feature....13

Legal Notice....14
Trademarks....14
Quality Management System....15
Worldwide Sales and Service....16

1. Errata for IGLOO 2 Devices

The following table lists the specific device Errata and the affected IGLOO 2 devices. Refer to the Marking Specification Details in the *PB0121:IGLOO 2 FPGA Product Brief* for this Die revision part marking specification.

Table 1-1. Summary of IGLOO 2 Device Errata

Errata No.	Errata	Silicon Revision(s) Affected													Software Errata
		M2GL005		M2GL010			M2GL025		M2GL060	M2GL090			M2GL150		
		0	1,2	0	1,2	3	0	1,2	0	0	1,2	3	0	1,2	
1.	VPP must be set to 2.5V when programming or writing the eNVM at Industrial temperature range	X[1]	—	X[1]	—	—	X[1]	—	—	—	—	—	—	—	—
2.	Overvoltage support on MSIOs during Flash*Freeze mode	X[1]	—	X[1]	—	—	X[1]	—	—	—	—	—	—	—	—
3.	Verification of the FPGA fabric at junction temperatures higher than 50 °C erroneously indicates a failure	X[1]	—	X[1]	—	—	X[1]	—	—	—	—	—	—	—	—
4.	DDR_OUT and I/O-Reg functional Errata due to a software bug	—	—	—	—	—	—	—	—	—	—	—	—	—	X[1]
5.	Dedicated differential I/O driving the reference clock of the CCC may cause a functional failure due to a software bug	—	—	—	—	—	—	—	—	—	—	—	—	—	X[1]
6.	Power-up digest is not supported	X[1]	—	X[1]	—	—	X[1]	—	—	X[1]	—	—	X[1]	—	—
7.	Programming of the eNVM must only occur as part of a bitstream containing the FPGA fabric	—	—	—	—	—	—	—	—	—	—	—	—	—	X[1]
8.	Updating eNVM from the FPGA fabric requires changes in the FREQRNG register	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	—
9.	SYSCTRL_RESET_STATUS macro is not supported	X[1]	—	X[1]	—	—	X[1]	—	—	X[1]	—	—	X[1]	—	—
10.	Zeroization is not supported	X[1]	—	X[1]	—	—	X[1]	—	—	X[1]	X[1]	—	X[1]	—	—
11.	The System Controller RC oscillator runs at 25 MHz after a programming recovery operation	—	—	NS[3]	X[1]	—	—	—	—	NS[3]	X[1]	—	—	—	—
12.	ECC Point-Multiplication service and ECC Point-Addition System service are not supported	—	—	—	—	—	—	—	—	X[1]	—	—	X[1]	—	—
13.	Programming the FPGA fabric can occur only at room temperature	—	—	—	—	—	—	—	—	X[1]	—	—	X[1]	—	—

.....continued

Errata No.	Errata	Silicon Revision(s) Affected													Software Errata
		M2GL005		M2GL010			M2GL025		M2GL060	M2GL090			M2GL150		
		0	1,2	0	1,2	3	0	1,2	0	0	1,2	3	0	1,2	
14.	Programming the eNVM blocks needs to occur independent of the fabric	—	—	—	—	—	—	—	—	X[1]	—	—	X[1]	—	—
15.	PCIe Hot Reset support requires a soft reset solution	—	—	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	—
16.	eNVM1 becomes inaccessible to FPGA fabric master after executing SRAM-PUF services	—	—	—	—	—	—	—	—	X[1]	X[1]	X[1]	X[1]	X[1]	—
17.	After successful completion of 2-step IAP, user design/logic cannot access the fabric SRAM (LSRAM and uSRAM) blocks	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	—
18.	SRAM-PUF system services may take two to three seconds to complete	—	—	—	—	—	—	—	—	X[1]	X[1]	X[1]	X[1]	X[1]	—
19.	The I/Os state during programming is changed from Z to weak pull-up	X[1]	—	X[1]	—	—	X[1]	—	—	—	—	—	X[1]	—	—
20.	For S (security) grade devices, user must not enable write protection for Protected 4 K Regions, also known as Special Sectors in the eNVM	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	—
21.	Users must not set page lock in eNVM0 for the 060 device and eNVM1 for 090/150 devices	—	—	—	—	—	—	—	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	—
22.	PCIe hard IP core receive FIFO may reach the full condition resulting in incorrect data passed to PCIe subsystem and cause the PCIe core to ignore subsequent PCIe traffic	—	—	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	—

Notes:

1. An “X” means that the Errata exists for that particular device and revision number.
2. A blank box means that the Errata does not exist or the feature does not exist for that particular device and revision number.
3. NS (Not Supported) means the Programming Recovery mode is not available in this revision.
4. Software Errata can be avoided by using Libero®SoC v11.4 SPI or a newer version.

2. Errata Descriptions and Solutions

This section shows the Errata descriptions and their solutions.

2.1 VPP Must Be Set to 2.5V When Programming or Writing the eNVM at Industrial Temperature Range

VPP can be set to 2.5V or 3.3V. However, when writing or programming the eNVM of Revision 0 of the M2GL005, M2GL010, and M2GL025 devices below 0 °C, VPP must be set to 2.5V.

For the VPP minimum and maximum settings, see the *DS0128:IGLOO 2 FPGA and SmartFusion 2 SoC FPGA Datasheet*. The eNVM reading, with VPP set to 3.3V or 2.5V, operates as intended.

2.2 Overvoltage Support on MSIOs During Flash*Freeze Mode

When the input voltage is driven above the reference voltage for a particular bank, additional current can be consumed in Flash*Freeze mode.

2.3 Verification of the FPGA Fabric at Junction Temperatures Higher than 50°C Erroneously Indicates a Failure

Standalone verification (STAPL VERIFY action) must be run at temperatures lower than 50 °C. If a VERIFY action is run at temperatures higher than 50 °C, a false verify failure may be reported. The Check Digest system services can be used to confirm design integrity at temperatures within the recommended operation conditions.

2.4 DDR_OUT and I/O-Reg Functional Errata due to a Software Bug

This Errata is applicable only if you have created or updated the design using Libero SoC v11.1 SP1 or v11.1 SP2.

The corresponding I/O does not function properly in the silicon due to the wrong software implementation of the I/O macro,if you have one of the following in the design:

- If you use DDR_OUT macro in the design
- If you combine an output or output enable register with an I/O using the PDC command, `set_io <portName>-register yes`

Solution:

Both Errata are fixed in Libero SoC v11.1 SP3. Migrate the design to Libero SoC v11.1 SP3 or a newer version, and re-run Compile and Layout.

2.5 Dedicated Differential I/O Driving the Reference Clock of the CCC May Cause a Functional Failure Due to a Software Bug

If the design has a dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug, and the device fails during silicon testing. There are several options to drive the ref clock of the CCC. One of the options is to drive from “Dedicated Input PAD x” (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the ref clock. This Errata exists when you choose the differential I/O option (dedicated differential I/O is used as CCC reference clock input).

This Errata cannot be detected in any functional simulation, and can only be detected in silicon testing.

Solution:

The Errata is fixed in the Libero SoC 11.1 SP3. Migrate the design to Libero SoC 11.1 SP3 or a newer version, and re-run Compile and Layout.

2.6 Power-Up Digest is Not Supported

Workaround:

Use NVM Data Integrity Check System service after the device is switched ON, and check the data integrity.

2.7 Programming of the eNVM Must Only Occur as Part of a Bitstream Containing the FPGA Fabric

The Bitstream Configuration dialog box in the Libero SoC allows the user to program the eNVM and the FPGA fabric separately. However, if Libero v11.1 SP2 or an older version is used, program the eNVM along with the FPGA fabric for the M2GL005, M2GL010, M2GL025, and M2GL050 devices. The fabric can be programmed separately, if needed.

Solution:

The Errata is fixed in the Libero SoC 11.1 SP3. Migrate the design to Libero SoC 11.1 SP3 or to a newer version, and re-run Compile and Layout.

2.8 Updating eNVM from the FPGA Fabric Requires Changes in the FREQRNG Register

When updating the eNVM from the FPGA fabric, the NV_FREQRNG register must be changed from 0x07(default) to 0x0F. eNVM reads are not affected.

Note: Refer to the AC429, page no 26, Section 4: Appendix 2: eNVM and eSRAM Write/Read Operations.

2.9 SYSCTRL_RESET_STATUS Macro is Not Supported

2.10 Zeroization is Not Supported

2.11 The System Controller RC Oscillator Runs at 25 MHz After a Programming Recovery Operation

After a programming recovery event, the System Controller operates at 25 MHz. In general, the System Controller must operate at 50 MHz after a programming recovery event.

Workaround:

For the System Controller to operate at 50 MHz, contact Microchip by creating a new case at microchip.my.site.com/s/newcase.

.

2.12 ECC Point-Multiplication Service and ECC Point-Addition System Service are Not Supported

2.13 Programming the FPGA Fabric Can Occur Only at Room Temperature

2.14 Programming the eNVM Blocks Needs to Occur Independent of the Fabric

Customer using Revision 0 of M2GL090 or M2GL150 devices must program the eNVM block independently in Libero v11.6 or older. If you want to program the eNVM block independently in Revision 0 of M2S090 and M2S150 devices using Libero v11.7, contact Microchip and create a new case at microchip.my.site.com/s/newcase.

2.15 PCIe Hot Reset Support Requires a Soft Reset Solution

On IGLOO 2 devices, a PCIe® Hot Reset requires a soft FPGA logic reset scheme, which clears the sticky bits of the PCI configuration space.

Workaround:

The application note *AC437:Implementing PCIe Reset Sequence in SmartFusion 2 and IGLOO 2 Devices* describes the PCIe Hot Reset reset scheme. However, this reset scheme causes PCIe violations in some cases:

- For the M2GL060/M2GL090T(S) devices there are no violations
- For the M2GL010/M2GL025/M2GL150T(S) devices, at Gen1 rates, there are no violations
- For the M2GL/M2GL025/M2GL150T(S) devices, at Gen2 rates, there are two PCIe CV violations:
  - Test case 1: TD_1_7 (Advanced Error Reporting Capability)
  - Test case 2: TD_1_41 (LinkCap2Control2Status2 Reg)

2.16 eNVM1 Becomes Inaccessible to FPGA Fabric Master After Executing SRAM-PUF Services

In the IGLOO 2 M2GL090/M2GL150 devices, the System Controller does not release the eNVM1 access after executing the following SRAM-PUF system services:

- Create User AC (Activation Code) service
- Delete User AC service
- Create User KC for an Intrinsic Key service
- Create User KC for an Extrinsic Key service
- Delete User KC service

The above system services are executed successfully. However, the eNVM1 is inaccessible to fabric master.

Any subsequent access to eNVM1 after this point, where eNVM1 is locked by the System Controller, results in a stall, and a Power on Reset (POR) is required to remove the stall.

Workaround:

Execute "Get Number of the Key Code (GET_NUMBER_OF_KC)" SRAM-PUF system services immediately after the above services.

- The additional GET_NUMBER_OF_KC services releases the eNVM1 access from the System Controller
- The firmware code for running SRAM-PUF services workaround must be executed from eNVM0, eSRAM,or DDR memories only, as the Fabric master does not get access to the eNVM1 that time

2.17 After Successful Completion of 2-step IAP, User Design/Logic Cannot Access the Fabric SRAM (LSRAM and uSRAM) Blocks

If LSRAM/uSRAM Read and Write access fails from the fabric path after performing 2-step IAP, perform a system reset or F*F Entry/Exit.

Workaround:

The user application must execute System Reset as soon as the IAP system service is completed. Otherwise, user write and read accesses to LSRAM/uRAM are not possible. The System Reset can be generated with the use of the tamper macro (availably in the Libero SoC Catalog). Immediately after the IAP service, the user logic checks the LSRAM/uRAM access. If access is denied, the user logic sends the reset request/interrupt to the System Controller via the tamper macro (by enabling the RESET Function in the tamper macro configuration window) and then the System Controller executes the system level reset.

For a design example on how to implement the workaround, contact Microchip by creating a new case at microchip.my.site.com/s/newcase.

2.18 SRAM-PUF System Services may Take Two to Three Seconds to Complete

This errata is fixed for devices manufactured after December 2016. Currently, SRAM-PUF services take max time of 100 ms.

> **Important:** *Devices with date codes prior to and including December 2016 still have this issue. SRAM-PUF services may take longer than 100 ms for such devices.*

For further information, contact Microchip by creating a new case at microchip.my.site.com/s/newcase.

2.19 The I/Os State during Programming is Changed from Z to Weak Pull-Up

The state of the I/O during programming is changed from Z to weak pull-up in the latest Die revisions. Affected Die revisions (marked with "X" in the Summary of IGLOO 2 Device Errata table) have I/Os that are tristated during programming.

2.20 For S (Security) Grade Devices, User Must Not Enable Write Protection for Protected 4 K Regions, Also Known as Special Sectors in the eNVM

For S (security) devices, there are two or four 4 KB regions per eNVM array that can be protected for read and write. These regions are known as Protected 4 K Regions or Special Sectors. If write protection is enabled for any of these regions, none of the locked pages inside the same eNVM block can be unlocked.

2.21 Users Must Not Set Page Lock in eNVM0 for the 060 Device and eNVM1 for 090/150 Devices

For 060, 090, and 150 device densities, each eNVM memory block has a user page lock bit (refer to PAGE_LOCK_SET register) to lock a page and prevent accidental writing. After the page lock is set in eNVM0 for the 060 device or eNVM1 for the 090/150 devices, the user will not be able to clear the lock for subsequent page updates later.

Workaround:

To use page lock feature, the user can use eNVM0 of 090/150 device and set/clear page lock using the master (for example, M3 or fabric). There is no workaround for the 060 device. User must contact SoC tech support if they already used page lock in the 060 device, which they need to unlock now.

2.22 PCIe Hard IP Core Receive FIFO May Reach the Full Condition Resulting in Incorrect Data Passed to PCIe Subsystem and Cause the PCIe Core to Ignore Subsequent PCIe Traffic

A condition has been identified with the IGLOO 2 PCIe interface where the PCIe hard IP block's receive FIFO may reach the full condition resulting in incorrect data passed to PCIe subsystem, and cause the PCIe core to ignore subsequent PCIe traffic. This only occurs under very specific conditions, as outlined in the associated PCN SYST-18UJME493.

Workaround:

This failure mechanism is isolated to the PCIe hard IP core within the FPGA device, where it cannot be corrected. To avoid the issue, the posted receive buffer must not become full. This can be accomplished using one of the options in PCN SYST-18UJME493. For more details, refer to this PCN: SmartFusion2, IGLOO 2 and RTG4 FPGA PCIe Receive FIFO Full.

3. Usage Guidelines for IGLOO 2 Devices

3.1 Programming Support

There may be package dependencies that may not expose certain programming interfaces. For device/package specific features, see *PB0121: IGLOO 2 FPGA Product Brief*.

Table 3-1. Revision 0 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SPI_SC	SPI_0	SPI_0	SPI_0	SPI_0
M2GL005 (S)	Yes	Yes	No	No	No	No
M2GL010 (S, T, TS)	Yes	Yes	No	No	No	No
M2GL025 (T, TS)	Yes	Yes	No	No	No	No
M2GL060 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	No	No	No	Yes[1]
M2GL150 (T, TS)	Yes	Yes	No	No	No	No

Note:

1. See Errata item 11.

Table 3-2. Revision 1 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0
M2GL005 (S)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL010 (S, T, TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]
M2GL025 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]
M2GL0150 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. See Errata item 11.

Table 3-3. Revision 2 Devices

ProgrammingMode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
ProgrammingInterface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0
M2GL005 (S)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL010 (S, T, TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]
M2GL025 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes[1]
M2GL150 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. See Errata item 11.

Table 3-4. Revision 3 Devices

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2-Step IAP	Programming Recovery
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0
M2GL010 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes
M2GL090 (T, TS)	Yes	Yes	Yes	Yes	Yes	Yes

3.2 SHA-256 System Service

Microchip recommends the message required to be on byte boundary when using SHA-256 System Service for the SmartFusion® 2 devices.

3.3 Accessing the PCIe Bridge Register in the High-speed Serial Interface

The PCIe Bridge registers must not be accessed before the PHY is ready. Wait for the PHY_READY signal (which indicates that the PHY is ready) to be asserted before updating the PCIe Bridge registers.

The PHY_READY signal is normally asserted within 200 µs after the device is powered up. Wait for 200 µs before accessing the PCIe Bridge registers.

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
B	05/2024	The following is the summary of changes made in revision B: • Updated Table 1-1 to add row 22. • Added errata item 2.22 PCIe Hard IP Core Receive FIFO May Reach the Full Condition Resulting in Incorrect Data Passed to PCIe Subsystem and Cause the PCIe Core to Ignore Subsequent PCIe Traffic .
A	04/2024	The following is the summary of changes made in revision A: • The document was updated to Microchip template. • The document number was changed from 55900198 to DS50003660. • Added a note in errata item 2.8 Updating eNVM from the FPGA Fabric Requires Changes in the FREQRNG Register. • Updated 2.18 SRAM-PUF System Services may Take Two to Three Seconds to Complete section to indicate that the errata has been fixed in devices manufactured after December 2016, resulting in faster (100 ms) running of SRAM-PUF system services. • Replaced the Microsemi links with Microchip links throughout the document.
1.4	07/2016	Updated text for errata item 2.19 The I/Os State during Programming is Changed from Z to Weak Pull-Up.
1.3	04/2016	Added errata items 2.20 For S (Security) Grade Devices, User Must Not Enable Write Protection for Protected 4 K Regions, Also Known as Special Sectors in the eNVM and 2.21 Users Must Not Set Page Lock in eNVM0 for the 060 Device and eNVM1 for 090/150 Devices.
1.2	12/2015	The following is the summary of changes made in revision 1.2: • Updated Table 1-1 to include the M2GL010 device in revision 3. • Added errata item 2.19 The I/Os State during Programming is Changed from Z to Weak Pull-Up. • Updated Table 3-4 to include the M2GL010 (T, TS) device. • Added solution for errata item 2.14 Programming the eNVM Blocks Needs to Occur Independent of the Fabric.
1.1	08/2015	Updated M2GL060 Revision from ES to Rev 0.
1.0	06/2015	The following is the summary of changes made in revision 1.0: • Combined M2GL005, M2GL010, M2GL025, M2GL060,M2GL090 and M2GL150 devices and die revisions to one centralized document. • Created a separate Errata for the M2GL050 device.

Microchip FPGA Support

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic

ISBN: 978-1-6683-4648-8

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	**Australia - Sydney** Tel: 61-2-9868-6733	**India - Bangalore** Tel: 91-80-3090-4444	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393
Atlanta Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455	**China - Beijing** Tel: 86-10-8569-7000	**India - New Delhi** Tel: 91-11-4160-8631	**Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829
Austin, TX Tel: 512-257-3370	**China - Chengdu** Tel: 86-28-8665-5511	**India - Pune** Tel: 91-20-4121-0141	**Finland - Espoo** Tel: 358-9-4520-820
Boston Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088	**China - Chongqing** Tel: 86-23-8980-9588	**Japan - Osaka** Tel: 81-6-6152-7160	**France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79
Chicago Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075	**China - Dongguan** Tel: 86-769-8702-9880	**Japan - Tokyo** Tel: 81-3-6880- 3770	**Germany - Garching** Tel: 49-8931-9700
Dallas Addison, TX Tel: 972-818-7423 Fax: 972-818-2924	**China - Guangzhou** Tel: 86-20-8755-8029	**Korea - Daegu** Tel: 82-53-744-4301	**Germany - Haan** Tel: 49-2129-3766400
Detroit Novi, MI Tel: 248-848-4000	**China - Hangzhou** Tel: 86-571-8792-8115	**Korea - Seoul** Tel: 82-2-554-7200	**Germany - Heilbronn** Tel: 49-7131-72400
Houston, TX Tel: 281-894-5983	**China - Hong Kong SAR** Tel: 852-2943-5100	**Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906	**Germany - Karlsruhe** Tel: 49-721-625370
Indianapolis Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380	**China - Nanjing** Tel: 86-25-8473-2460	**Malaysia - Penang** Tel: 60-4-227-8870	**Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44
Los Angeles Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800	**China - Qingdao** Tel: 86-532-8502-7355	**Philippines - Manila** Tel: 63-2-634-9065	**Germany - Rosenheim** Tel: 49-8031-354-560
Raleigh, NC Tel: 919-844-7510	**China - Shanghai** Tel: 86-21-3326-8000	**Singapore** Tel: 65-6334-8870	**Israel - Hod Hasharon** Tel: 972-9-775-5100
New York, NY Tel: 631-435-6000	**China - Shenyang** Tel: 86-24-2334-2829	**Taiwan - Hsin Chu** Tel: 886-3-577-8366	**Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781
San Jose, CA Tel: 408-735-9110 Tel: 408-436-4270	**China - Shenzhen** Tel: 86-755-8864-2200	**Taiwan - Kaohsiung** Tel: 886-7-213-7830	**Italy - Padova** Tel: 39-049-7625286
Canada - Toronto Tel: 905-695-1980 Fax: 905-695-2078	**China - Suzhou** Tel: 86-186-6233-1526	**Taiwan - Taipei** Tel: 886-2-2508-8600	**Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340
	China - Wuhan Tel: 86-27-5980-5300	**Thailand - Bangkok** Tel: 66-2-694-1351	**Norway - Trondheim** Tel: 47-72884388
	China - Xian Tel: 86-29-8833-7252	**Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Poland - Warsaw** Tel: 48-22-3325737
	China - Xiamen Tel: 86-592-2388138		**Romania - Bucharest** Tel: 40-21-407-87-50
	China - Zhuhai Tel: 86-756-3210040		**Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91
			Sweden - Gothenberg Tel: 46-31-704-60-40
			Sweden - Stockholm Tel: 46-8-5090-4654
			UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820