PD69104B1 Based Design of a 4-port Auto Mode System (IEEE® 802.3af/802.3at Compliant)

Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a 4-port Power over Ethernet (PoE) technology system, based on Microchip's 4-channel PoE manager PD69104B1.

This document allows system designers to integrate PoE capabilities, as specified in the IEEE® 802.3af and IEEE 802.3at standards, to an Ethernet switch.

PD69104B1, a 4-port PoE manager implements real time functions as specified in IEEE 802.3af and IEEE 802.3at standards. These include detection, classification, and port-status monitoring. Furthermore, it implements the system level activities such as power management and Management Information Base (MIB) support for system management. The PoE manager is designed to detect and disable disconnected Powered Devices (PDs) using DC disconnection method, as specified in the standard. An I^{2}C or UART interface is available for communication with a hosting system.

PD69104B1 operates in auto mode, managed using a host control or using an EEPROM that configures the system as it turns on.

This application note defines the following functions.

- Communication with the host controller through an I^{2}C bus
- PD69104B1 configuration

Features

- IEEE 802.3af-2003 compliant
- IEEE 802.3at-2009 compliant and two-event classification
- Configurable AT/AF modes
- Single DC voltage input (44 V to 57 V)
- Supports pre-standard PD detection
- Low power dissipation (0.36 Ω sense resistor and 0.3 Ω internal MOSFET R_{DS_ON})
- Internal power on reset
- Includes reset command pin
- Four direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable standard and legacy detection mode
- Power soft start mechanism
- On-Chip thermal protection
- Voltage monitoring or protection
- Built in 3.3 V and 5 V regulators
- Emergency power management supporting four configurable power bank I/Os
- LED support for every port
- Auto mode for stand-alone systems
- MAX_LED for indicating max power budget
- I^2C or UART communication
- Power management
- EEPROM support
- Wide temperature range is from –10 °C to 85 °C
- RoHS compliant
- 4-pair support
- An auto mode system is configured through one of the following three options.
  - Host I^2C communication
  - EEPROM configuration
  - Hardware configuration

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1. Circuit Description

The circuit is made of the following blocks.

- PD69104B1 4-ports auto mode circuit. See Figure 2-1.
- An isolation circuit for I^2C bus. See Figure 2-2.
- An EEPROM to configure PD69104B1 by I^2C communication. See Figure 2-1.

1.1 General Circuit Description

A 4-port configuration for PoE auto mode system, shown in Figure 2-1, comprises of a PoE manager circuit (PD69104B1) that functions as peripheral to a host controller. Host controller utilizes the I^2C or UART bus to control PD69104B1. Extended registers support operations are performed automatically by PoE manager circuits, while the PoE host controller performs power management and other tasks.

1.1.1 Communication Flow

The Host CPU issues commands, utilizing a dedicated I^2C or UART communication protocol to PD69104B1 through an isolation component.

This isolation is a basic requirement of IEEE 802.3 PoE standards.

1.1.2 Isolation

Used isolation circuitry comprises of opto-coupler and digital isolator destined to provide 1500Vrms isolation required by standards (IEEE 802.3af/IEEE 802.3at). See Figure 2-3.

The following isolation signals cross over the isolation circuitry.

- I^2C (SDA, SCL)
- Reset (xPoE_RESET)
- Interrupt (nINT). See Figure 2-2.

The following are the isolation voltage parameters from host side.

- $V_{IH} > 1.6$ V
- $V_{IL} < 0.4$ V
- $V_{OH} > 3$ V
- $V_{OL} < 0.2$ V

1.1.3 Main Supply

The PoE system operates within a supply range of 44 V to 57 V (802.3at high power port's supply range is 50 V to 57 V). To comply with UL SELV regulations, maximum output voltage should not exceed 60 V. System power supply must supply power for four ports. Each port can consume up to 40 W, 720 mA, depending on the current set.

1.1.4 Grounds

The following grounds are used in the system.

- Analog
- Digital
- Chassis
- Floating

Digital and analog grounds are electrically same ground. However, to reduce noise coupling, grounds are physically separated and connected only at a single point U3. See Figure 2-1.

The chassis ground is connected to switch’s chassis ground. This ground plane should be 1500Vrms isolated from PoE circuitry.

The floating ground is controller’s digital ground.

1.1.5 3.3 V Regulator

The PD69104B1 comprises of a built-in regulator used for the PD69104B1 internal circuitry and PoE domain side isolation circuit. The maximum output current when using the internal regulator is 5 mA. The external NPN transistor is used to decrease internal power dissipation and the output current is increased to 30 mA. The host (switch domain) should provide isolated 3.3 V/5 mA (2.7V ≤ VDD1 ≤ 3.6) to the host domain side of the isolation circuit.

1.2 Detailed Circuit Description

The following sections describe the overall block diagram of a PD69104B1 (See Figure 2-1).

1.2.1 Communication Interfaces

The interface between the Ethernet switch and PoE ICs is 1500Vrms isolation I^2C interface. Each side of the circuitry is fed by a separate power supply. The isolation circuit is as shown in Figure 2-3.

1.2.2 Control and Indication Signals

Control or indication signals are made of single hardware line type that runs between the host controller and the PoE manager. These signals are isolated to achieve 1500Vrms isolation (See Figure 2-3 and Figure 2-2).

- When nINT pin is configured to work as an interrupt pin, a signal generated by the PoE manager indicates events such as port on, port off, port fault, PoE manager fault, voltage out of range, and so on. nINT pin output voltage shall be greater than 3 V with a 10 KΩ external pull-up resistor to 3.3 V. If not utilized as nINT, the pin functions as a CAP or RES detection configuration pin.
- xPoE_RESET signal generated by the host, resets all the PoE managers and throws an isolation reset line as shown in Figure 2-3. All the PoE managers reset input lines must be connected with a pull-up resistor.

The reference for internal voltages within the PoE manager is set by a precision resistor of 30.1 KΩ (R15). See Figure 2-1 for more information.

1.2.3 I^2C Interface

Host controller communicates with the PoE managers using I^2C communication.

I^2C communication between host CPU and the PD69104B1 is managed by setting the address of the ICs. This is made by selecting add0 to add3 pins that are connected to 3.3 V or GND.

These pins set to I^2C address as shown in Figure 2-1.

1.2.4 UART

External Host can communicate with PD69104B1 using UART protocol. To enable UART, pin 34 (COMM_MODE) should be connected to AGND. When UART is active, EEPROM is not functional.

1.2.5 Ground Interface Connection (AGND)

Power supplies ground connector enables the current path back to the power supply.

Ground connection is capable of carrying all the string currents back to the power supplies.

1.2.6 Thermal Design

Design for IEEE 802.3at PoE standard must consider the power dissipation of PoE manager, associated circuitry, and maximum ambient operating temperature of the switch. Adequate ventilation and airflow should be a part of the design to avoid thermal over-stress on components.

The application's thermal design must consider the temperature derived by the power dissipation of the switch and by the PoE daughter board, when powered at maximum load.

1.2.7 Current Set

When a port is in auto mode, ICUT and ILIM is automatically set after the port powers up successfully. Levels for ICUT and ILIM depends on the following parameters.

- Chip hardware configured on pin 33

- EEPROM configured by communication
- Host CPU configuration by communication

See current set description in the datasheet for full parameters.

1.2.8 EEPROM

When PD69104B1 is configured to work with EEPROM, pin 34 (COMM_MODE) should be open. EEPROM (See U4 at Figure 2-1) communicates with PoE manager by dedicated I^2C lines (pin 42 and pin 43) as shown in Figure 2-1. In multi PoE managers system, each system must have its own EEPROM.
Note: For EVB—When EEPROM is needed to be programmed, R6 and R7 must be removed to allow the programmer to communicate with the EEPROM and not the PoE manager.

1.2.9 LED Indication

- When PD69104B1 turns one of its ports on, the LED (pins 7, 8, 29, and 30) of this port is activated.
- MAX_LED analog output indication that consumption is below the power guard band determined by the user.

Table 1-1. LED Indication

Pin	Status	LED
LED <3:0>	Port power on	On
	Power management event	The LEDs blink at 0.4 Hz
	Port overload Port short circuit Port failed at startup	The LEDs blink at 0.8 Hz
	V_{main} out of range or over temp	All LEDs blink at 3.3 Hz
	Port off	Off
	4-pair on	Two LEDs are turned on
	4-pair off	Two LEDs are turned on
MAX_LED	Total power consumption is below the power guard band determined by the user	Off
	Total power consumption is above the power guard band, but below the total budget.	On
	Total power consumption is above the total budget or power integral is still positive	Blink

1.2.10 Output Protection

The PD69104B1 PoE manager is a UL 2367 (category QVRQ2) recognized component that fulfills Limited Power Source (LPS) requirements as per IEC62368-1 ED2 for systems whose total power is less than 250 VA. For systems whose total power is greater than 250 VA, F1 to F4 are needed to fulfill the LPS requirements specified in the safety standards IEC 62368-1 ED2. For more information, see *AN3527, Compliance to Limited Power Source Requirements*.

1.2.11 4-Pair

PD69104B1 is configured to work in 4-pair mode, that is, the port 1–port 2 and port 3–port 4 are synchronized to be turned on together when PD 4-pair mode is connected.

To work in a 4-pair mode, pin 32 (4_PAIRS) should be connected to VCC.

In each pair, the second port (port 1 and port 3) are the primary or main ports and the first port (port 0 and port 2) are secondary or replica ports.

2. Schematics

The following are the schematics of PoE system.

Figure 2-1. 4-Ports Auto Mode Circuit

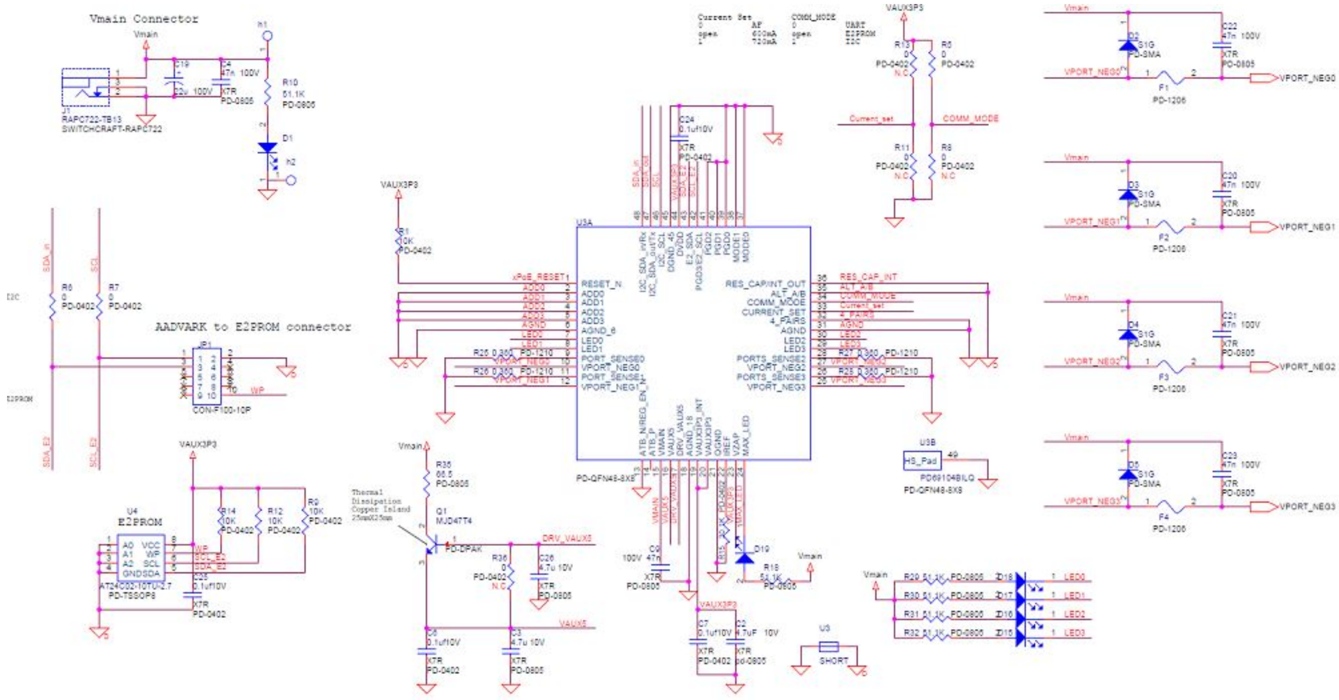


Figure 2-2. Interrupt Isolation Circuitry

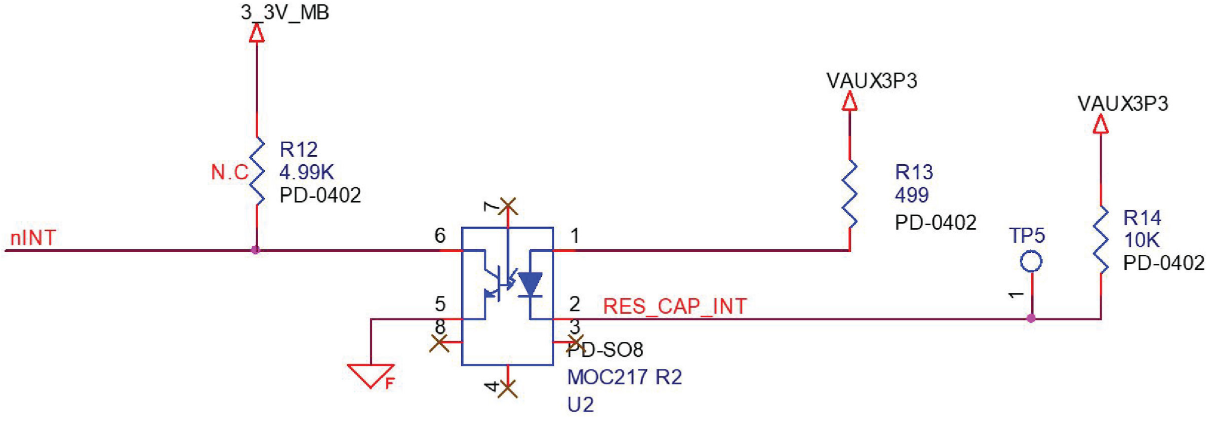
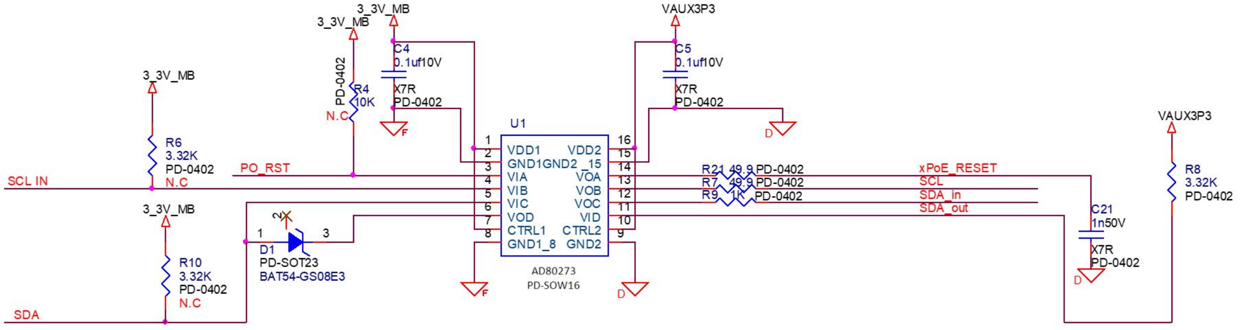


Figure 2-3. I²C and Reset Isolation



3. Bill of Materials for PoE System

The following table lists the bill of matierials for PoE system.

Table 3-1. Main Components

Block	Quantity	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
Main	3	C2, C3, C26	CAP CRM 4.7 µF 10 V 10% X7R 0805	PD-0805	Taiyo Yuden	LMK212B7475KG-T
	1	C4	CAP CRM 47 nF 100 V 10% X7R 0805	PD-0805	Murata	GRM40X7R473K100
	4	C6, C7, C24, C25	CAP CER 0.1 µF 10 V 10% X7R 0402	PD-0402	Walsin	0402B104K100CT
	1	C9	CAP CRM 47 nF 100 V 10% X7R 0805	PD-0805	Novacap	0805B473K101CTM
	1	C19	CAP ALU 22 µF 100 V 20% 105C 8X10.2 2000Hr	D8H10_2F9P3_2-SMD	Sanyo	100CE22FS
	4	C20, C21, C22, C23	CAP CRM 47 nF 100 V 10% X7R 0805	PD-0805	Vishay	VJ0805Y473KXBAT
	6	D1, D15, D16, D17, D18, D19	LED SuperYelGrn 100-130º 20-40mcd h=1 0603	led-0603-a	Everlight	19-21-SYGCS530E3TR8
	4	D2,D3,D4,D5	DIO RECOV. REC 400 V 1 A SMA SILICON	PD-SMA	Diodes Inc.	S1G
	4	F1,F2,F3,F4	FUSE FST BLO 1.5 A 63 V 1206	PD-1206	AVX	F1206B1R50FW-TR

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Block	Quantity	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
	1	Q1	TRN NPN 250 V 1 A 15 W	D-Pak SMT	STMicro	MJD47T4
	4	R1, R9, R12, R14	RES TCK FLM 10 K 1% 62.5 mW 0402	PD-0402	Vishay	CRCW0402-1002F RT7
	3	R5, R6, R7	Resistor, 0 Ω, 5%, 1/16 W 0402	PD-0402	ASJ	CR10-000ZK
	4	R8, R11, R13, R36	Resistor, 0 Ω, 5%, 1/16 W 0402	PD-0402	ASJ	CR10-000ZK
	6	R10, R18, R29, R30, R31, R32	RES TK FLM 51.1 K 125 mW 1% 0805	PD-0805	Yageo	RC0805FR-0751K1L
	1	R15	RES TK FLM 30.1 K 1% 62.5 mW 0402	PD-0402	Panasonic	ERJ2RKF3012X
	4	R25, R26, R27, R28	RES TCK FLM 0.360R 1% 0.5 W 200PPM 1210	PD-1210	Rohm	MCR25JZHFLR360
	1	R35	RES TCK FLM 66.5R 125 mW 1% 0805	PD-0805	Yageo	RC0805FR-07100RL
	1	U3A/B	4-ports PSE IC auto mode	PD-QFN48-8x8-1	Microchip	PD69104B1ILQ
	1	U4	EEPROM 2WIRE 2K 256 X 8 TSSOP8	PD-TSSOP8	Microchip	AT24C02-10TU-2.7

Table 3-2. Interrupt Isolation Circuitry

Quantity	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
1	R12	Resistor, 4.99K 1%, 1/16 W	PD-0402	Yageo	RC0402FR-074K99L
1	R13	RES TCK FLM 499R 1% 62.5 mW	PD-0402	Bourns	CR0402-FX-4990-E
1	R14	RES TCK FLM 10K 1% 62.5 mW	PD-0402	Yageo	RC0402FR-0710KL

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Quantity	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
1	U2	IC OPTOISOLATOR MOC217	PD-S08	Fairchild	MOC217R2-M

Table 3-3. I^{2}C and Reset Isolation

Quantity	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
3	R6, R10, R8	RES TCK FLM 3.32K 1% 62.5 mW SMT	PD-0402	Bourns	CR0402-FX-3321-ELF
1	D1	Diode Schottky Dual 30 V CC BAT54C	PD-SOT23	Diodes Inc.	SGE2565-3LF
1	R4	RES TCK FLM 10K 1% 62.5 mW	PD-0402	Yageo	RC0402FR-0710KL
1	U1	IC Dig.Iso	PD-SOW16	Analog Devices	AD80273ARWZ RL [1]
2	C4, C5	CAP CER 0.1 µF 10 V X7R 10%	PD-0402	Samsung	CL05B104KP5NNNC
2	R21, R7	RES TCK FLM 49.9R 1% 62.5 mW	PD-0402	Samsung	RC1005F49R9CS
1	R9	RES TCK FLM 1K 1% 62.5 mW	PD-0402	Rohm	MCR01MZPF1001
1	C21	Capacitor, X7R, 1 nF 50 V 10%	PD-0402	Yageo	CC0402KRX7R9BB102

Note: 1. Special part number for Microchip PoE application and preferential pricing for Microchip customers.

4. PCB Layout

This section provides detailed PCB layout guidelines for the the PoE section based on the PD69104B11.

4.1 Isolation and Termination

According to the IEEE 802.3af and the IEEE 802.3at standards, certain isolation requirements need to be met in all PoE equipment. Additionally, EMI limitations must be considered, as specified in the FCC and European EN regulations.

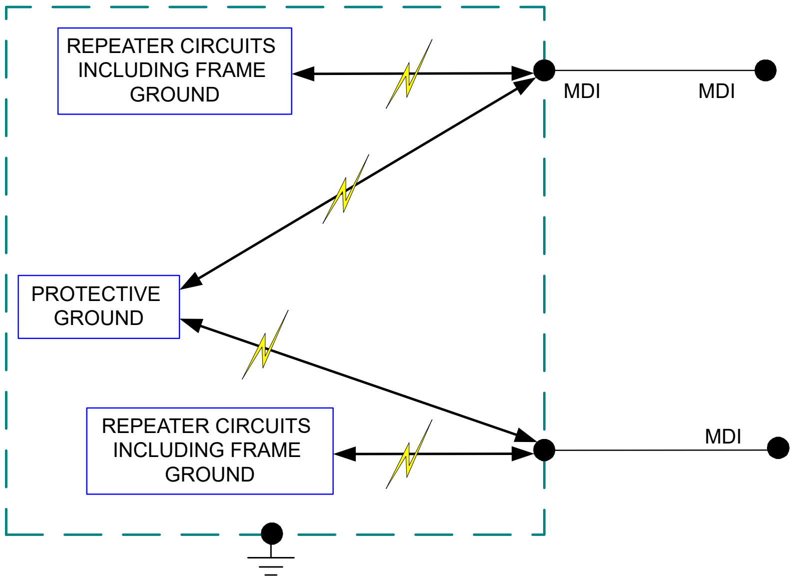
These requirements are considered by PoE switch vendors, while designing the switch circuitry. However, when a PoE manager is integrated into a switch, special design considerations must be met, due to the unique combination of data and power circuitries.

The following sections define these requirements and provide recommendations for their implementation, so as to assist designers in meeting those requirements and in integrating Microchip's PoE chip set and daughter boards.

4.1.1 Isolation

As specified in the IEEE PoE standards, 1500 Vac rms isolation is required between switch's main board circuitry, including protective and frame ground, and the Media Dependent Interface (MDI). The following figure shows the overall isolation requirements.

Figure 4-1. Isolation Requirements Scheme Meeting Requirements



Reference to environment A

1. IEEE 802.3 Repeater 500Vrms min (27.5.3.1 ; 9.7.1)
2. IEEE 802.3 Repeater, PMA to MDI 1500Vrms min (23.5.1.1)
3. UL1950: 1500Vrms

⚡ 1500= Vrms min

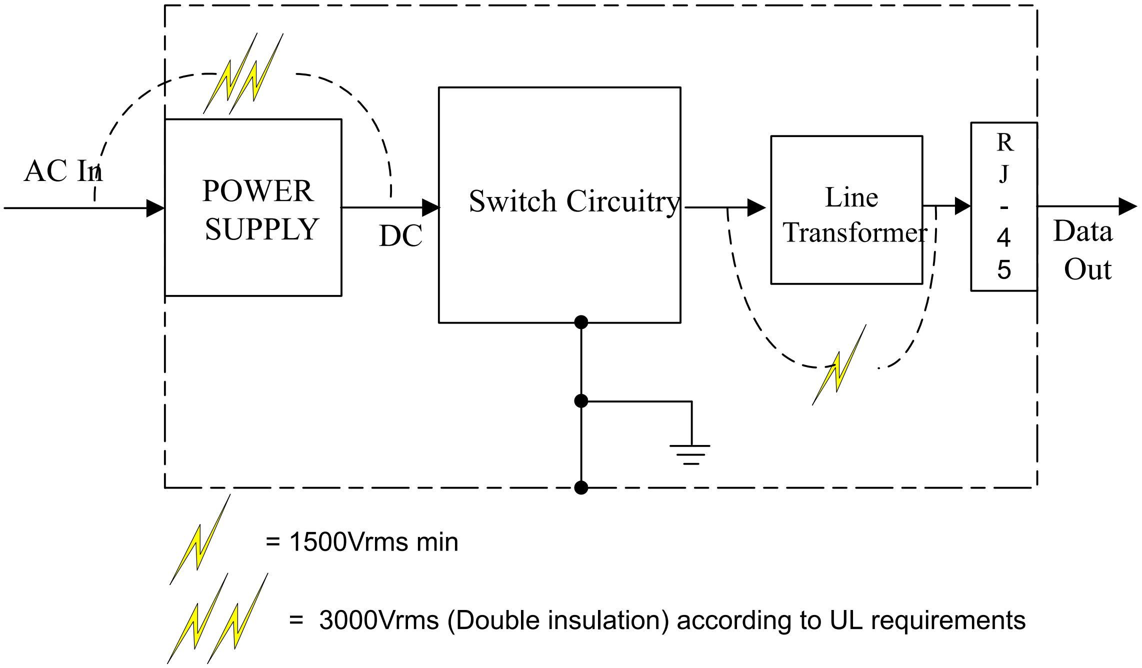
PMA: Physical Medium Attachment
MDI: Media Dependent Interface

4.1.2 High Voltage Isolation

For a switch without PoE circuitry, isolation requirements between the physical input terminals and the data connectors are met by an isolated AC/DC power supply and isolated pulse transformers (see Figure 4-2).

When integrating a PoE circuitry into a switch, the output power can be supplied through the central tap of the pulse transformer's secondary side (unless power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation, if the PoE ground or DC input is connected to the switch's circuitry or ground.

Figure 4-2. Switching Circuitry



To comply with the isolation requirements, the PoE managers must be isolated in regard to all other switch circuitries. Use one of the following methods.

- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry (see Figure 4-3).
- A single DC input (separate power supplies) for both the switch and PoE circuit as well as additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry (see Figure 4-4).

Figure 4-3. Switch Circuitry with Two DC Sources

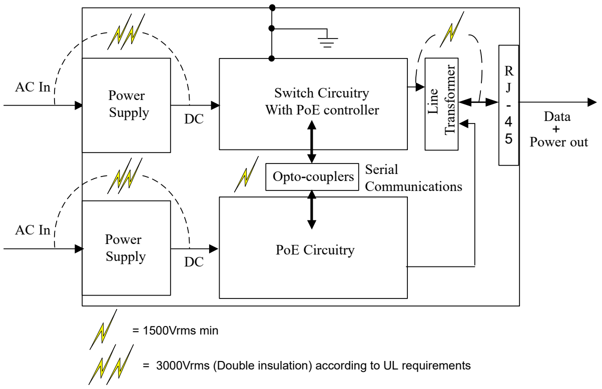
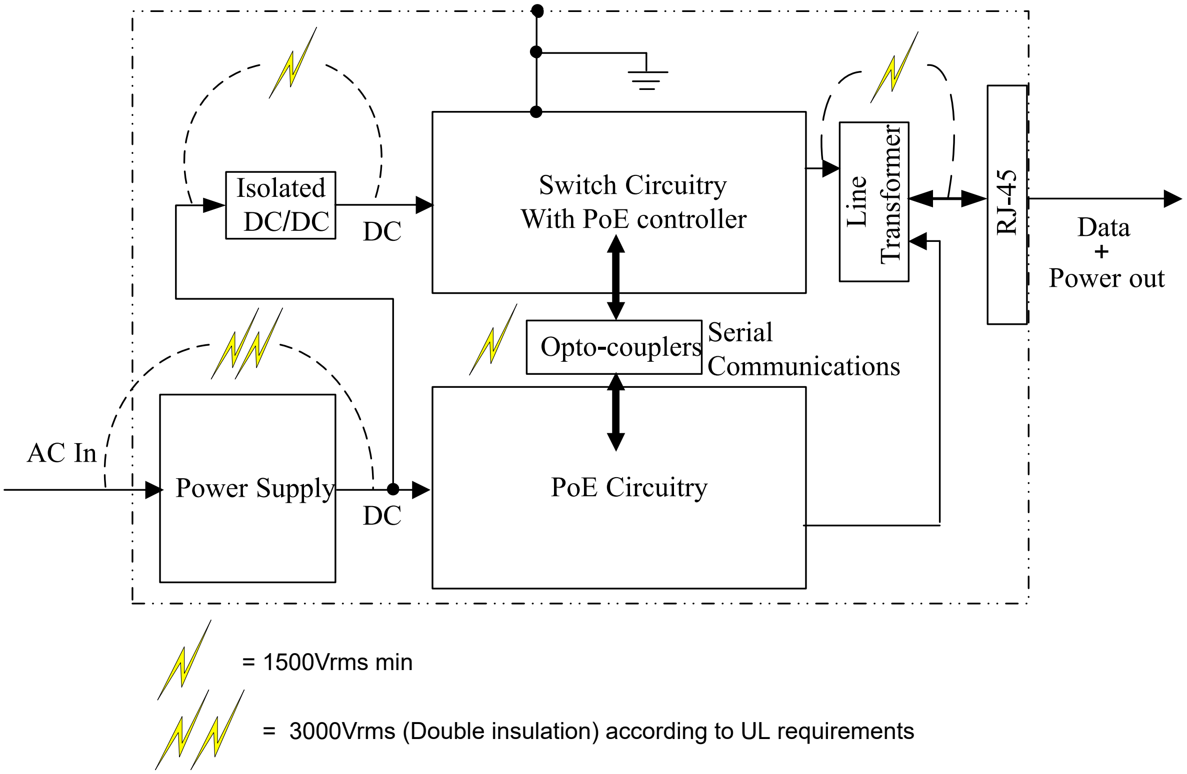


Figure 4-4. Switch Circuitry with a Single DC Source



To maintain 1500Vrms isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is required. This provides a safe margin for hi-pot requirements.

4.1.3 PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations might be needed when connecting the PoE circuit output terminals to the switch circuitry (see Figure 4-5). In most PoE systems, 0 Ω resistors for R1 and R2 are used. However, certain systems might benefit from 75 Ω resistors. Filtering provisions must be made. In quiet PoE systems, the EMI filter can be replaced (bypassed) using R3 and R4.

The following lists the circuitry for the recommended filter.

- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

Since each system is a unique EMI case, this circuit is a good starting point for EMI suppression.
Note: For best EMI performance and to avoid additional noise accumulated on the lines between filter and port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs or the spare pairs. Both methods are detailed in Figure 4-6 which illustrates an MDI-X (or Auto MDI-X) connection associated with the switch.

4.1.4 Isolating the Stacked Modular Jack Assembly

IEEE PoE standards require 1500Vrms isolation between PoE voltages and frame ground (EGND). The RJ-45 jack assemblies have a metal cover of 80 mils that almost reaches the PCB surface.

Maintain an 80 mils traces clearance between EGND traces for RJ-45 modular jack assembly metal covering and for adjacent circuit paths and components. To prevent 1500Vrms isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ-45 connector assemblies.

PoE technology involves voltages as high as 57 VDC. Therefore, plan adjacent traces for 100 VDC operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

Figure 4-5. Recommended EMI Filter

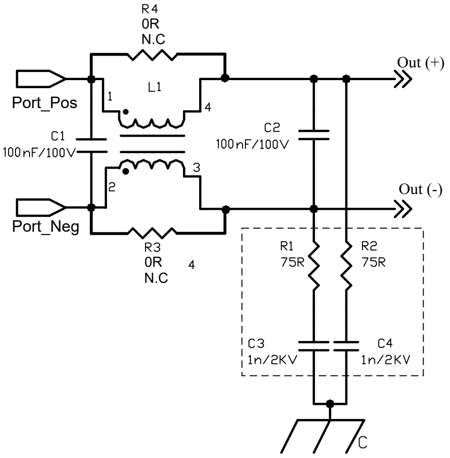
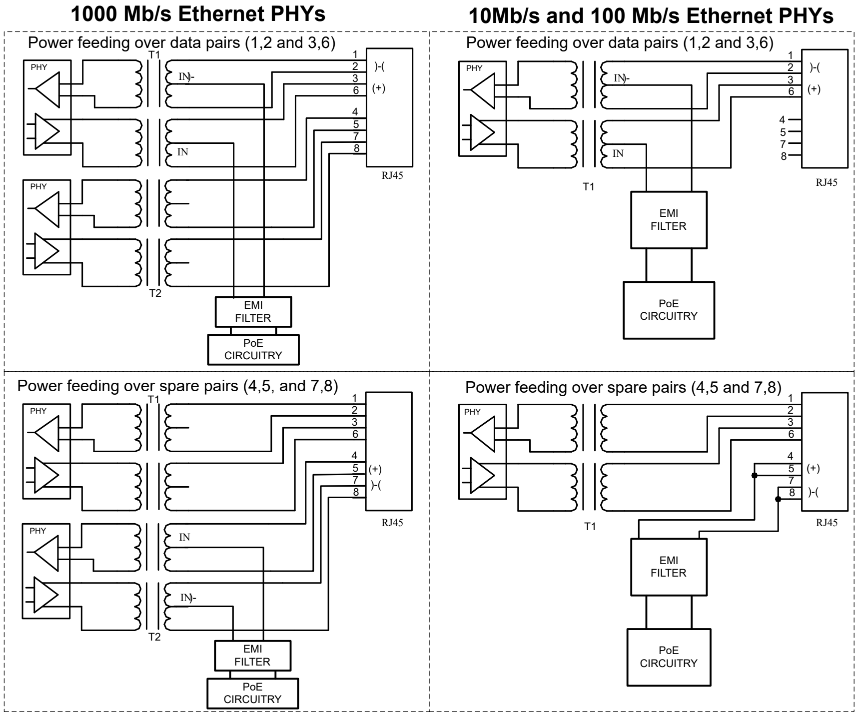


Figure 4-6. Output Ports Design Details



4.2 Layout Guidelines

Microchip's PD69104B1 PoE manager is designed to simplify the integration of PoE-circuitry into switches, based on the IEEE PoE standards. The pin-out arrangement is configured for optimal PCB routing. The following are Microchip's recommendations for proper PCB layout.

- 5 V voltage source (VAUX5) (1)
- 3.3 V voltage source (VAUX3P3) (2)
- Sense resistor for current measurement (3)
- Output capacitor used for filtering (4)
- Protection fuse (5)
- Protection diode against reverse polarity (6)
- RESET, I^2C bus, and I^2C address lines (7)
- Power good inputs (8)

Note: The VAUX5 supply might include an external transistor connected to pin 16, destined to increase current drive for external circuitry. To prevent heat from being transferred to the PD69104B1, place this transistor away from the PoE managers.

Figure 4-7 describes the various circuits and elements surrounding the PD69104B1 PoE manager in the block diagram. This block diagram includes the following peripheral elements, identified by numbers.

For more information on the interconnection circuitry of the PD69104B1, see the application notes listed in the 5. References section.

The provided circuitry is intended to facilitate the design of a switch when integrating a PoE capability into it.

4.2.1 Locating PoE Circuitry in a Switch

To minimize the length of high current traces and RFI pick-up, place the PoE circuitry close to the switch's pulse transformers. Circuit can be fully integrated into switch's PCB, or can easily be placed on top of the switch using daughter board PoE application. Typical integration of PoE modules inside a switch is shown in Figure 4-9 and Figure 4-10.

4.2.2 Ground and Power Planes

Since the Chip Set PoE solution (PD69104B1) is a mixed-signal (analog and digital) circuitry, care must be taken when routing the ground and power signals lines.

Reference design is a four layer board: top, mid1, mid2, and bottom. The main planes are Vmain/AGND and DGND.

Ground planes are crucial for proper operation and must be designed in accordance with the following guidelines, as shown in Figure 4-11.

- Separate analog and digital grounds, with a gap of at least 40 mils.
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD69104B1 (see *Thermal Pad Definition and Design*). AGND should be the lower layer.
- Earth ground is used to tie in the metal frame of the RJ-45 connectors. This ground is routed separately and connected to the switch's metal chassis/enclosure to maintain 80 mils traces clearance between EGND traces and other traces.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds as shown in Figure 4-12 and Figure 4-13.
- Grounding layout is implemented as described in Figure 4-13.
- To minimize noise effects from the heavy currents flowing to the ports, a number of separate grounding areas are essential in the design. Establish several separate ground areas to concentrate sensitive circuits, apart from the main grounding surfaces.
- To connect various DGND points and to enable stable impedance to the I^2C bus traces, extend the digital ground (DGND) surface under pin 35–pin 48 of the PD69104B1 managers.
- Rsense resistors for each PoE manager are all connected to local star point. The star center is connected to the analog ground (AGND) using four tied power via's of 6 mil diameter each (see Figure 4-12, Figure 4-13 and Figure 4-14).

- In addition, the Rsense resistors' star point connection to the PD69104B1 utilized as #0, is to be the focal interconnection point for the digital and analog grounds (see Figure 4-13).
- Leave spacing for a ceramic 1 nF bypass capacitor near each PoE manager (marked as Cb in Figure 4-13) between the analog and digital layers near each PoE manager. The capacitors form low impedance paths for digital driving signals.
- Leave spacing (provision) for two parallel and inversed Schottky diodes (Da, Db, and Figure 4-13) between analog and digital layers near each PoE manager. The diodes form low impedance paths for highly energized signals running between analog and digital layers and enhance circuit immunity.

The power and return (ground) planes for the 48 V supply must be designed to carry 35 A continuous current, based on full 48-port capacity. Minimize DC power losses on this plane by using a wide copper land.

When implementing the PoE circuitry on a daughter board, the high current is not routed through the daughter board but as the return path as shown in Figure 4-7.

4.2.3 Current Flow through PoE Application

The following steps show the port's current flows in a DC disconnect application.

1. Switch's power supply provides a positive line, reaching the center taps through a mother-board, on a wide trace (not through DB).
2. From the center tap of the line transformer through switch's RJ45 to the PD side.
3. The return current from the PD flows through RJ45 and line transformer to DB PoE circuitry.
4. From DB analog ground (AGND) the current flows back to switch's power supply negative, through harness.

Note: The positive port's heavy current flows directly to the PD side without going through PoE DB managers.

4.3 Specific Component Placement

4.3.1 Peripheral Components

The following gaps must be maintainted to prevent heat transfer among various components.

- Minimum gap between PD69104B1s must be 45 mm.
- To prevent a hot spot on the PCB, do not group sense resistors together under full load conditions. Leave at least 10 mm between PD69104B1 and its sense resistors.

4.3.2 PD69104B1 PoE Manager and Peripherals

The side of the PoE manager that includes pin-37 to pin-48 must face the digital ground (DGND plane). The pins function as communication and control pins for the manager (connected between the PoE manager and the PoE controller through the isolation circuitry).

Locate the bypass capacitors for the PoE manager supply input, close to the relevant pin. In cases where two bypass capacitors are placed on the same line, locate the lower value capacitor closer to the pin on the same layer and place the higher value capacitor at a more distant location.

Locate VAUX5 and VAUX3P3 0.1 µF and 4.7 µF filtering capacitors close to PoE manager pins 16 and 20, respectively.

4.4 Conductor Routing

4.4.1 General Guidelines

Conductor (or printed lands) routing is performed as practiced in general layout guidelines.

- Conductors that deliver a digital signal are routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.
- The total resistance of all sense resistor traces (both sides) needs to be 6 mΩ.

4.4.2 Specific Requirements for Clock and Sensitive Signals

The following are the issues that need special design considerations.

- Each PD69104B1's port incorporates a current sense resistor. For proper power management and control, layout these lines so that the adjacent ports' current flow or excessive path resistance does not impede measured current. Use a single common point to aggregate the current flow of all four ports to the analog ground (AGND) layer. This point is called the local PoE manager star point (see Figure 4-12, and Figure 4-13). Designing the total layout path (traces resistance from `PORT_SENSEx` pin to AGND star point) is crucial for an accurate resistance value, since a wrong resistance value results in a current measurement error and unreliable power management. Parasitic resistance added by the layout traces must be 6 mΩ. Since routing requires narrow traces in some areas, wide traces in other areas are necessary to achieve a total trace resistance of 6 mΩ.
- The local star point carries high current from the sense resistors to AGND. To achieve this, use four tied power vias of 6 mil diameter each (see Figure 4-14). Avoid using plugged vias to preclude temperature rise.
- Route a senses trace (`SENSE_NEG`) from QGND (pin-21) to the local PoE manager star point.
- PD69104B1's AGND (pin-6, pin-18, and pin-31) must also be connected directly to the local PoE manager star point through individual traces.
- The IREF resistor used for current reference (connects to pin-22), is directly connected to QGND (pin-21).
- Route the I^{2}C/UART communication clock (SCL) line from the host so that it does not disturb the other lines. Two ground lines (connected to DGND) could be routed with the clock line to isolate it from rest of the lines.

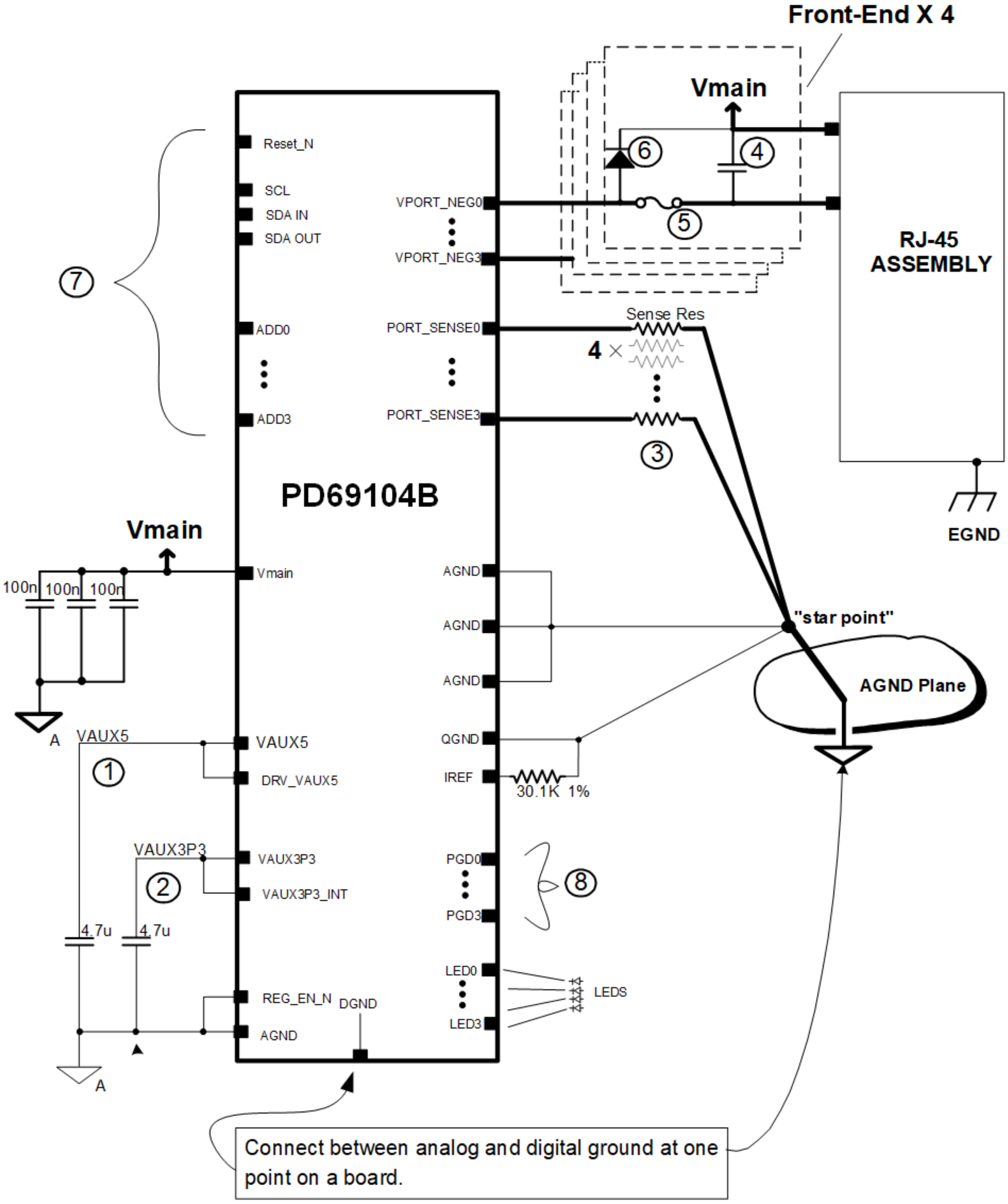
4.4.3 Port Outputs

For robust design, the ports output traces are 45 mils wide to handle maximum current and port power.

However, to obtain a 10°C (maximum) copper rise, set the minimum width for traces in accordance with the layer location and copper thickness.

- For two ounce copper, external layer must be 15 mils.
- For two ounce copper, internal layer must be 20 mils.
- For one ounce copper, external layer must be 25 mils.
- For one ounce copper, internal layer must be 30 mils.
- For half ounce copper, external layer must be 30 mils.
- For half ounce copper, internal layer must be 55 mils (20°C copper rise).
- The ports output traces must be short and parallel to each other to reduce RFI coupling and to keep the series resistance low.
- The PoE output ports must be connected to the switch's pulse transformers as shown in Figure 4-6. The common mode choke is used to reduce RFI noise. A Bob-Smith termination (resistor-capacitor) to chassis ground is optional. The circuit is located close to the pulse transformer.

Figure 4-7. Component Identification for PD69104B1 Circuitry



Connect between analog and digital ground at one point on a board.

Figure 4-8. Component Identification for PD69104B1 Circuitry

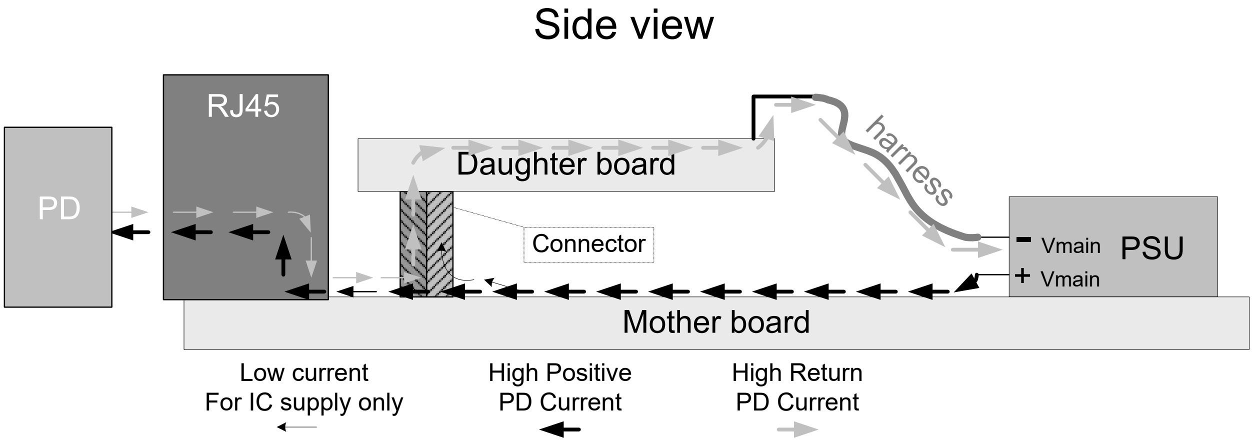


Figure 4-9. Block Diagram – PoE Circuitry inside the Switch

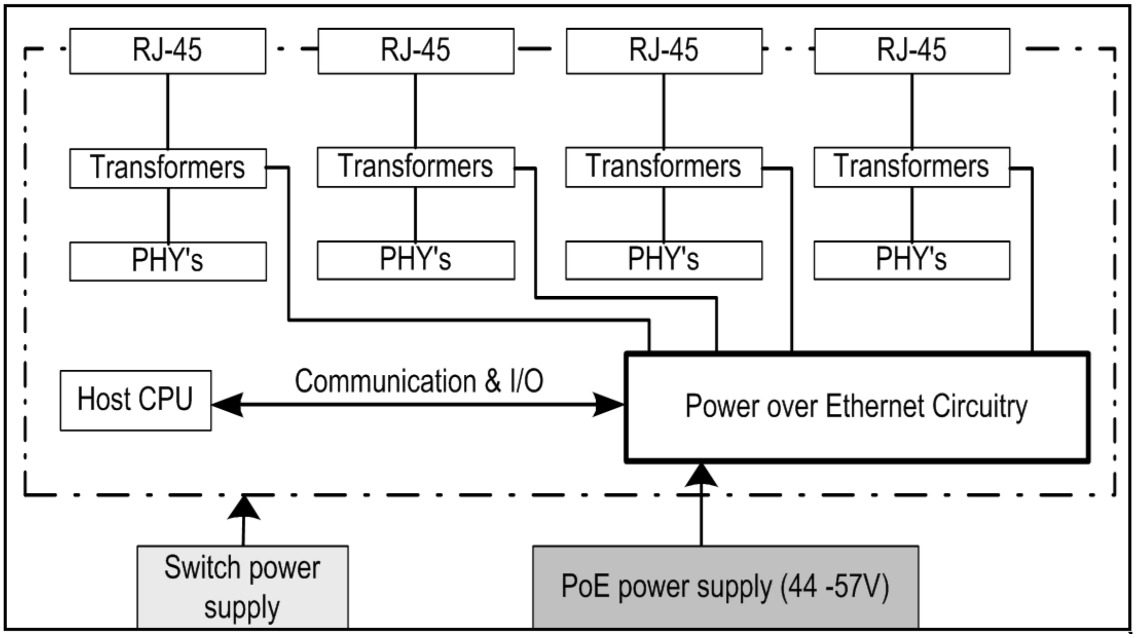


Figure 4-10. PoE DB Circuitry inside the Switch

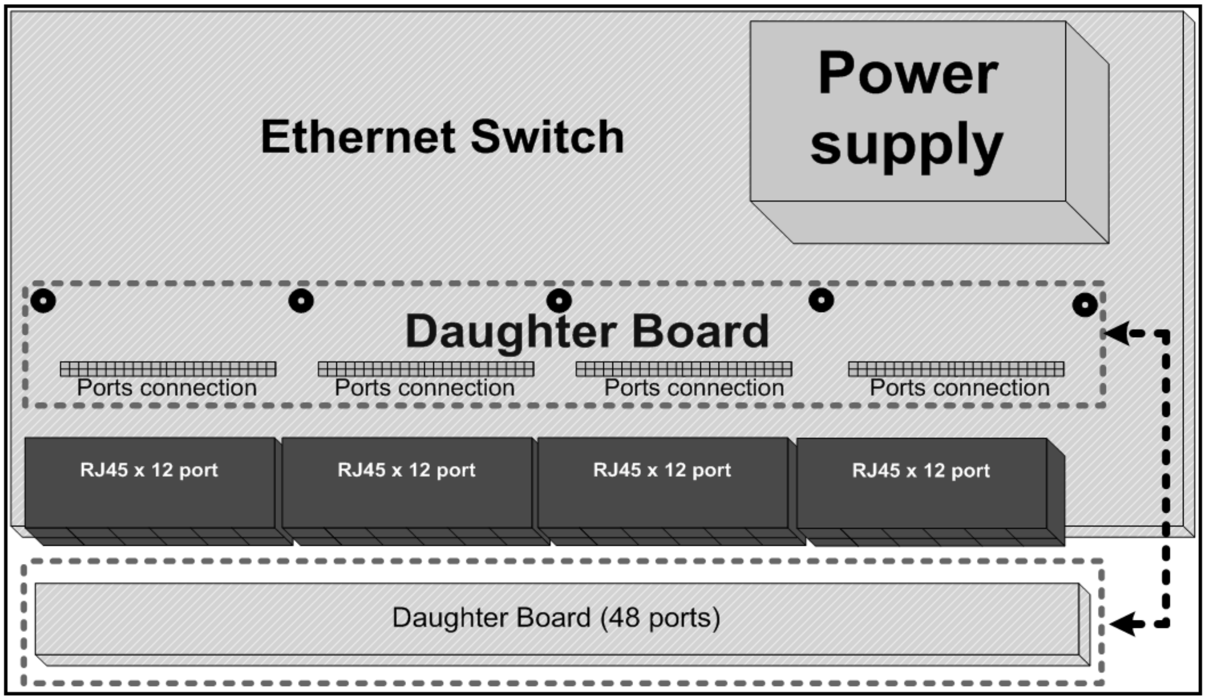


Figure 4-11. Ground and Power Planes

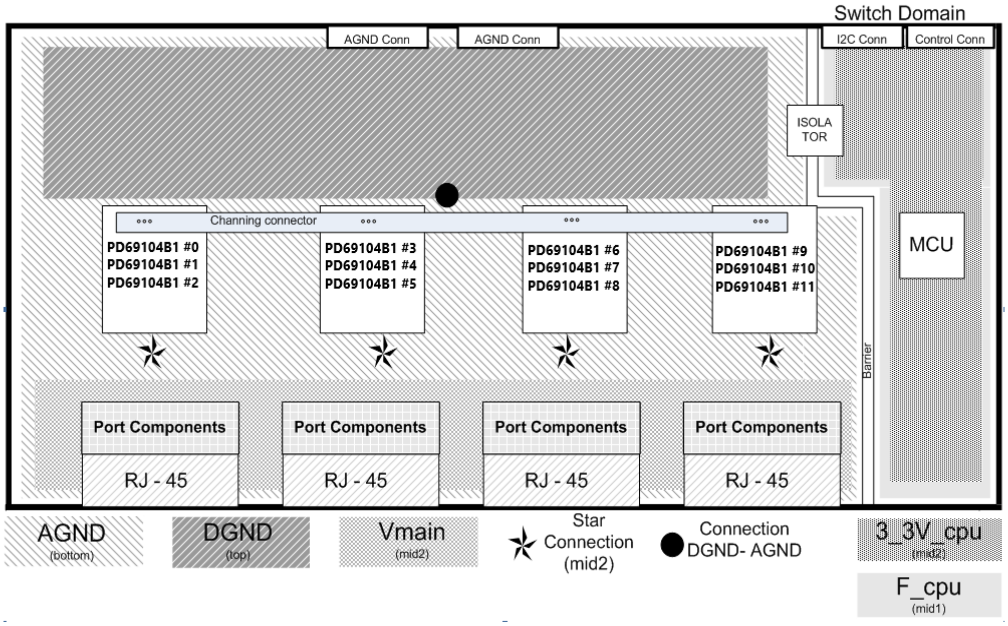


Figure 4-12. Star Point and Sense Resistors Design Criteria

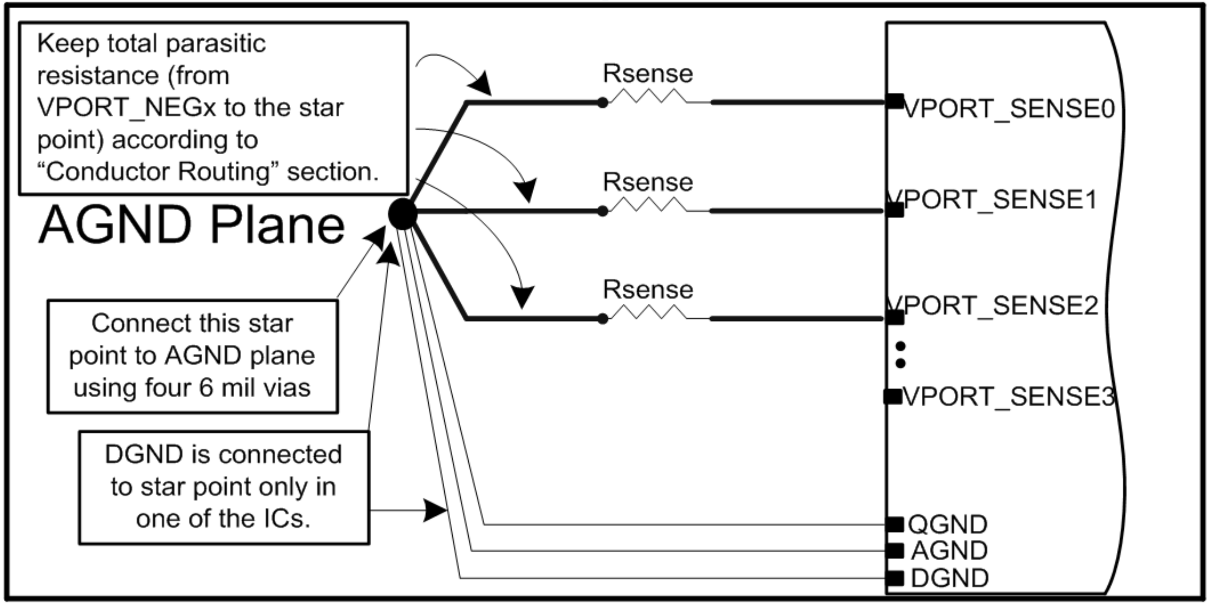


Figure 4-13. Overall Grounding Scheme

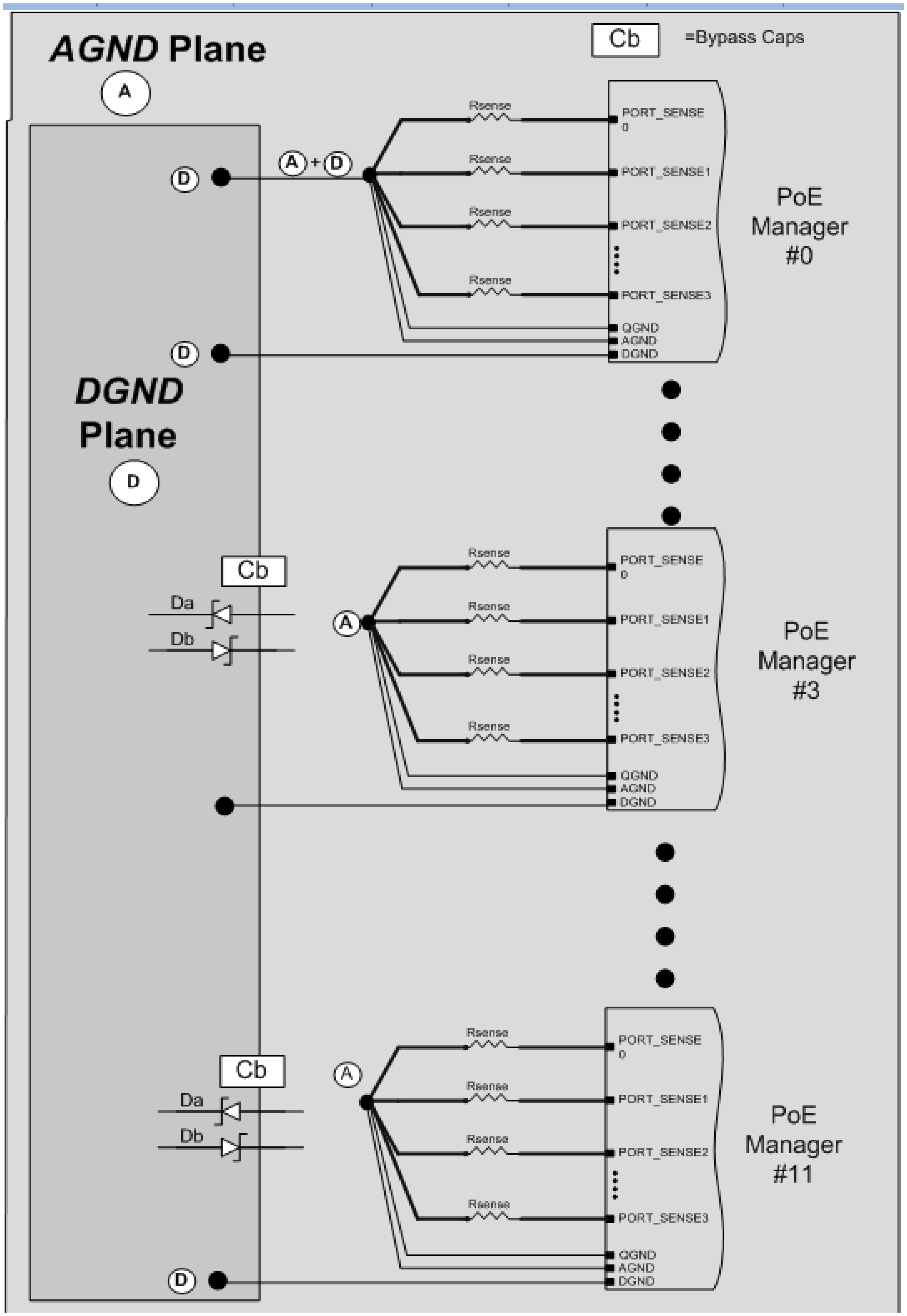
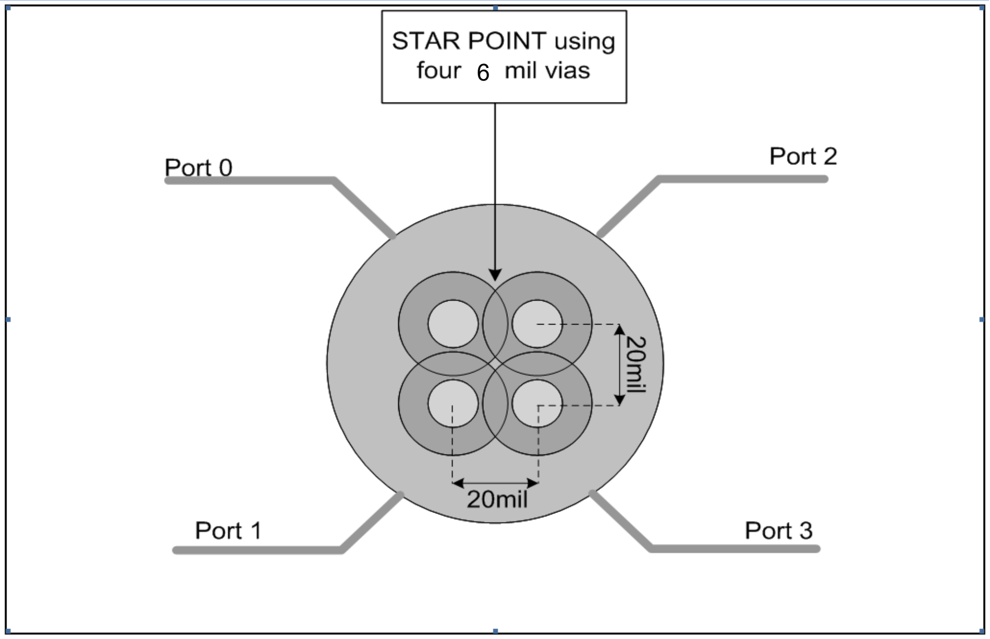


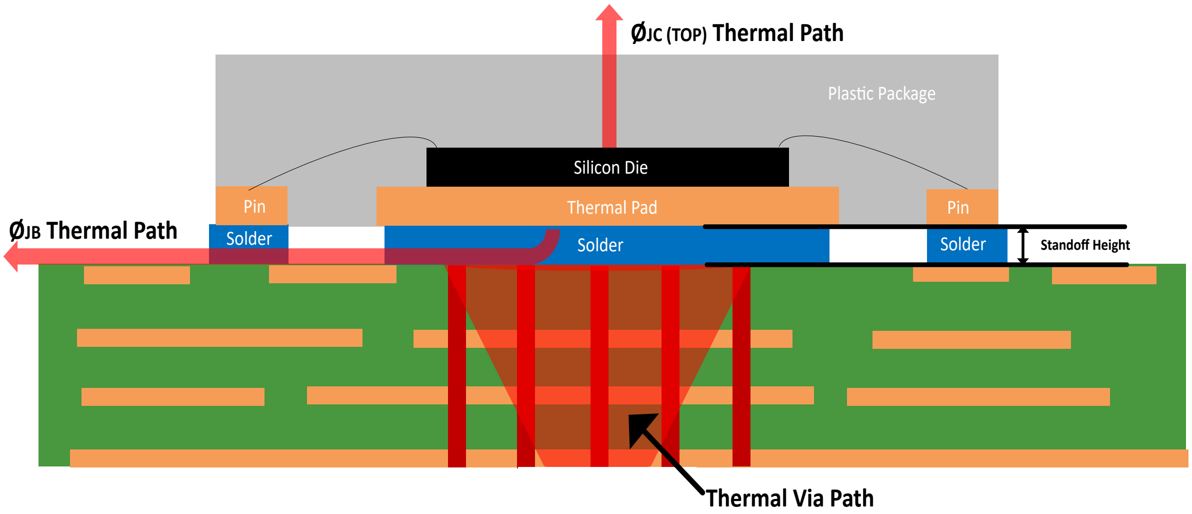
Figure 4-14. Star Point Layout



4.5 Thermal Design

For proper heat dissipation, follow the foot print or layout guidelines.

Figure 4-15. Heat Dissipation in PCB



The following lists the thermal paths for heat to flow from IC.

- Heat flow from the junction to the package side and pins. This parameter is a package parameter and it is defined by ØJB in the device data sheet.
- Heat flow from the junction to the package top surface. This parameter is a package parameter and is defined by ØJC (TOP) in the device data sheet.
- Heat flow from the junction to the package lower surface (the thermal pad) through the thermal vias to the various thermal ground planes. This is the significant thermal path. The thermal resistance of this path is determined by the package e-pad design and the PCB construction: number PCB layers, number of thermal vias, construction of thermal vias, size, and location of the copper thermal plane. This is the primary heat flow path and it is the main reason to follow the footprint recommendations.
- Per IPC7093 standard standoff must be minimum 2 mil (0.050 mm), with a Microchip recommended target of 2.5 mil (0.0635 mm). A paste mask stencil thickness of 5 mils must be considered.
- Thermal vias must be unplugged with a diameter approximately 0.33 mm. Microchip recommends a 3 x 4 via array and no solder paste covering on the lower PCB layer.
- Solder paste is a 2 x 2 array with streets between the array. Streets are important to allow outgassing during the reflow process to achieve uniform stand-off height.
- The PCB copper thermal planes must be of maximum practical area on PCB layers.

5. References

- *IEEE 802.3af—2003 standard, DTE Power via MDI*
- *IEEE 802.3at—2009 standard, DTE Power via MDI*
- *PD69104B1 datasheet*
- *AN3527 Compliance to Limited Power Source Requirements*

6. Revision History

Revision	Date	Description
A	09/2020	The following changes are made in this revision: • Updated the document as per Microchip standards. • The document number was changed from 06-0134-080 to DS00003648. • Application note number AN-198 was changed to AN3648. • Added NPN. • Revised IC part number. • Made structural changes. • Added PCB layout guidelines (see 4. PCB Layout).
1.4	01/2012	Added 1.2.11 4-Pair Description.
1.3	01/2012	Res_cap_int pin description with pull up was added.
1.2	01/2012	PG pins names were changed.
1.1	12/2011	Structural changes were made.
1.0	12/2011	Information and a table were added in 1.2 Detailed Circuit Description section.
0.2	10/2011	—
0.1	11/2010	This is the initial release of this document.

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