8 GHz Phase Frequency Detector IC with Dual 40 GHz Prescalers

PFD1K

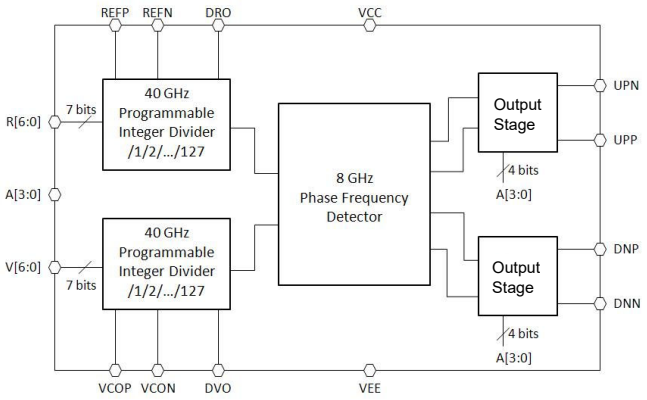
Product Overview

The PFD1K is a high-frequency, phase frequency detector (PFD) with fully differential inputs and outputs. It features dual 7-bit programmable high-speed prescalers which allow the PFD1K to operate up to 40 GHz for the reference- and voltage-controlled oscillator input frequency. The 8 GHz phase frequency detector allows operation at higher reference frequencies with concurrent lower phase noise and PLL figure of merit. The PFD1K operates with a single positive or negative 3.3V supply, and is packaged in a 40-pin, 6 mm × 6 mm Ceramic QFN package.

Key Features

- **40 GHz reference and VCO input frequencies**
- **7-bits Programmable 1 – 127 variable modulus prescalers**
- **DC–8 GHz phase frequency detector operation**
- **4-bits output voltage digital control with invert pin**
- **Single-ended or differential inputs and outputs**
- **6 mm × 6 mm 40-Leads Ceramic QFN**

Functional Block Diagram



Applications

The PFD1K can be used as a general purpose phase frequency detector (PFD) with integrated prescalers. It is ideally suited to phase locked loop (PLL) applications. The prescalers can be programmed at a rate greater than 100 MHz, which makes it an excellent choice for wideband and high speed fractional-N digital frequency synthesizers.

Phase Detector Characteristic (Divide Ratios: R = V = 1)

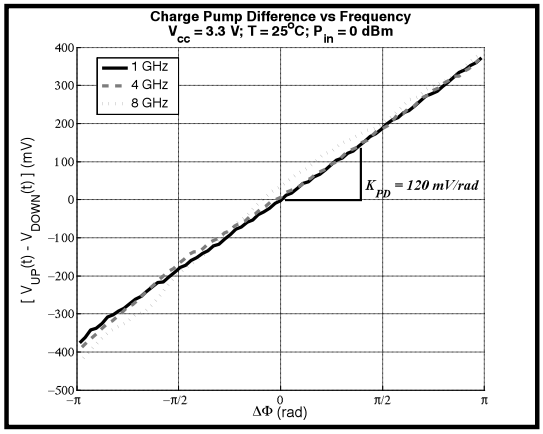


Table 1. Performance Overview

Parameter	Typ	Units
Input reference frequency	0.01 – 40	GHz
Input VCO frequency	0.01 – 40	GHz
Maximum comparison (PFD) frequency	8	GHz
SSB phase noise at 10 kHz offset	–153	dBc/Hz

Export Classification: EAR99

Table of Contents

1. Electrical Performances

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at +25 °C, –3.3V/130 mA and 50Ω Terminations (unless otherwise specified)

Parameter	Min	Typ	Max	Units
Input reference frequency **Note:** Minimum input	0.01		40	GHz
Input VCO frequency	0.01		40	GHz
Input reference power	– 10	0	+10	dBm
Input VCO power	– 10	0	+10	dBm
Differential output voltage		400		mVp-p
SSB phase noise at 10 kHz offset		–153		dBc/Hz
Supply voltage		–3.3		V
Supply current (divide-by-8)		130		mA

1.2 Typical Performance Curves

The following graphs show the typical performance curves of the device at +25 °C and + 3.3V (unless otherwise indicated).

1.2.1 Prescaler Characteristics

The following graphs show the typical performance curves of the device at +25 °C and + 3.3V, unless otherwise indicated.

Figure 1-1. Input Sensitivity vs. Temperature

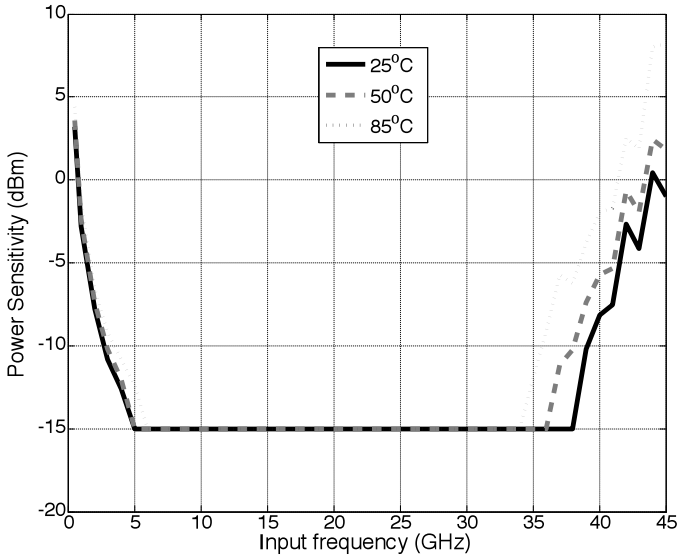


Figure 1-2. Input Sensitivity vs. Supply

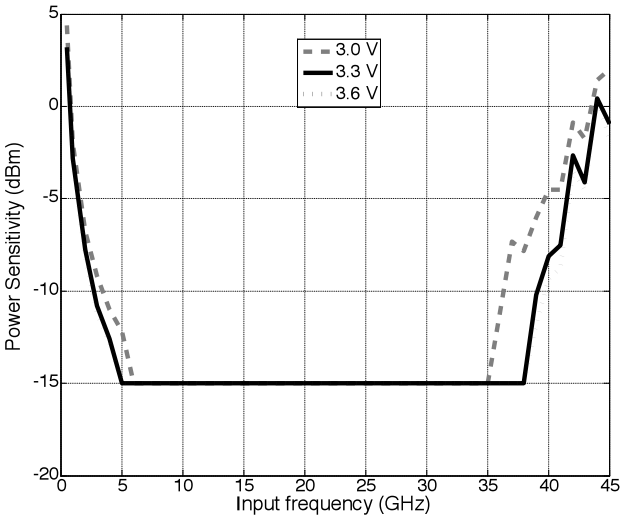


Figure 1-3. Diff. Output Voltage vs. Temp. (1 GHz & 0 dBm)

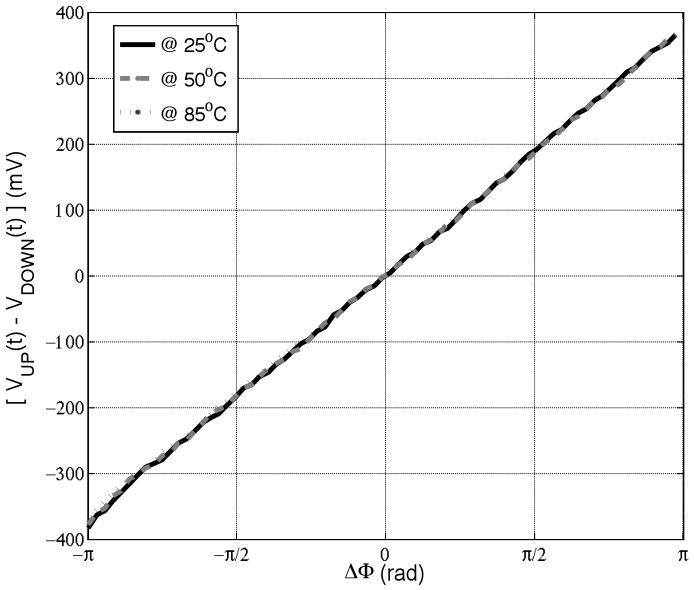


Figure 1-4. Diff. Output Voltage vs. Temp. (1 GHz & 0 dBm)

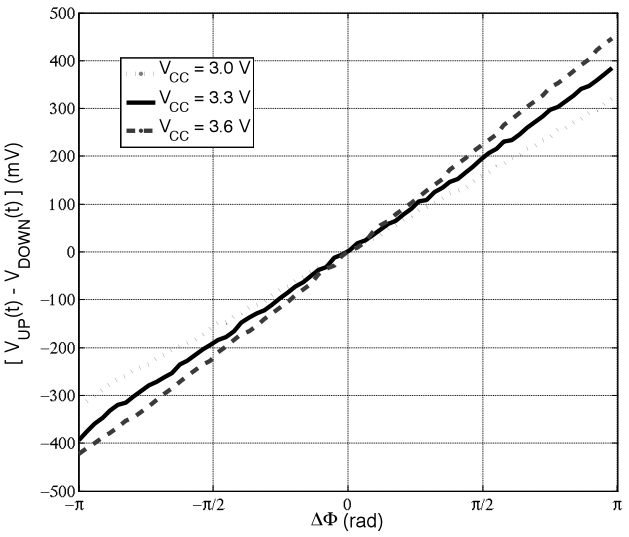


Figure 1-5. Binary Divide-by-4 Configuration at 20 GHz Input Freq. (150 mV/div)

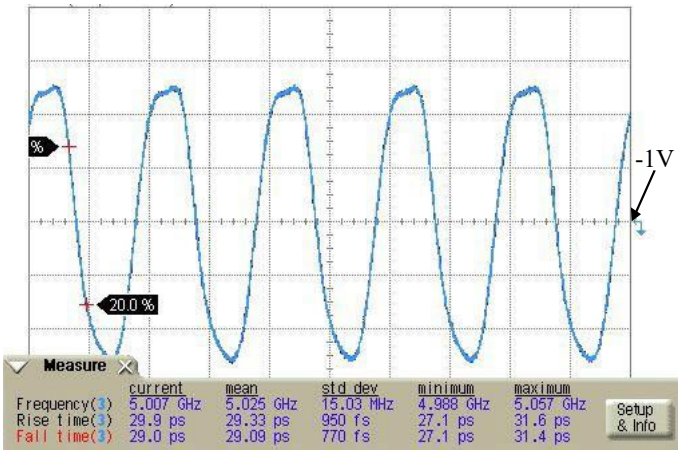
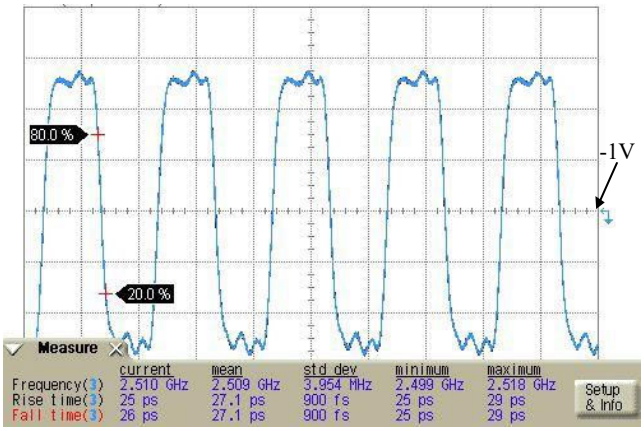


Figure 1-6. Binary Divide-by-8 Configuration at 20 GHz Input Freq. (150 mV/div)



1.2.2 PFD Characteristics

The following graphs show the typical performance curves of the Prescaler device at +25 °C and + 3.3V (Unless otherwise indicated).

Figure 1-7. Diff. Output Voltage vs. Frequency (0 dBm Pin)

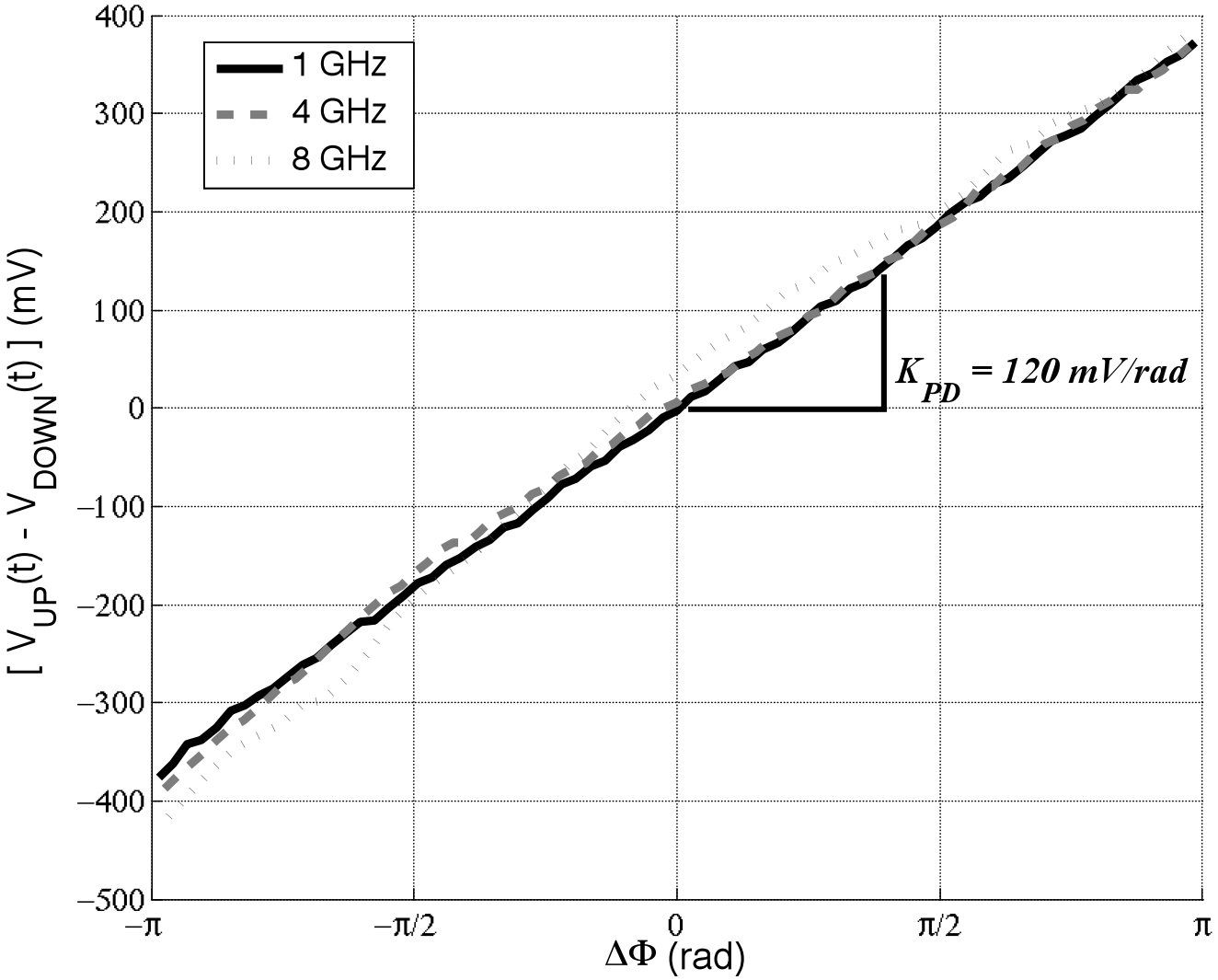


Figure 1-8. Diff. Output Voltage vs. Temp. (1 GHz & 0 dBm)

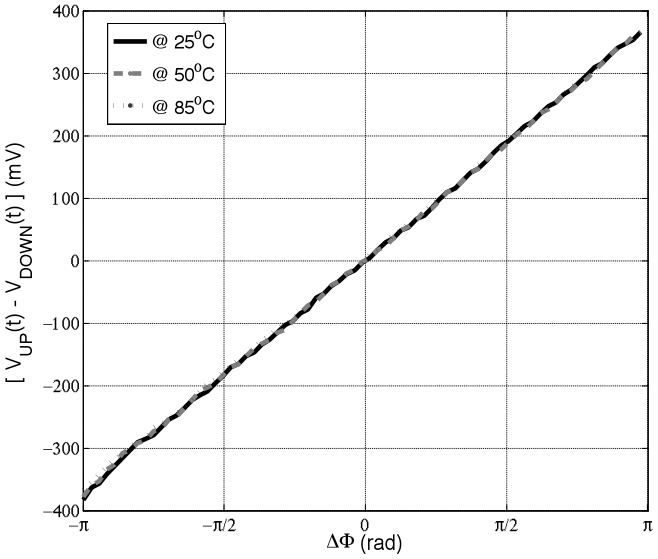


Figure 1-9. Diff. Output Voltage vs. Temp. (1 GHz & 0 dBm)

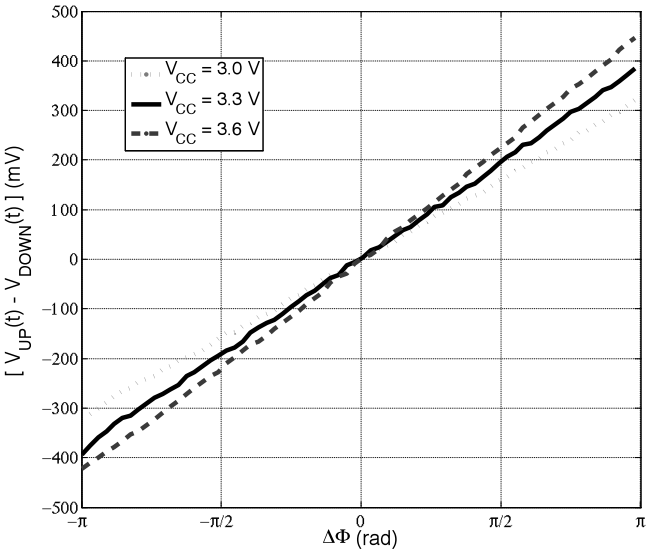


Figure 1-10. Diff. Output Voltage when REF leads VCO

fREF > fVCO; fREF = 5 GHz; VCC = 3.3 V; T = 25oC; Pin = 0 dBm; POL = open

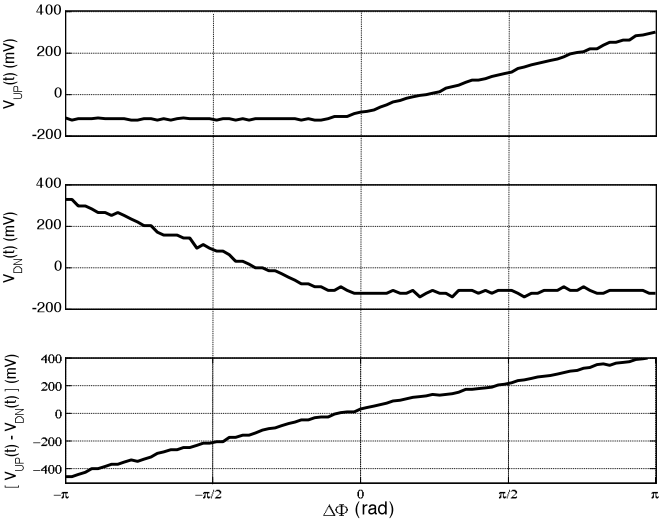
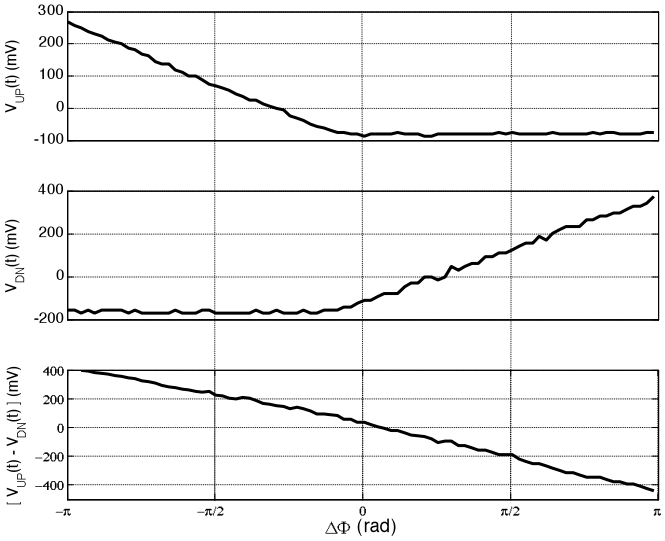


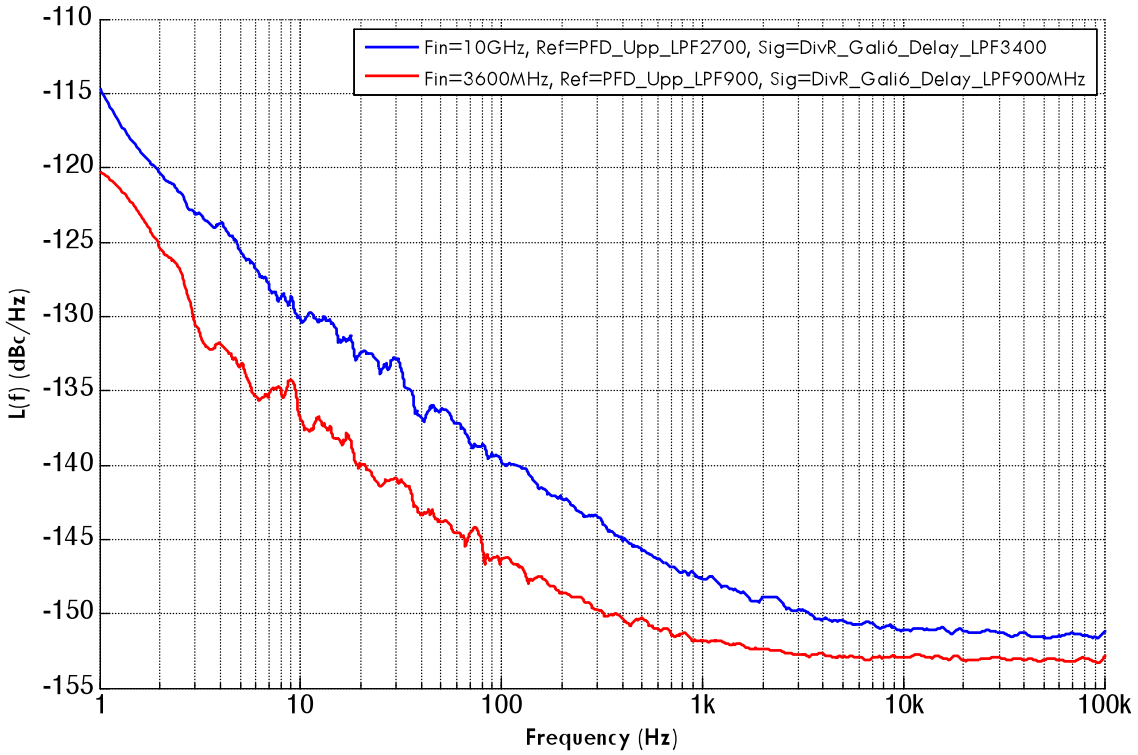
Figure 1-11. Diff. Output Voltage when REF laggs VCO

fVCO > fREF; fREF = 5 GHz; VCC = 3.3 V; T = 25oC; Pin = 0 dBm; POL = open



1.2.3 Phase Noise Characteristics

Figure 1-12. SSB Residual Phase Noise Performance: DivV = 4 & DivR = 4



1.3 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the PFD1K device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings could potentially cause damage or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Supply volgate (VCC – VEE)	4V
RF input power (INP, INN)	+ 10 dBm
Operating temperature	– 40 °C to + 85 °C
Junction temperature	+ 125 °C
Thermal resistance (junction to GND paddle)	20 °C/W
Storage temperature	–65 °C to +150 °C
ESD sensitivity (HBM)	Class 0
ESD sensitivity (CDM)	Class 0

ESD Sensitive Device

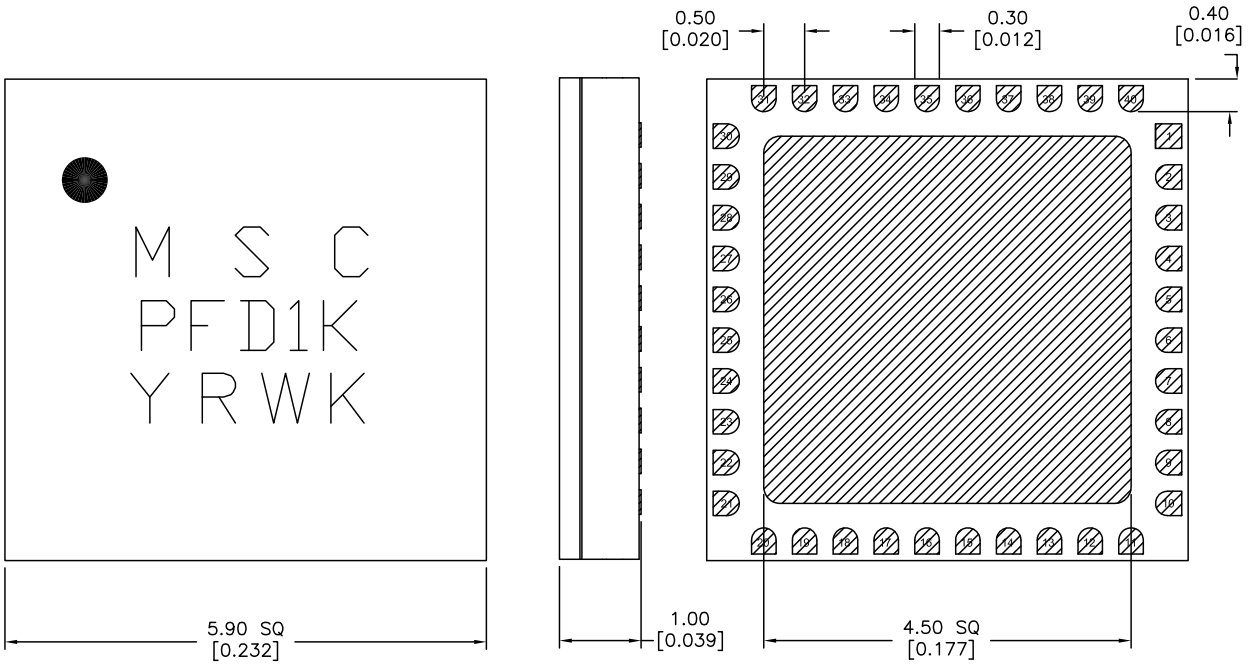
1.4 ESD Sensivity

Although SiGe ICs have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling. Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the low-frequency inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 100 V. For performance reasons, the RF inputs are not protected with ESD diodes and the ESD sensitivity is higher

2. Package Specifications

For additional packaging information, contact your Microchip sales representative.

Figure 2-1. Package Outline Drawing



6 mm × 6 mm, 40L Air Cavity Ceramic QFN Package

Table 2-1. Package Information

Parameter	Specification
Plating	Ni/Au
Package body material	Alumina

Table 2-2. I/O Pad Description

PIN Number	PIN Label	PIN Description	Notes
34 / 35	REFP / REFN	Prescaler differential REF inputs, positive/negative terminal	CML signal levels
17 / 16	VCOP / VCON	Prescaler differential VCO inputs, positive/negative terminal	CML signal levels
26 / 27	UPP / UPN	PFD differential UP output, postive/ negative terminal	CML output level set by output stage level
25 / 24	DNP / DNN	PFD differential DN output, postive/ negative terminal	CML output level set by output stage level
31	DRO	Single-ended divided REF output	CML output level, requires DC Pull-Up
20	DVO	Single-ended divided VCO output	CML output level, requires DC Pull-Up
36, 37, 38, 39, 1, & 2	R[6:0]	REF prescaler divide ratio	3.3V CMOS levels, defaults to logic 0 if open
15, 14, 13, 12, 11, 10 & 9	V[6:0]	VCO prescaler divide ratio	3.3V CMOS levels, defaults to logic 0 if open
4, 5, 6 & 7	A[3:0]	Diff. output voltage level control	3.3V CMOS levels, defaults to logic 0 if open

.....continued

PIN Number	PIN Label	PIN Description	Notes
3	VADJ	Diff. output voltage analog control	From VEE to VCC, VCC for max output
30	VADR	Divided REF output level control	From VEE to VCC, VCC for max output
21	VADV	Divided VCO output level control	From VEE to VCC, VCC for max output
8	POL	Polarity of phase detector	3.3V CMOS levels, defaults to logic 0 if open
32, 19, 23 & 28	VCC1, VCC2, VCC3 & VCC4	Positive power supply	+3.3V at 500 mA
33, 18, 22 & 29	VEE1, VEE2, VEE3 & VEE4	Negative power supply	Ground
PKG Backside		DC/RF ground	

3. Theory of operation

Overiew

The Programmable Prescaler divide the REF and VCO input frequencies to the PFD frequency (comparison frequency).

The REF input divide ratio R is determined as follows:

$$R = R_6^{2\hat{}6} + R_5^{2\hat{}5} + R_4^{2\hat{}4} + R_3^{2\hat{}3} + R_2^{2\hat{}2} + R_1^{2\hat{}1} + R_0^{2\hat{}0}$$

where R6 thru R0 have values of 0 or 1. (All bits set to 0 results in a divide ratio of 1.) Similarly, the divide ratio for the VCO input is set by V6 thru V0.

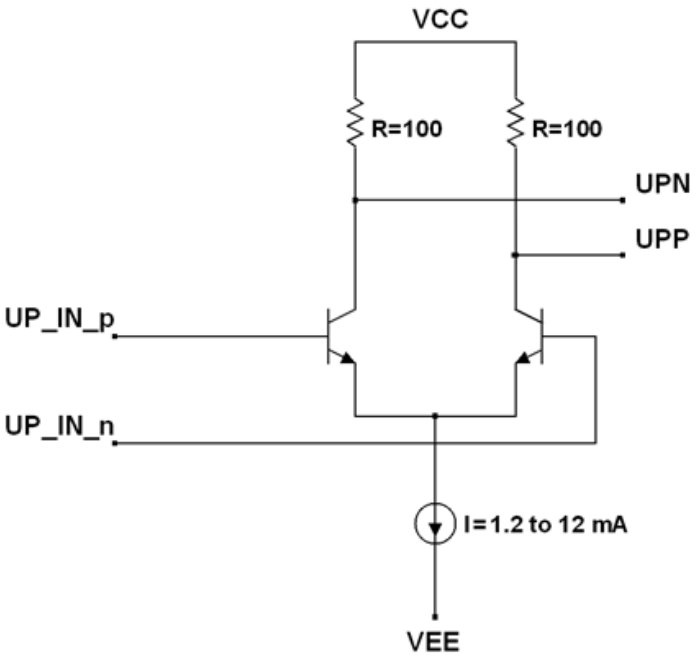
The core phase frequency detector can be operated up to a reference frequency of 8 GHz. The output of the phase frequency detector drives two programmable output buffers. The amplitudes of the up and down pulses can be controlled digitally by setting A[3:0]. There is also an analog adjustment at the VADJ* pin.

The divided reference and VCO signals may be monitored at the DRO and DVO outputs respectively. Analog adjustments, VADV* and VADR*, can be used to control the amplitudes of DVO and DRO, or to disable DVO and DRO in order to reduce power consumption. With the exception of DRO and DVO, all of the RF inputs and outputs of the Prescaler are fully differential CML-compatible levels so that they are easy to interface with other logic.

Output Voltage Control

The Programmable Prescaler outputs are differential CML outputs with 100Ω terminations. With this design, the up and down pulse width can be as small as 100 ps. The output pulses are digitally programmable with a 4-bit parallel interface. The maximum output current is 12 mA, which will produce a pulse of 1200 mVpp into the internal 100Ω termination resistor. When the output is terminated with a 50Ω load, the parallel impedance of 100Ω and 50Ω results in a 33Ω load, which reduces the output to 400 mVpp. In addition to the digital control, there is an analog output level control voltage, VADJ, which can be used for fine control of the output current. The maximum output current of 12 mA occurs when VADJ is set to VCC (which is the normal mode of operation). Logic 1 on the POL control input reverses the polarity of the PFD outputs.

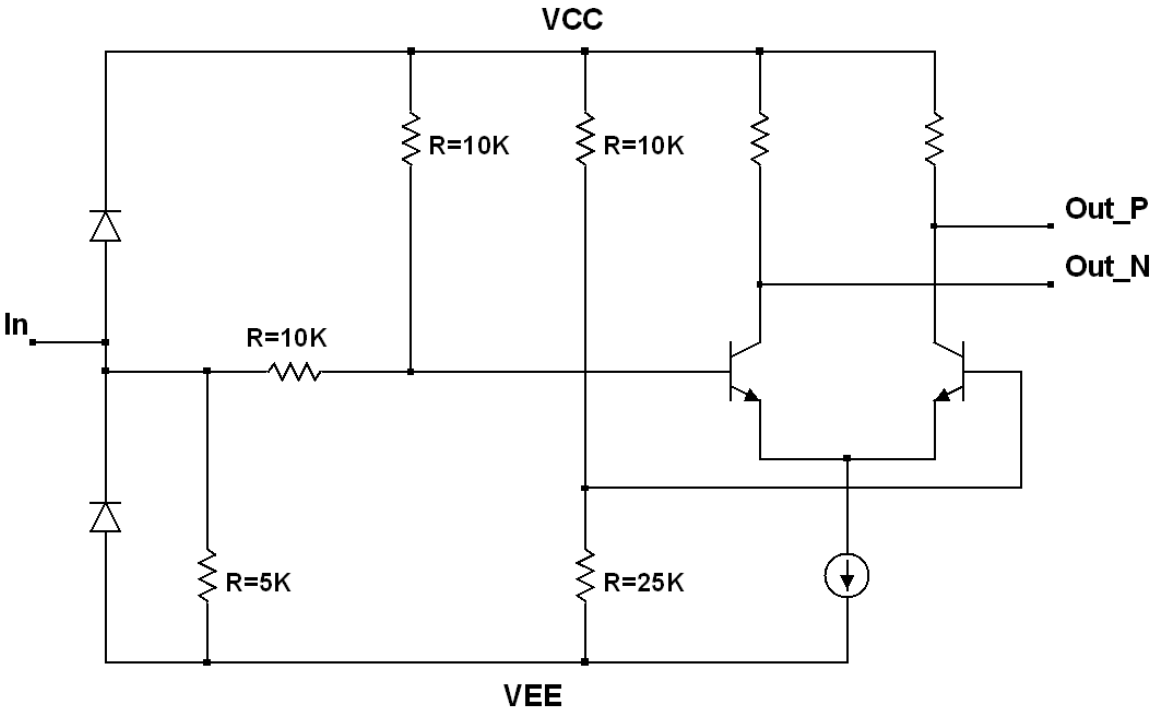
Figure 3-1. Simplified Output Circuit



Control Logic Circuitry

The same circuitry is used for all control lines: A[0:3], R[0:6], V[0:6] and POL. A control pin left open defaults to logic 0.

Figure 3-2. Simplified Control Logic Input



Analog Amplitude Controls

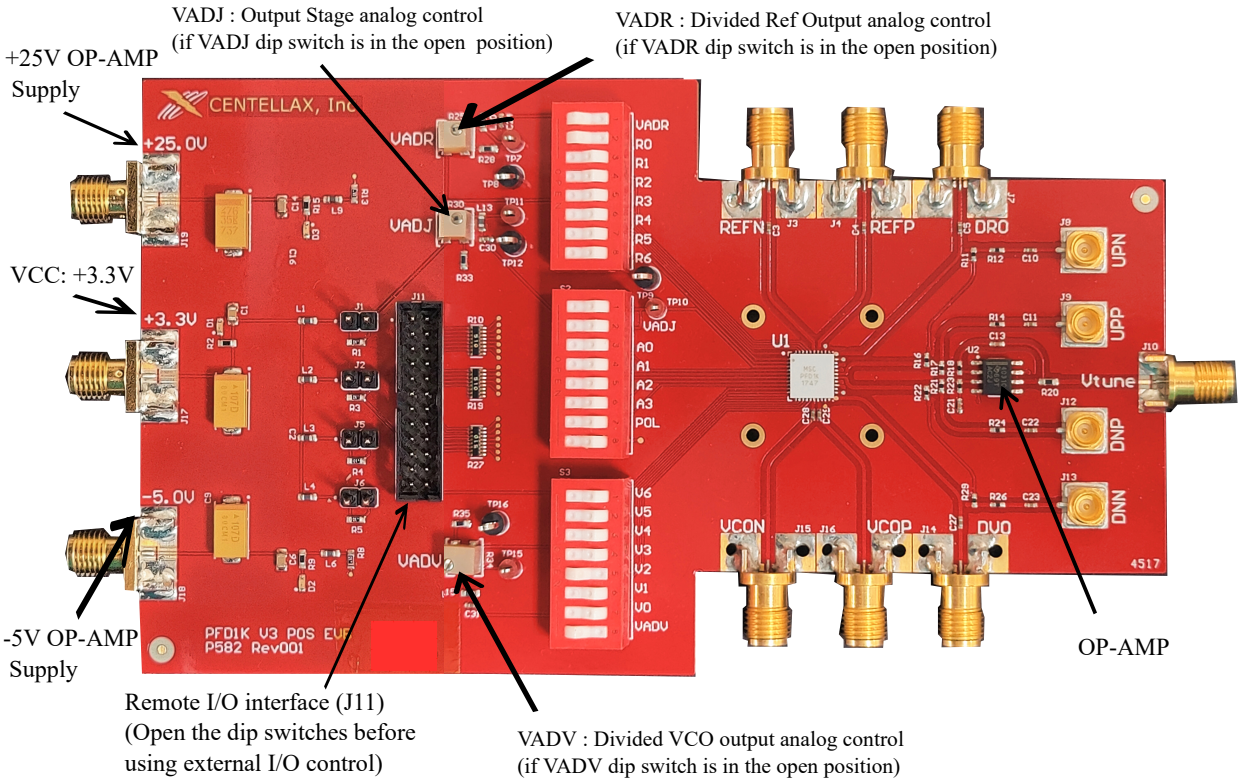
VADJ can be used for fine tuning the output current. Maximum current is achieved by setting VADJ to VCC. Similarly, the amplitudes of the prescaler outputs at DRO and DVO can be controlled with analog voltages VADR and VADV, respectively. As with VADJ, setting VADR and VADV to VCC results in maximum output amplitude.

Table 3-1. Control Voltage (LVTTL Compatible)

Logic Level	Minimum	Typical	Maximum
1 (high)	VCC – 1.3V	VCC	VCC
0 (low)	VEE	VEE	VEE + 0.8V

4. Evaluation PCB

Figure 4-1. MMFEB21PP6/PFD1K Evaluation PCB



⚠ CAUTION VCC supply voltage must be positive. The +3.3V must be turned on first before applying the +25V and –5V supply. **If not turned on, it will damage the phase detector**

Figure 4-2. Eval PCB DIP Switch

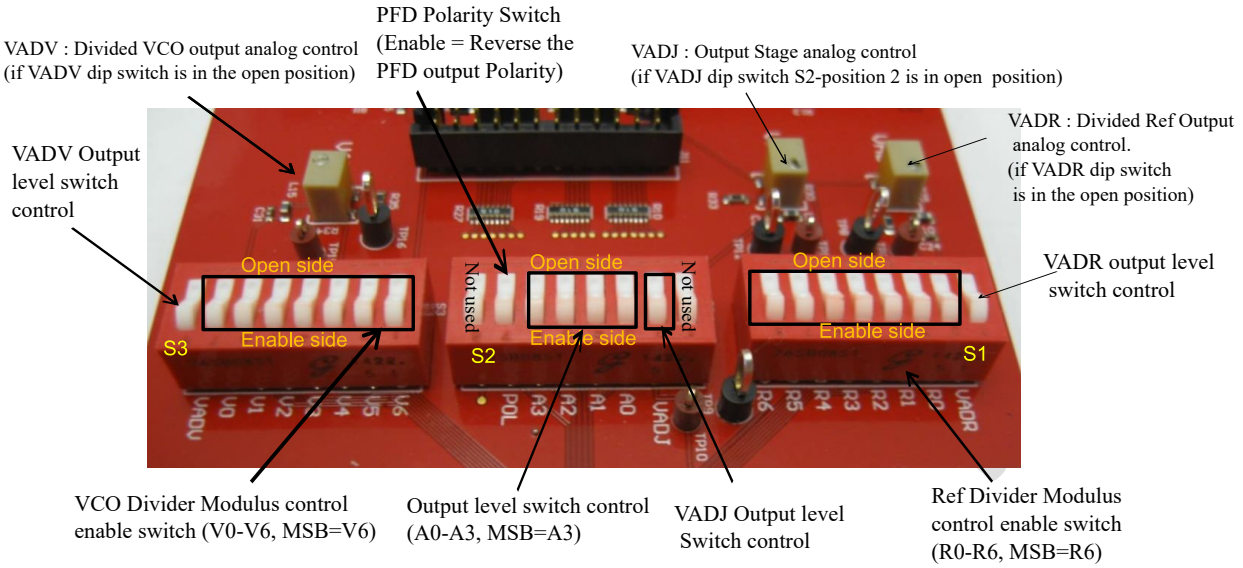
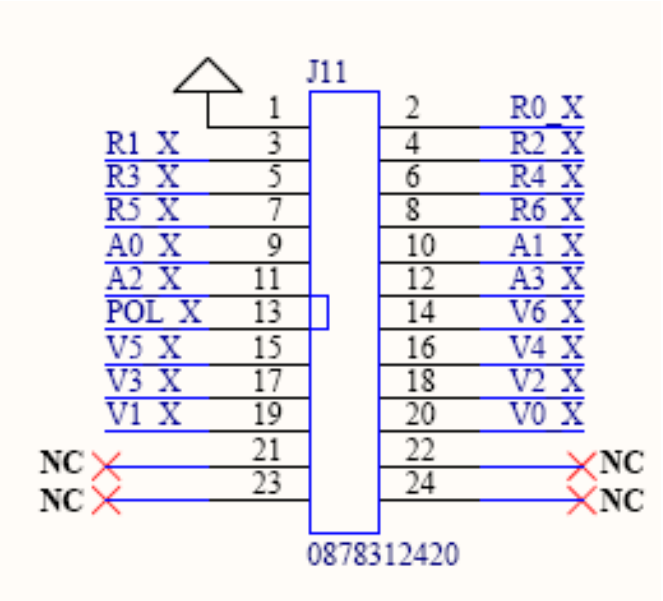


Figure 4-3. Remote I/O pin configuration (J11)



Turn On Sequence

Attention: Please take caution of static damage as the evaluation board and the phase detector device are both sensitive to static discharge.

1. If RF inputs/outputs are used in single-ended configuration, terminate unused inputs/outputs with 50Ω loads.
2. Apply a +3.3V supply (VCC) to the evaluation board (J17, SMA (f) connector) for the divider/phase detector.

⚠ CAUTION **Warning: In order to avoid damaging the device, +3.3V supply must be turned on before turning on the op-amp bias voltages (+25V and –5V).**

3. Apply a +25V supply to the evaluation board (J19, SMA (f) connector) for the op-amp.
4. Apply a –5V supply to the evaluation board (J18, SMA (f) connector) for the op-amp.
5. Use on-board dip switches to adjust the Reference and VCO divide ratios.
   Note: All zeros is a default divide by 1.

Switch Settings (Open = 0, Close = 1)		Division Ratio Output
VCO (S3) V6 V5 V4 V3 V2 V1 V0 (V6=MSB)	REF (S1) R6 R5 R4 R3 R2 R1 R0 (R6=MSB)	
0000001	0000001	1
1000000	1000000	1/64
1111111	1111111	1/127

6. Apply RF signals at the inputs (REFP/REFN and VCOP/VCON, 2.9 mm (f) connectors).
7. Set the dip switches VADV (part of S3, VCO) and VADR (part of S1, REF) to the disable (open) position. Adjust the VADV potentiometer to control the desired VCO divider's output amplitude and adjust the VADR potentiometer to control the desired REF divider's output amplitude. The divided RF output signals can be viewed at the DRO port (REF) and at the DVO port (VCO) using a spectrum analyzer or oscilloscope. Those connectors are 2.9 mm (f).
8. For maximum output swing on the prescalers, set the dip switches VADV and VADR to the close position (i.e., set the VADV and VADR voltage levels to the same voltage as VCC). Note that while in logic 1 on the dip switch of VADV and VADR, the VADV and VADR potentiometers will have no effect on the prescalers' output swing voltage.
9. The output stage has a digital adjustment which scales the current. For example, if VADJ is ON (S2 dip switch's position 2 is set to CLOSE/ON) and A0 to A3 (S2) are all set to ON (i.e., logic 1), then the maximum current will be 12 mA. The A3-A0 switch of S2 settings allows the value to be adjusted as follows:

Switch Settings (S2, Open = 0, Close = 1) A3 A2 A1 A0 (A3=MSB)	Output Stage Current
0000	0 mA
0001	0.75 mA
0010	1.5 mA
....	....
1111	12 mA

10. Or to control the output of the level manually using the VADJ potentiometer, then settle VADJ dip switch's (S2) position 2 to OPEN and then use the VADJ potentiometer to adjust the desired output current swing.
11. The POL dip switch (S2) - position 7 (see Figure 3), allows the polarity of the PFD to be reversed. This is useful to unlock the loop momentarily.
12. The PFD output can be viewed at UPP/UPN and DWP/DWN connectors (SMP plug (m)) using a spectrum analyzer or oscilloscope. 8 GHz is the maximum frequency output. See 5. Application Note section for additional info.
13. Optional: The divide ratio of the prescaler and the output current of the phase frequency detector can also be programmed through (J11), (a 24-pin Molex connector interface,mfg pn 87831-2420), using an external programming device, see Figure 2. If using an external programming device, set the on-board dip switches (S1: R0-R6, S2: A0-A3 and POL, and S3:V0-V6) to the **open position first** before making connection to the external programming device.

Note: Do not use both on-board divider modulus control/output level control (Dip Switches) and the external I/O interfaces (J11) at the same time.

Input voltage levels for I/O control lines:

Logic Level	Minimum	Typical	Maximum
1 (high)	VCC-1.3V	VCC	VCC
0 (low)	VEE	VEE	VEE + 0.8V

14. The evaluation board also included an integrator (op-amp circuitry, if the option is loaded), which generates a Vtune error voltage output signal at the Vtune port (2.9 mm (f) connector). This signal can be viewed using a spectrum analyzer or oscilloscope. See 5. Application Note section for additional information.
    This error voltage represented the phase frequency difference between the REF and VCO input signals (~10 MHz signal, the average of this signal is the VCO's DC error correction voltage).
15. Refer to MMFEB21PP6 and PFD1K datasheets for performance specifications.

5. Application Note

1. All of the controls on the evaluation board are brought out to a Molex test connector (J11) for programmability. A 0V to +3.3V TTL signal can be used to override the dip switches (except for the VADV, VADR, and VADJ switches). Set those dip switch positions to **OFF**and apply a+3.3V TTL signal (i.e., a logic “High” level) to the test header.
2. The evaluation board has an OP AMP to drive a Varactor VCO oscillator with a 0V-to-20V tuning voltage (see Figure 4). Make sure that the proper NO-LOAD resistors are installed to enable the OP AMP circuitry (refer to the schematic in Figure 5) and make sure that a –5VEE and+25VCC supply are connected. The –5V and +25V supplies are not needed if the OP AMP integrator circuitry is not needed.

   If evaluating the PFD output circuit (i.e., UPN/UPP and DNP/DNN outputs), make sureR12, R14, R24 and R26 (0Ω) resistors are loaded. Also remove R17 and R21 (200Ω) resistors. If not, those two resistors (R17 and R21) will load down the phase detector output circuit. However, it is okay to leave them in place during the evaluation if the output level is not a concern.

   If using the Vtune (op-amp) output (J10) for evaluation, terminate the UPN/UPP and DNP/DNN output ports with 50Ω load to minimize reflection. This action will also lower the output amplitude signal level by a small amount.
3. Figure 4 shows a block diagram of the MMFEB21PP6/PFD1K phase frequency detector and the VCO errorvoltage integrator circuit (if loaded) that is part of the evaluation board.
4. A schematic of the evaluation board is included on the next page ().

Figure 5-1. Block Diagram for MMFEB21PP6/PFD1K Eval PCB Including Loop Filter and VCO Op-Amp

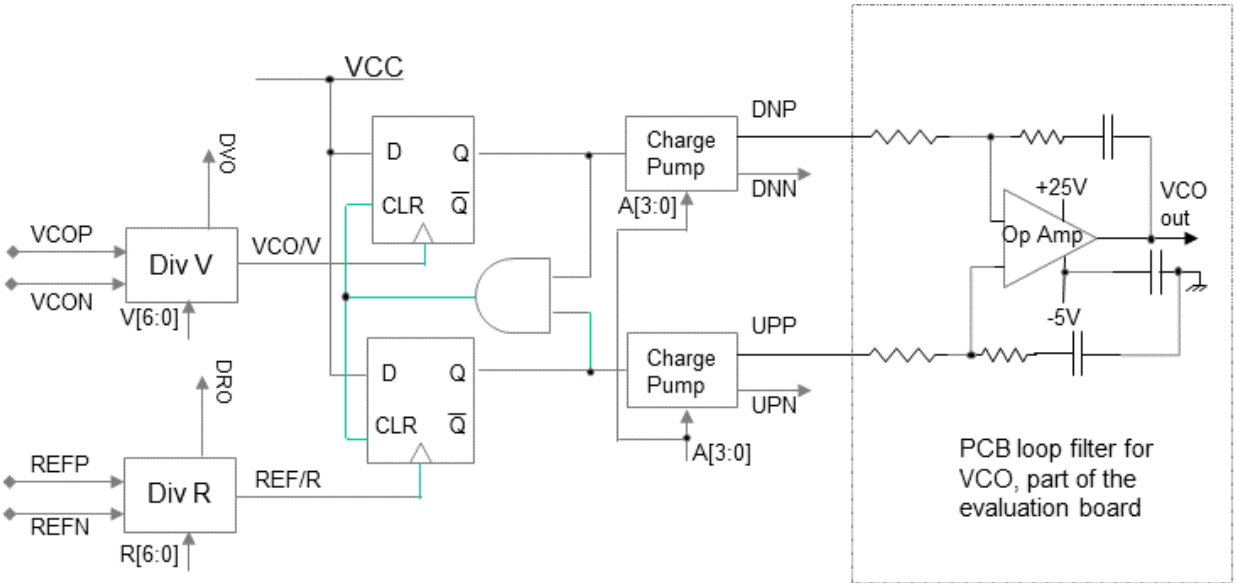
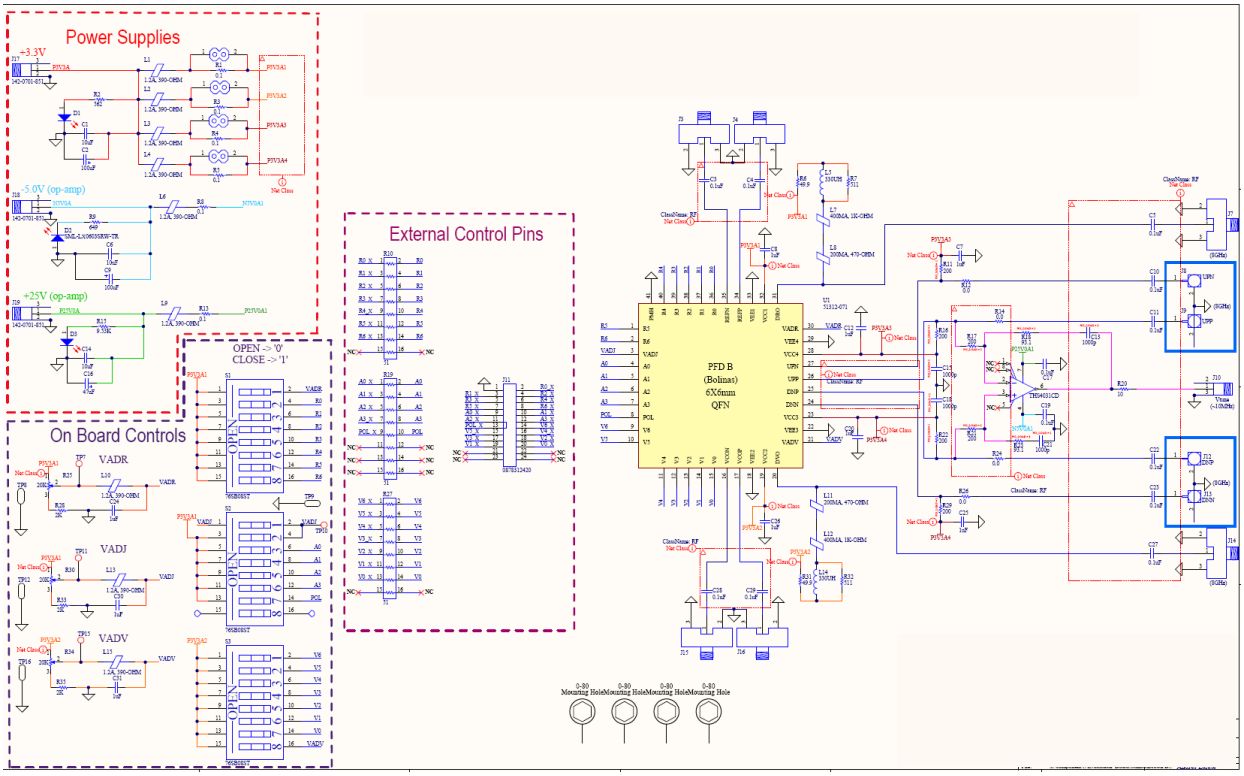


Figure 5-2. Schematic of the MMFEB21PP6/PFD1K Eval PCB



6. Ordering, Shipping, and Handling

6.1 Handling Recommendations

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by Static Electricity. It is recommended to follow all procedures and guidelines outlined in Datasheet.

6.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package	Note
PFD1K	6 mm × 6 mm, 40L Air Cavity Ceramic QFN	NiAu Plating Finish
PFD1K-Sn63	6 mm × 6 mm, 40L Air Cavity Ceramic QFN	Sn63Pb27 Plating Finish (Gold Removal by J-STD-001)
PFD1KE	PFD1K Eval PCB	

6.3 Packing Information

Part Number	Description
PFD1K/TR	Tape and Reel

Note: Contact your Microchip sales representative for the minimum quantity order

7. Revision History

Table 7-1. Revision History

Revision	Date	Description
B	06/2023	Document migrated from Microsemi template to Microchip template. .
Initial release (Microsemi Revision A)	**SMD-00191 Rev D**	Document created

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ISBN:

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office	**Australia - Sydney**	**India - Bangalore**	**Austria - Wels**
2355 West Chandler Blvd.	Tel: 61-2-9868-6733	Tel: 91-80-3090-4444	Tel: 43-7242-2244-39
Chandler, AZ 85224-6199	**China - Beijing**	**India - New Delhi**	Fax: 43-7242-2244-393
Tel: 480-792-7200	Tel: 86-10-8569-7000	Tel: 91-11-4160-8631	**Denmark - Copenhagen**
Fax: 480-792-7277	**China - Chengdu**	**India - Pune**	Tel: 45-4485-5910
Technical Support:	Tel: 86-28-8665-5511	Tel: 91-20-4121-0141	Fax: 45-4485-2829
www.microchip.com/support	**China - Chongqing**	**Japan - Osaka**	**Finland - Espoo**
Web Address:	Tel: 86-23-8980-9588	Tel: 81-6-6152-7160	Tel: 358-9-4520-820
www.microchip.com	**China - Dongguan**	**Japan - Tokyo**	**France - Paris**
Atlanta	Tel: 86-769-8702-9880	Tel: 81-3-6880- 3770	Tel: 33-1-69-53-63-20
Duluth, GA	**China - Guangzhou**	**Korea - Daegu**	Fax: 33-1-69-30-90-79
Tel: 678-957-9614	Tel: 86-20-8755-8029	Tel: 82-53-744-4301	**Germany - Garching**
Fax: 678-957-1455	**China - Hangzhou**	**Korea - Seoul**	Tel: 49-8931-9700
Austin, TX	Tel: 86-571-8792-8115	Tel: 82-2-554-7200	**Germany - Haan**
Tel: 512-257-3370	**China - Hong Kong SAR**	**Malaysia - Kuala Lumpur**	Tel: 49-2129-3766400
Boston	Tel: 852-2943-5100	Tel: 60-3-7651-7906	**Germany - Heilbronn**
Westborough, MA	**China - Nanjing**	**Malaysia - Penang**	Tel: 49-7131-72400
Tel: 774-760-0087	Tel: 86-25-8473-2460	Tel: 60-4-227-8870	**Germany - Karlsruhe**
Fax: 774-760-0088	**China - Qingdao**	**Philippines - Manila**	Tel: 49-721-625370
Chicago	Tel: 86-532-8502-7355	Tel: 63-2-634-9065	**Germany - Munich**
Itasca, IL	**China - Shanghai**	**Singapore**	Tel: 49-89-627-144-0
Tel: 630-285-0071	Tel: 86-21-3326-8000	Tel: 65-6334-8870	Fax: 49-89-627-144-44
Fax: 630-285-0075	**China - Shenyang**	**Taiwan - Hsin Chu**	**Germany - Rosenheim**
Dallas	Tel: 86-24-2334-2829	Tel: 886-3-577-8366	Tel: 49-8031-354-560
Addison, TX	**China - Shenzhen**	**Taiwan - Kaohsiung**	**Israel - Ra'anana**
Tel: 972-818-7423	Tel: 86-755-8864-2200	Tel: 886-7-213-7830	Tel: 972-9-744-7705
Fax: 972-818-2924	**China - Suzhou**	**Taiwan - Taipei**	**Italy - Milan**
Detroit	Tel: 86-186-6233-1526	Tel: 886-2-2508-8600	Tel: 39-0331-742611
Novi, MI	**China - Wuhan**	**Thailand - Bangkok**	Fax: 39-0331-466781
Tel: 248-848-4000	Tel: 86-27-5980-5300	Tel: 66-2-694-1351	**Italy - Padova**
Houston, TX	**China - Xian**	**Vietnam - Ho Chi Minh**	Tel: 39-049-7625286
Tel: 281-894-5983	Tel: 86-29-8833-7252	Tel: 84-28-5448-2100	**Netherlands - Drunen**
Indianapolis	**China - Xiamen**		Tel: 31-416-690399
Noblesville, IN	Tel: 86-592-2388138		Fax: 31-416-690340
Tel: 317-773-8323	**China - Zhuhai**		**Norway - Trondheim**
Fax: 317-773-5453	Tel: 86-756-3210040		Tel: 47-72884388
Tel: 317-536-2380			**Poland - Warsaw**
Los Angeles			Tel: 48-22-3325737
Mission Viejo, CA			**Romania - Bucharest**
Tel: 949-462-9523			Tel: 40-21-407-87-50
Fax: 949-462-9608			**Spain - Madrid**
Tel: 951-273-7800			Tel: 34-91-708-08-90
Raleigh, NC			Fax: 34-91-708-08-91
Tel: 919-844-7510			**Sweden - Gothenberg**
New York, NY			Tel: 46-31-704-60-40
Tel: 631-435-6000			**Sweden - Stockholm**
San Jose, CA			Tel: 46-8-5090-4654
Tel: 408-735-9110			**UK - Wokingham**
Tel: 408-436-4270			Tel: 44-118-921-5800
Canada - Toronto			Fax: 44-118-921-5820
Tel: 905-695-1980			
Fax: 905-695-2078			