VSC8502
User Guide
VSC8502 Reference Board

May 2014

Microsemi
a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 of this datasheet was published in May 2014. This was the first publication of the document.

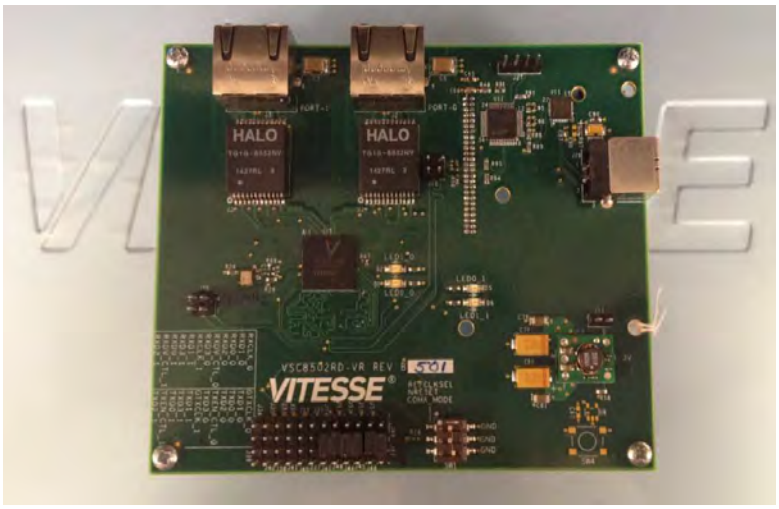
2 Introduction

The VSC8502 device is a low-power, cost-optimized, dual-port Gigabit Ethernet PHY. It features integrated, line-side termination to conserve board space, lower EMI, and improved system performance. To further reduce system complexity, component count, and system cost, the VSC8502 device can operate from a single 3.3 V supply using integrated voltage regulators. Additionally, integrated RGMII timing compensation eliminates the need for on-board delay lines. The device also optimizes power consumption in all link operating speeds and features Wake-on-LAN (WOL) power management using magic packets. This document describes the architecture and usage of the VSC8502RD and VSC8502RD-VR Reference Design Boards. The Quick Start section describes how to install and run the graphical user interface (GUI) to fully control the evaluation board.

Figure 1 • VSC8502RD Reference Board E

The following illustration shows the 501 VSC8502 Reference Board.

Figure 2 • VSC8514 Evaluation Board (Bottom View)



Additional VSC8502 collateral for both the VSC8502 device and VSC8502 reference design, including schematics, layout, GUI, and application notes can be found on the VSC8502 product web page at: www.vitesse.com/products/product/VSC8502.

3 General Description

The evaluation board, shown in Figure 1, provides the user a way to evaluate the VSC8502 device in multiple configurations. Two RJ-45 connectors are provided for copper media interfaces. The MAC interface (RGMII) is exposed via 0.1 inch steakheaders, J31 - J53. For standalone access to all of the features of the device, an external microcontroller is used to configure the VSC8502 via the MDIO bus. The GUI enables the user to read and write device registers.

3.1 Copper Port RJ45 Connections

PHY ports 0 and 1 use generic RJ45 connectors with discrete Halo TG1G-S032NYRL magnetics.

3.2 RGMII MAC Connectors

The parallel MAC interface is available through 0.1 inch headers. The layout is such that by installing jumpers the RX and TX signals can be looped on board. When mating to a MAC board, a specialized cable will need to be constructed.

The following is the RGMII connectors positioned in the board:

Table 1 • RGMII Connector Positions

Channel 1						Channel 0					
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GN
RXD2	RXDV_CTL	RXD0	RXD3	RXD1	RXCLK	RXD3	RXDV_CTL	RXD2	RXD0	RXD1	RX
TXD2	TXDV_CTL	TXD0	TXD3	TXD1	TXCLK	TXD3	TXDV_CTL	TXD2	TXD0	TXD1	TX
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GN

3.3 Static Controls (SW1)

Three static control signals are set by the DIP switch SW1.

Signal Name	Description	Position for Normal Operation
REFCLK_SEL	Select the input frequency to the device. 0: 125 MHz 1: 25 MHz	1
NRESET	Hold the device in rest. 0: Reset state 1: Normal device operation	1
COMA_MODE	Hold the device in coma state. 0: Disabled 1: Enabled	0

3.4 Clocking

VSC8502RD board is equipped with a 2.5V CMOS, 25.00 MHz standard clock oscillator (U5), while the VSC8502RD-VR board uses a 3.3 V CMOS version.

3.5 Software Interface Microcontroller Card

A Silabs F340 microcontroller is included to facilitate a software interface to the registers on the VSC8502 through a USB port.

Note: Alternatively, a Rabbit card is available for an IP-based manager of the PHY register space, installed in the keep-out area (U6) of the board's top-side. Or, MDC and MDIO can be accessed on stake header J10 if desired for another microcontroller to host the PHY register space.

3.6 Software Interface Microcontroller Card

The VSC8502RD or VSC8502RD-VR is powered by plugging in a USB cable to the board and to a PC. For the VSC8502RD board, there are three on-board regulators that will convert the 5 V supplied by the PC to 1.0 V and 2.5 V for the VSC8502 and 3.3 V for other devices. For the VSC8502RD-VR board, there is only one on-board regulator that will convert the 5 V supplied by the PC to 3.3 V for the VSC8502's internal voltage regulators, VSC8502's 3.3 V digital supplies, as well as other devices. A board will draw less than 350 mA from the USB port.

4 Quick Start

This section shows the quick start for the VSC8502 Reference Board.

4.1 Connecting the Power Supply

The reference design board is powered by the USB cable. The on-board switcher(s) converts the +5V USB power to the required power supplies for devices on the board. Please see section 2.6 for reference.

Note: For proper device operation, prior to powering the board, ensure the NRESET input to the VSC8502 through SW1 is in the low state (right position). After connecting the USB cable which supplies power, toggle the NRESET input to the high state (left position) then back to the high state (left position).

4.2 PC Software Installation

1. Download the ZIP file from Microsemi's website onto a PC that has a USB port
2. Install the GUI by launching the setup.exe file
3. USB communication is assisted by the Silabs USBXpress® drive. If not present on the PC, the user will need to download the USBXpress
   Development Kit from the Silicon Labs website (URL: http://www.silabs.com/products/mcu/Pages/USBXpress.aspx)
4. Double click the desktop icon to launch the GUI

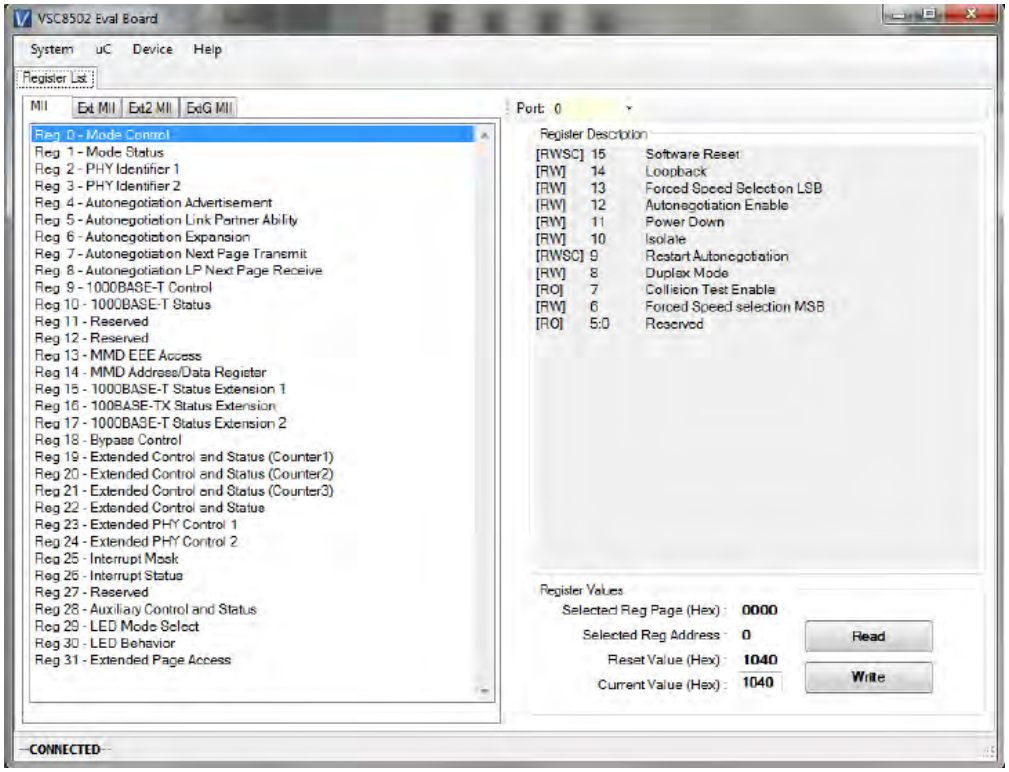
4.3 Connecting to the Board to the PC

After following the power sequence discussed in 3.1, launch the GUI either by clicking on the Desktop shortcut or clicking on **Start** > **Programs** > **Vitesse Semiconductor Corp** > **VSC8502_GUI**. The initial window will detect the attached USB devices automatically. Figure 3 shows a typical EVB Connection window.

Figure 3 • GUI Connection Window

The EVB serial number should appear. If not, click on “Scan For USB Devices.” Select that EVB serial number then click “Launch GUI”. The MII Register List GUI window will appear as shown in Figure 4. When the communication is successfully established, it should say “CONNECTED” at the bottom left corner of this GUI Window.

Figure 4 • MII Registers GUI Window



Verify the device is up and running by reading MII Register 0. It should read back 0x1040. Reading back all 0's or all 1's indicates a problem. For a multi-port device, the corresponding PHY port number is accessed via the "Port:" pick list shown above the Register Description in Figure 4.

As Figure 4 indicates, the extended MII register pages can be accessed to read or write by clicking on one of the ExtMII/Ext2MII/ExtGMII tabs.

4.3.1 Board Initialization

Once the evaluation board connectivity has been established and confirmed, the PHY should be initialized. Initialization can be accomplished by running an init-script sequence, such as performed by the pre- and post-reset functions of the PHY API standalone app.

While the init-script sequence may not be required for specific operational modes, an init-script sequence is highly recommended to ensure correct performance over the greatest set of user scenarios for the PHY. After initialization is performed, refer to the PHY Datasheet section on Configuring the PHY and PHY Interfaces for the desired application.

An initialization file, **vsc8502_init.txt**, is included in the GUI package. This initialization file will optimize the copper media interface settings based on the latest factory test result. To execute initialization script, click "Device" on the top menu and choose "Load Init Script" option, which will automatically load and execute vsc8502_init.txt file in the directory. Once the initialization is completed, it should say "LOADED 17 REGISTERS" at the bottom left corner of the GUI Window.

In addition, three other configuration scripts are included:

- vsc8502_RGMII_2nsRXCLKdelay.txt: configure the MAC interface to RGMII mode with 2.0 ns RX_CLK delay compensation. Note that the board is designed and laid out such that the RGMII DATA, CONTROL and CLOCK for each direction are matched in length approximately within +/-200 ps.

- vsc8502_RGMII_2nsGTXCLKdelay.txt: configure the MAC interface to RGMII mode with 2.0ns GTX_CLK delay compensation.
- vsc8502_10BTe_Config.txt: optimize the copper media interface settings for 10BASE-Te.

To load and execute configuration scripts, click “Device” on the top menu and choose “Load Config Script” option then select the desired script file. Once the script is executed, it should say “LOADED n REGISTERS” at the bottom left corner of the GUI Window, where n is the loaded registers count.

4.3.2 Copper Media Operation (Auto-negotiation Enabled)

The easiest configuration for passing traffic is with Autoneg enabled (MII 0.12 = 1). Use MII Register 0, 4 and 9 to change speed and restart autoneg (MII 0 bit 9) to advertise new settings. As per the datasheet descriptions, the commonly-used speed advertisement definitions are as follows:

Table 2 • Auto-Negotiation Advertisements

	MII reg 4 bits 8:7	MII reg 4 bits 6:5	MII reg 9 bits 12:11	MII reg 9 bits 9:8
1000BT Master mode	N/A	N/A	11	11
1000BT Slave mode	N/A	N/A	10	11
100 BASE-TX Full Duplex	11	N/A	N/A	00
10 BASE-T Full Duplex	00	11	N/A	00

The following steps are used to configure a link:

1. Set up the Copper traffic source (i.e., IXIA or Smartbits)
2. Run the vsc8502_init.txt script
3. Connect Ethernet cable(s) to a single or multiple RJ-45 ports
4. Connect 0.1 inch shunt jumpers between row-2 and row-3 of RGMII connectors as external loopback within a single port
5. Configure MAC interface for RGMII mode, enable RX_CLK output and set RX_CLK or GTX_CLK delay, as described in Configuration section of the datasheet. Alternatively, this can also be done by running either one of the two RGMII configuration scripts.
6. Configure auto-negotiation as per above and re-start ANEG (MII bit 0.12)
7. The linkup bit is in MII Reg 1, bit 2 (MII 1.2), read it twice to update

Traffic should now be flowing.

5 Useful Test Features

5.1 Ethernet Packet Generator

ExtMII 29E is the Ethernet Packet Generator register. The EPG sends traffic in multiple of 10,000 frames regardless of when you stop transmit activity. Refer to the datasheet for configuration options.

A Good CRC packet counter is in ExtMII 18.13:0. The Good CRC packet counter is a modulo 10,000 counter so values will always be between 0-9,999. A read of the register reads back the good CRC packets and then clears the register so the subsequent reads will be 0 if no traffic has been received. If traffic has been received since the last read, bit 15 will be set.

5.2 Copper PHY Error Counters

Idle errors = MII 10.7:0
RX errors = MII 19.7:0
False carrier = MII 20.7:0
Disconnects = MII 21.7:0
CRC errors = ExtMII 23.7:0

5.3 Near-End Loopback

When the near-end loopback test feature is enabled, the transmitted data is looped back in the PCS block on the receive data signals. To enable the loopback, set register bit 0.14 to 1. Near-end loopback mode involves traffic flow over the GMII/RGMII interface, so a breakout of the MAC interface on SAMTEC connector J1 must be connected to another system for this mode to pass traffic.

5.4 Far-End Loopback

When the far-end loopback test feature is enabled, incoming data from a link partner on the Copper interface to be transmitted back to the link partner on the Copper interface. To enable the loopback, set register bit 23.3 to 1.

5.5 Transmitter Test Mode

1000BASE-T PMA test control can be configured through reg.9.15:13. Please refer to PMA Test application note for additional information in regard to performing the PMA conformance test.

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

VPPD-03822