
HDMI Loopback Design

Introduction

This document describes how to run video loopback design using the PolarFire® Video Kit with a video source, display, HDMI TX port, and HDMI RX port. The demo design features a fully-integrated solution developed using Microchip's Libero® System-on-Chip (SoC) software that enables you to evaluate PolarFire FPGA in smart embedded vision applications and to build prototypes, quickly. For more information about Smart Embedded Vision IPs, see [Smart Embedded Vision](#).

The demo design captures the video and audio from a source using the HDMI 2.0 RX port and decodes the HDMI data as a video and an auxiliary data (audio and control data). The decoded data is then written to the FIFOs before looping back to an external HDMI compliant source or a monitor using the HDMI 2.0 TX port.

The following are the PolarFire Video Kit features:

- 300K LE FPGA (MPF300T-FCG1152)
- HDMI 2.0 TX
- HDMI 2.0 RX
- HDMI 1.4 TX

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1. Demo Prerequisites

Before you begin, perform the following steps:

- Download the design files from the following link: www.microchip.com/en-us/application-notes/AN4768.
- Download and install the Libero SoC Design Suite from [Libero SoC Software Downloads](#).

2. Demo Requirements

The following table lists the hardware and software required to run the demo.

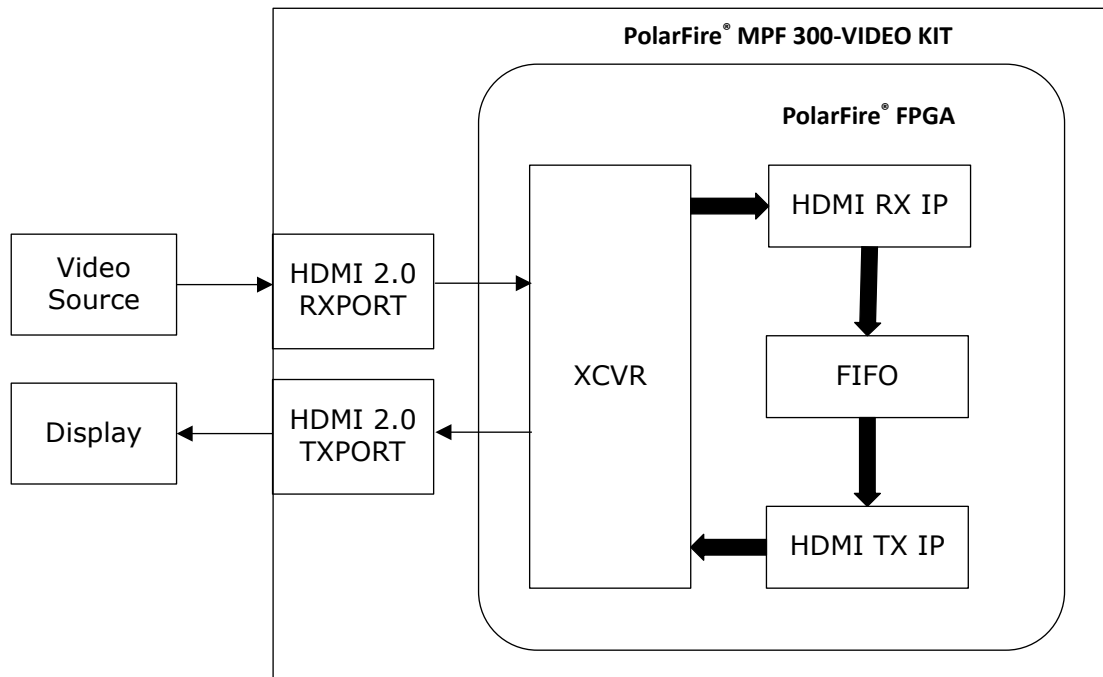
Table 2-1. Demo Requirements

| Requirement | Description |
|-----------------------------|--|
| Hardware | |
| PolarFire® video kit | DVP-102-000512-001 REV 1.0 |
| USB A to mini-B cable | Required for FPGA programming |
| HDMI Display | 1920 x 1080 (60 Hz) resolution |
| Two HDMI cables | HDMI A male-to-male cable |
| Power Adapter | 12V, 5A |
| Software | |
| Program_Debug_v22.3_win.exe | This executable file installs FlashPro Express that is used to program FPGA. |

3. Design Description

The following figure shows a high-level block diagram of the design.

Figure 3-1. Block Diagram



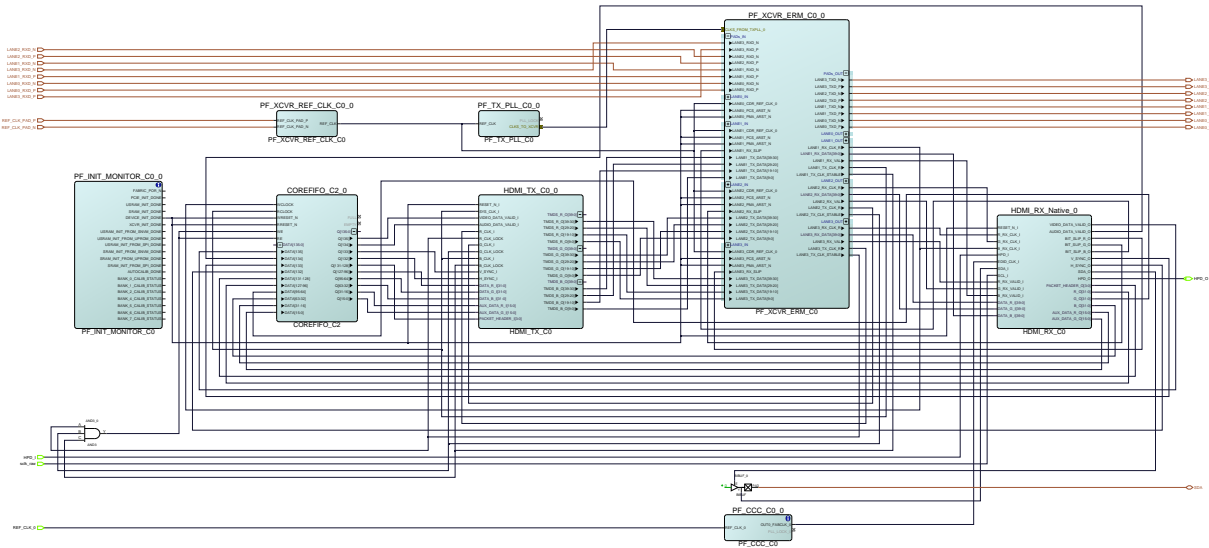
The video input is received through a HDMI compliant video source through the HDMI RX port. The serial HDMI data is converted to parallel data by XCVR. XCVR is configured for four lanes for HDMI video reception and transmission. The XCVR Lane 0 is a clock lane and remaining three lanes such as B, G, and R are used as data channels. XCVR is configured for 1.5 Gbps with 40 bits parallel data width to serialize four pixels per clock.

The 40 bits data (4 pixels) received at HDMI RX IP is decoded as either a video data or an auxiliary data, and the respective valid signals and frame control signals are generated. The decoded video data, audio data, and control signals are packed and written into a FIFO. The FIFO output data is unpacked to video, auxiliary, and control signals, which are given as inputs to the HDMI TX IP. The HDMI TX IP encodes the data using TMDS encoding. The encoded data is serialized by XCVR and sent to HDMI TX port. The display connected to the HDMI TX port receives the encoded data from the HDMI TX IP, which is the same video and audio as the HDMI RX input.

3.1 Hardware Implementation

The following figure shows the Libero SoC implementation of the top-level SmartDesign.

Figure 3-2. High-Level HDMI Loopback Design



The high-level HDMI loopback design includes the following key IP cores:

- XCVR
- HDMI TX IP
- HDMI RX IP
- FIFO
- XCVR

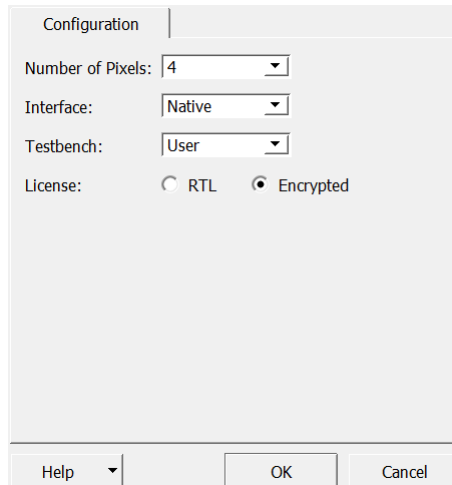
XCVR is configured in Full-Duplex mode, as the system receives Transition Minimized Differential Signaling (TMDS) data and transmits the encoded TMDS. XCVR uses LANE 0 for clock data and LANE 1, LANE 2, and LANE 3 a data lanes, and HDMI has three data channels such as: B, G, and R. In this system, the XCVR data rate is selected to support Full High Definition (FHD) video data transmission and reception at 60 FPS. XCVR serializes or deserializes the HDMI 40 bits data that contains four pixels where MSB 10 bits represent the latest pixel.

Figure 3-3. XCVR Configuration

| | | | |
|--|-------------------------|---|--------------|
| General | | | |
| Transceiver mode | Tx and Rx (Full Duplex) | <input type="checkbox"/> Enhanced receiver management | |
| Number of lanes | 4 | Receiver calibration | None (CDR) |
| | | <input type="checkbox"/> Incrementally recalibrate data eye | |
| | | <input type="checkbox"/> Incrementally recalibrate DFE coefficients | |
| PMA Settings | | | |
| TX data rate | 1485 Mbps | RX data rate | 1485 Mbps |
| TX clock division factor | 4 | RX CDR lock mode | Lock to data |
| TX PLL base data rate | 5940.000 Mbps | RX CDR reference clock source | Dedicated |
| TX PLL bit clock frequency | 2970.000 MHz | RX CDR reference clock frequency | 148.5 MHz |
| | | RX JA clock frequency | 37.125 MHz |
| PCS Settings | | | |
| TX PCS-Fabric interface width | 40 bits | RX PCS-Fabric interface width | 40 bits |
| TX FPGA interface frequency | 37.125 MHz | RX FPGA interface frequency | 37.125 MHz |
| PMA Mode | | | |
| <input checked="" type="checkbox"/> Enable CDR Bit-slip port | | | |
| <input type="checkbox"/> 8b10b Encoding/Decoding | | | |
| <input type="checkbox"/> 64b66b Gear Box | | | |
| <input checked="" type="radio"/> 64b66b | | <input checked="" type="radio"/> 64b67b | |
| <input type="checkbox"/> Enable Disparity | | <input type="checkbox"/> Enable BER monitor state machine | |
| <input type="checkbox"/> Enable Scrambler/Descrambler | | <input type="checkbox"/> Enable 32 bits data width | |
| SoR PIPE Interface | | | |
| Protocol: PCIe Gen1 (2.5 Gbps) | | | |
| Clocks and Resets | | | |
| Interface Clocks | | | |
| <input type="checkbox"/> Use as PLL reference clock | | | |
| TX clock | Regional | RX clock | Regional |

The HDMI RX IP is configured with four pixels per clock for native interface.

Figure 3-4. HDMI RX IP Configuration



The screenshot shows a configuration dialog box titled "Configuration". It contains the following settings:

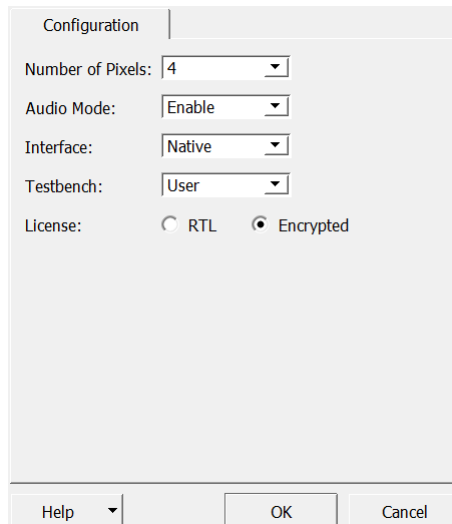
- Number of Pixels: 4 (dropdown menu)
- Interface: Native (dropdown menu)
- Testbench: User (dropdown menu)
- License: RTL Encrypted

At the bottom of the dialog, there are three buttons: "Help" (with a dropdown arrow), "OK", and "Cancel".

The HDMI RX IP decodes the TMDS data to video, auxiliary data, and control signals. The HDMI RX IP can be configured to operate in one pixel per clock or four with the interface type as Native and AXI-4.

The FIFO core passes the decoded data of video and audio and control signals to HDMI TX IP for encoding. The HDMI TX IP is configured in **Audio Mode** as **Enable** to encode the audio data along with the video data.

Figure 3-5. HDMI TX IP Configuration



The screenshot shows a configuration dialog box titled "Configuration". It contains the following settings:

- Number of Pixels: 4 (dropdown menu)
- Audio Mode: Enable (dropdown menu)
- Interface: Native (dropdown menu)
- Testbench: User (dropdown menu)
- License: RTL Encrypted

At the bottom of the dialog, there are three buttons: "Help" (with a dropdown arrow), "OK", and "Cancel".

3.2 I/O Ports

The following table lists the important I/O ports of the design.

Table 3-1. Important I/O Ports

| I/O Port | Direction | Description |
|---------------|------------------|------------------------|
| LANE0_RXD_N | Input | Lane 0 RX channel N |
| LANE0_RXD_P | Input | Lane 0 RX channel P |
| LANE1_RXD_N | Input | Lane 1 RX channel N |
| LANE1_RXD_P | Input | Lane 1 RX channel P |
| LANE2_RXD_N | Input | Lane 2 RX channel N |
| LANE2_RXD_P | Input | Lane 2 RX channel P |
| LANE3_RXD_N | Input | Lane 3 RX channel N |
| LANE3_RXD_P | Input | Lane 3 RX channel P |
| REF_CLK_PAD_N | Input | Reference clock N |
| REF_CLK_PAD_P | Input | Reference clock P |
| REF_CLK_0 | Input | Reference clock |
| SDA | Input and Output | Serial data |
| sclk_raw | Input | Serial clock |
| HPD_I | Input | Hot plug detect input |
| LANE0_TXD_N | Output | Lane 0 TX channel N |
| LANE0_TXD_P | Output | Lane 0 TX channel P |
| LANE1_TXD_N | Output | Lane 1 TX channel N |
| LANE1_TXD_P | Output | Lane 1 TX channel P |
| LANE2_TXD_N | Output | Lane 2 TX channel N |
| LANE2_TXD_P | Output | Lane 2 TX channel P |
| LANE3_TXD_N | Output | Lane 3 TX channel N |
| LANE3_TXD_P | Output | Lane 3 TX channel P |
| HPD_O | Output | Hot plug detect output |

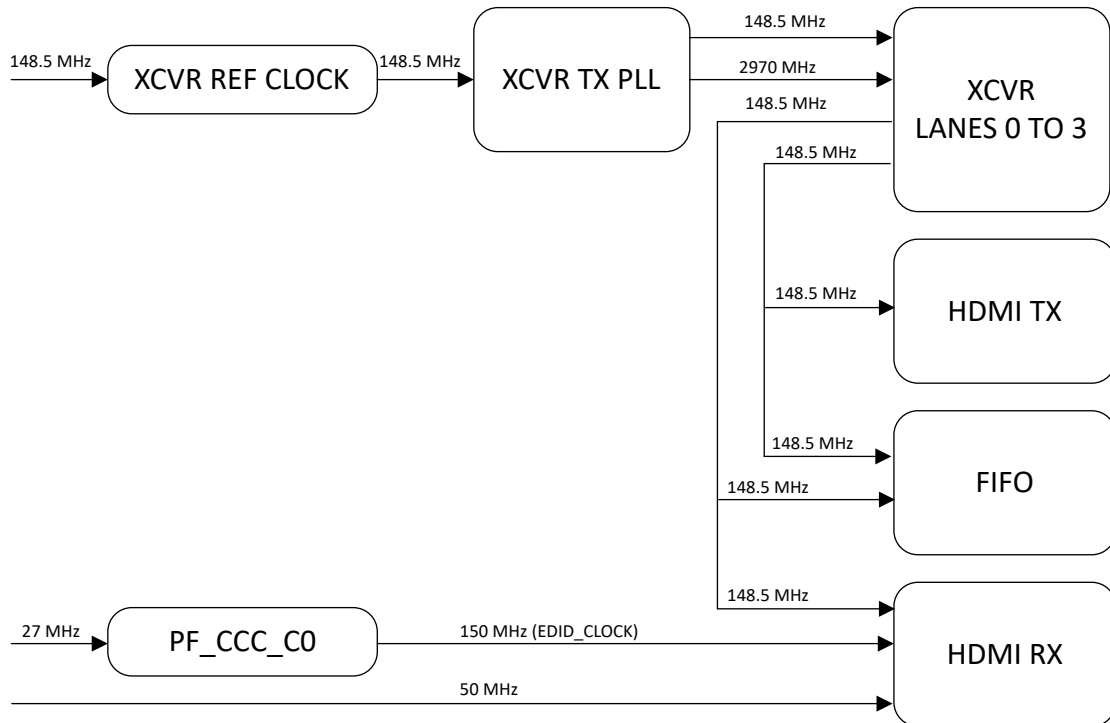
3.3 Clocking Structure

The design uses the following on-board clocks:

- The 27 MHz oscillator is used to provide a reference clock to PF_CCC_C0 and generates Extended Display Identification Data (EDID) clock of 150 MHz; the 148.5 MHz clock is used as a reference clock to XCVR as shown in the following figure.
- The XCVR TX PLL subsystem generates a bit clock, and XCVR transmits and receives clocks. The on-board 50 MHz clock is used as an I²C serial clock.

The following figure shows the clocking structure of the design.

Figure 3-6. Clocking Structure

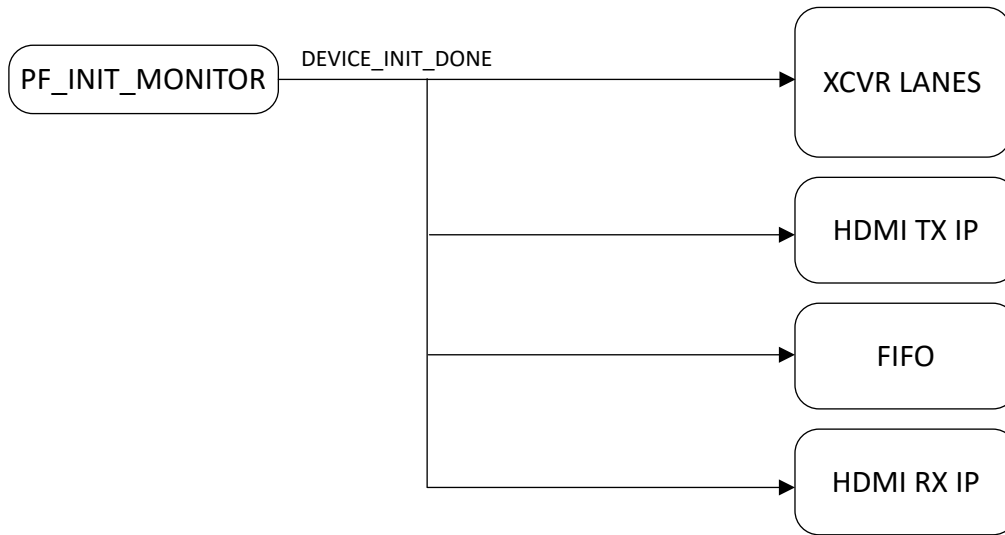


3.4 Reset Structure

The HDMI loopback design is released from the reset when the DEVICE_INIT_DONE signal of the PF_INIT_MONITIR block is de-asserted.

The following figure shows the reset structure of the design.

Figure 3-7. Reset Structure



4. Setting Up the Demo

Setting up the demo involves the following steps:

1. [Setting Up the Hardware](#)
2. [Programming the Device](#)

4.1 Setting Up the Hardware

Setting up the hardware involves interfacing HDMI source (Host PC) and HDMI display with the PolarFire Video Kit and verifying the jumper settings.

Perform the following steps to set up the hardware:

1. Connect the Host PC and the video kit through **J12** of the video kit using the USB mini cable.
2. Connect the HDMI 1920x1080 display to **J1** (HDMI 2.0 TX port) of the video kit.
3. Connect the HDMI source to **J35** (HDMI 2.0 RX port) of the video kit.
4. Connect the Host PC and video kit through the USB port (J12) of the video kit using the USB mini cable.
5. Connect the power supply cable to **J20** of the video kit.
6. Power up the HDMI monitor.
7. Power up the board using the **SW4** slide switch.

4.2 Programming the Device

To program the PolarFire device with the `.job` file provided as part of the design files using the FlashPro Express software, see [6. Appendix A : Programming the Device using FlashPro Express](#).

5. Running the Demo

When programming is done, the video sent by the source is displayed on the sink (monitor).

This concludes the demo.

6. Appendix A : Programming the Device using FlashPro Express

This section describes how to program the PolarFire device with the .job file using FlashPro Express. The HDMI_RX_TX.job file is available at the following location.

```
<$designfiles download
directory>\mpf_an4768_v2022p2_df\VKPFHDMIRXTX\designer\HDMI_RX_TX\export
```

Perform the following steps to program the PolarFire device with the .job file:

1. On the Host PC, start the FlashPro Express software from its installation directory.
2. Select **New** or **New Job Project from FlashPro Express Job** from Project menu to create a new job project.
3. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:
 - a. Programming job file: Click **Browse** and navigate to the location where the HDMI_RX_TX.job file is located and select the file. The default location is <\$ designfiles download directory>\mpf_an4768_v2022p2_df\VKPFHDMIRXTX\designer\HDMI_RX_TX\export.
 - b. FlashPro Express job project location: Select **Browse** and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears.
5. Verify that a programmer number appears in the **Programmer** box. If it does not, verify the board connections and click **Refresh/Rescan Programmers**.
6. Click **Run** to program the device. When the device is programmed successfully, a **Run PASSED** status is displayed.
7. Close FlashPro Express (**Project > Exit**). The PolarFire device and SPI Flash are programmed.
8. Power cycle the board using the **SW4** switch. After power cycling, the full HD displays the video from the Host PC.

7. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 7-1. Revision History

| Revision | Date | Description |
|----------|---------|-------------------|
| A | 11/2022 | Initial revision. |

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