AVR64EA28/32/48 Silicon Errata and Data Sheet Clarifications

AVR64EA28/32/48

The AVR64EA28/32/48 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002443), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR64EA28/32/48 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002443) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. B1(1)	Rev. B2
Device	2.2.1. NVM Programming Does Not Work Below 2.7V	X	-
	2.2.2. Reduced Flash Endurance for VDD Below BODLEVEL3	X	-
	2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces	X	X
	2.2.4. Limitation on Flash Boot Size and Flash Code Size Fuses	-	X
CRCSCAN	2.3.1. Running CRC Scan on Part of The Flash is Non-Functional	X	-
NVMCTRL	2.4.1. Flash Multi Page Erase Non-Functional from UPDI	X	X
	2.4.2. Flash-Self Programming Failing When Flash Read During Programming	X	-
USART	2.5.1. Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 NVM Programming Does Not Work Below 2.7V

Performing an erase or write operation when V_{DD} is below 2.7V may fail. Recommending to make sure that V_{DD} is above 2.7V before starting an erase or a write operation. Alternatively, BOD can be enabled with a level set to BODLEVEL2 or higher.

Work Around

None.

Affected Silicon Revisions

Rev. B1	Rev. B2
X	-

2.2.2 Reduced Flash Endurance for V_{DD} Below BODLEVEL3

If operating at V_{DD} below BODLEVEL3, Flash endurance is reduced to 1k erase/write cycles. The reduction is independent of the V_{DD} level during erase/write.

Work Around

None

Affected Silicon Revisions

Rev. B1	Rev. B2
X	-

2.2.3 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by either an ST/STD instruction to address < 64 or a write to the SLPCTRL.CTRLA register will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. B1	Rev. B2
X	X

2.2.4 Limitation on Flash Boot Size and Flash Code Size Fuses

If CRC is enabled through fuse (CRCSRC in FUSE.SYSCFG0) or started from software using CRCSCAN, the Flash Boot Size (FUSE.BOOTSIZE) and Flash Code Size (FUSE.CODESIZE) must be configured to be a multiple of 512 bytes (LSb of FUSE.BOOTSIZE and FUSE.CODESIZE must be '0').

Work Around

None.

Affected Silicon Revisions

Rev. B1	Rev. B2
-	X

2.3 CRCSCAN - Cyclic Redundancy Check Memory Scan

2.3.1 Running CRC Scan on Part of The Flash is Non-Functional

- Running CRC scan on the boot section does not work if FUSE.BOOTSIZE is different from 0x00
- Running CRC scan on the boot and application section does not work if FUSE.CODESIZE is different from 0x00
- Running CRC scan on the entire Flash works

Work Around

None

Affected Silicon Revisions

Rev. B1	Rev. B2
X	-

2.4 NVMCTRL - Nonvolatile Memory Controller

2.4.1 Flash Multi Page Erase Non-Functional from UPDI

Performing a Flash multi-page erase (writing the CMD bitfield in NVMCTRL.CTRLA to FLMPERn) from UPDI does not work on the boot section. It is not recommended to use multi-page erase on any Flash section.

Work Around

Use Flash page erase (writing the CMD bitfield in NVMCTRL.CTRLA to 0x08).

Affected Silicon Revisions

Rev. B1	Rev. B2
X	X

2.4.2 Flash-Self Programming Failing When Flash Read During Programming

If data are read from the Flash NRWW section while the Flash RWW section is being written to or erased (Flash Page Write or Flash Page Erase), the erase or write may fail. Instruction fetch from the Flash NRWW section does not affect erase or write operation to the Flash RWW section.

Work Around

Alternative 1: RWW functionality not needed

- Do not use flash self-programming when executing from the NRWW section

Alternative 2: RWW functionality needed

- Enable BOD in continuous mode (in FUSE.BODCFG, set bitfield LVL to BODLEVEL1 or higher and bitfield ACTIVE to 0x3)
- Do not use the *Flash Page Erase and Page Write* operation (writing the CMD bitfield in NVMCTRL.CTRLA to 0x05). Execute Flash Page Erase and Flash Page Write as two separate operations instead.

Affected Silicon Revisions

Rev. B1	Rev. B2
X	-

2.5 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.5.1 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. B1	Rev. B2
X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002443).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 SPI - Serial Peripheral Interface

A clarification has been made to the *Operation - Client Mode* section. The last sentence is removed.

26.3.2.2 Client Mode

In Client mode, the SPI peripheral receives the SPI clock and Client Select from a Host. Client mode supports three operational modes: One Normal mode and two configurations for the Buffered mode. In Client mode, the control logic will sample the incoming signal on the SCK pin. ~~**To ensure correct sampling of this clock signal, the minimum low and high periods must each be longer than two peripheral clock cycles.**~~

3.2 SPI - Serial Peripheral Interface

A clarification has been made to the *Operation - Client Mode - Buffer Mode* section.

26.3.2.2.2 Buffer Mode

The SPI peripheral can be configured in Buffered mode by writing a '1' to the Buffer Mode Enable (BUFEN) bit in the Control B (SPIn.CTRLB) register to avoid data collisions.

This mode will enable two receive buffers and one transmit buffer. Both will have separate interrupt flags, transmit complete and receive complete. *Figure 26-1* shows the extra buffers.

When Buffer mode is enabled, it can work in two different ways. The Buffer Mode Wait for Receive (BUFWR) bit in the Control B (SPIn.CTRLB) register controls how the Buffer mode works. The details of how they work, including timing diagrams, are described below.

Note: When operating as a client in Buffered mode and the SPI clock is close to maximum frequency, the client may not be able to set up data in time for the first sample edge during back-to-back transfers. Refer to the *Electrical Characteristics - SPI* section for details.

3.3 Electrical Characteristics - Supply Voltage

Some clarifications have been made to the *Supply Voltage* table.

Table 35-4. Supply Voltage

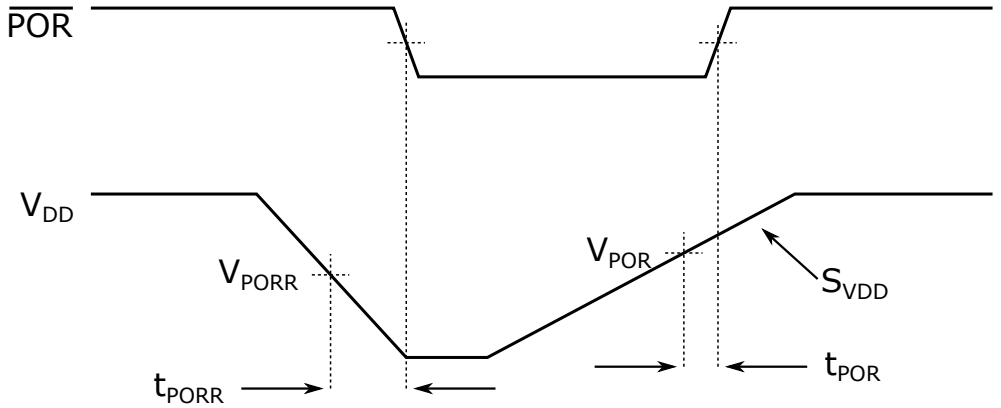
Symbol	Min.	Typ. †	Max.	Unit	Conditions
Supply Voltage[1]					
V_{DD}	1.8[2]	—	5.5	V	
RAM Data Retention[3]					
V_{DR}	1.7	—	—	V	Device in Power-Down mode
Power-on Reset Release Voltage[5]					
V_{POR}	—	1.6	—	V	BOD disabled[4]
t_{POR}	—	—	—	µs	BOD disabled[4]
Power-on Reset Re-Arm Voltage[5]					
V_{PORR}	—	**1.1**	—	V	BOD disabled[4]
t_{PORR}	—	—	—	µs	BOD disabled[4]
V_{DD} Slope[6]					
S_{VDD}	—	—	**0.2**	V/µs	**BOD disabled[4]**

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

Notes:

1. During Chip Erase, the Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON. The erase attempt will fail if the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0.
2. Operation is ensured down to 1.8V or BOD triggering level V_{BOD} when BOD is active.
3. This is the limit to which V_{DD} can be lowered in sleep mode without losing RAM data.
4. Refer to 35.11. RSTCTRL and BOD for BOD trip point information.
5. Refer to Figure 35-1.
6. For design guidance only and not tested in production.

Figure 35-1. $\overline{POR}$ and $\overline{POR}$ Re-Arm with Slow Rising V_{DD}



Note: When $\overline{POR}$ is low, the device is held in Reset.

3.4 Electrical Characteristics - Peripherals Power Consumption

Some clarifications have been made to the *Peripheral Power Consumption* table.

Table 35-6. Peripheral Power Consumption[1]

Operating conditions: V_{DD} = 3.0V T_A = 25°C OSCHF at 20 MHz with a prescaler division factor of six used as clock source Device in Standby sleep mode							
Symbol	**Description**	**Min.**	**Typ. †**	**Max. 85°C**	**Max. 125°C**	**Unit**	**Conditions**
I_{DD_WDT}	Watchdog Timer (WDT)	—	**0.68**	—	—	**µA**	32.768 kHz internal oscillator
I_{DD_BG}	**Bandgap**	**—**	**19**	**—**	**—**	**µA**	
I_{DD_VREF}	Voltage Reference (VREF)	—	**54**	—	—	µA	**DAC0REF.REFSEL = 0x1 (2.048V)** **Excluding bandgap**
		—	**48**	—	—	µA	**ACREF.REFSEL = 0x1 (2.048V)** **Excluding bandgap**
I_{DD_BOD}	Brown-out Detector (BOD)	—	14	—	—	µA	Brown-out Detect (BOD) continuous **Excluding bandgap**
		—	0.60	—	—	µA	Brown-out Detect (BOD) sampling @128 Hz, including I_{DD_OSC32K} **Excluding bandgap**
		—	**0.40**	**6**	—	µA	Brown-out Detect (BOD) sampling @32 Hz, including I_{DD_OSC32K} **Excluding bandgap**
I_{DD_TCA}	16-bit Timer/Counter Type A (TCA)	—	38	—	—	µA	Device in Idle sleep mode
I_{DD_TCB}	16-bit Timer/Counter Type B (TCB)	—	19	—	—	µA	
I_{DD_RTC}	Real-Time Counter (RTC)	—	**18**	—	—	µA	32.768 kHz internal oscillator (OSC32K)
I_{DD_OSC32K}	32.768 kHz Internal Oscillator (OSC32K)	—	**0.42**	—	—	µA	
$I_{DD\_XOSC32K}$	32.768 kHz Crystal Oscillator (XOSC32K)	—	**1.3**	—	—	µA	**XOSC32KCTRLA.LPMODE Enabled** **ESR = 50 kΩ, C_L = 12.5 pF**
		—	**5.7**	**—**	**—**	**µA**	**XOSC32KCTRLA.LPMODE Disabled** **ESR = 50 kΩ, C_L = 12.5 pF**
I_{DD_OSCHF}	Internal High Frequency Oscillator (OSCHF)	—	**85**	—	—	µA	
I_{DD_XOSCHF}	High Frequency Crystal Oscillator (XOSCHF)	—	—	—	—	µA	
I_{DD_ADC}	Analog-to-Digital Converter (ADC)	—	**295**	—	—	µA	**CTRLC.REFSEL = 0x0** **(V_{DD})**
		—	**570**	—	—	µA	**CTRLC.REFSEL = 0x5** **(Internal reference 2.048V)**
I_{DD_AC}	**Analog Comparator (AC)**	**—**	**150**	**—**	**—**	**µA**	**CTRLA.POWER = 0x0,** **device in Idle sleep mode**
		—	**110**	**—**	**—**	**µA**	**CTRLA.POWER = 0x1,** **device in Idle sleep mode**

.....continued

Operating conditions:

V_{DD} = 3.0V

T_A = 25°C

OSCHF at 20 MHz with a prescaler division factor of six used as clock source

Device in Standby sleep mode

Symbol	Description	Min.	Typ. †	Max. 85°C	Max. 125°C	Unit	Conditions
I_{DD_DAC}	Digital-to-Analog Converter (DAC)	—	**106**	—	—	µA	V_{DACREF} = 1.024V, device in Idle sleep mode
		—	125	—	—	µA	V_{DACREF} = 4.096V, device in Idle sleep mode
		—	**100**	—	—	µA	V_{DACREF} = V_{DD}, device in Idle sleep mode
I_{DD_USART}	Universal Synchronous and Asynchronous Receiver and Transmitter (USART)	—	**51**	—	—	µA	USART Enabled @9600 Baud
I_{DD_SPI}	Serial Peripheral Interface (SPI)	—	**14**	—	—	µA	SPI Host @100 kHz, device in Idle sleep mode
I_{DD_TWI}	Two-Wire Interface (TWI)	—	**56**	—	—	µA	TWI Host @100 kHz, device in Idle sleep mode
		—	**46**	—	—	µA	TWI Client @100 kHz, device in Idle sleep mode
$I_{DD\_NVM\_ERASE}$	Flash Programming Erase	—	**7**	—	—	mA	
$I_{DD\_NVM\_WRITE}$	Flash Programming Write	—	**10**	—	—	mA	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

Notes:

1. The module's current consumption only. To calculate the total internal power consumption of the microcontroller, add the power consumption values of all the peripherals and the clock sources used to the base power consumption given in 35.5. Power Consumption.
2. **Average power consumption with the following conditions:**
   - **Single-ended 12-bit ADC**
   - **ADC active in Free Running mode**
   - **CLK_ADC = 1 MHz**
   - **Device in Idle sleep mode**

3.5 Electrical Characteristics - I/O Pins

A clarification has been made to the *I/O Pin Specifications* table.

Table 35-7. I/O Pin Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Input Low Voltage						
V_{IL}	I/O PORT:					
	• with Schmitt Trigger buffer	—	—	0.2 × V_{DD}	V	INLVL = 0
	• with TTL levels	—	< 0.8	—	V	V_{DD} > 2.7V INLVL = 1
	$\overline{\text{RESET}}$ pin	—	—	0.2 × V_{DD}	V	
Input High Voltage						
V_{IH}	I/O PORT:					
	• with Schmitt Trigger buffer	0.8 × V_{DD}	—	—	V	INLVL = 0
	• with TTL levels	—	> 2.0	—	V	V_{DD} > 2.7V INLVL = 1
	$\overline{\text{RESET}}$ pin	0.8 × V_{DD}	—	—	V	
Input Leakage Current(1)						
I_{IL}	I/O PORTS	—	< 50	—	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A= 85°C
	$\overline{\text{RESET}}$ pin(2)	—	< 50	—	nA	GND ≤ V_{PIN} ≤ V_{DD}, pin at high-impedance, T_A= 85°C
Pull-up Resistance						
R_P		—	26	—	kΩ	
Output Low Voltage						
V_{OL}	Standard I/O ports	—	—	—	V	I_{OL} = 6 mA, V_{DD} = 3.0V
Output High Voltage						
V_{OH}	Standard I/O ports	—	—	—	V	I_{OH} = 6 mA, V_{DD} = 3.0V
I/O Slew Rate						
t_{SR}	Rising slew rate	—	45	—	ns	PORTCTRL.SRL = 0x01
	Rising slew rate	—	22	—	ns	PORTCTRL.SRL = 0x00
	Falling slew rate	—	30	—	ns	PORTCTRL.SRL = 0x01
	Falling slew rate	—	16	—	ns	PORTCTRL.SRL = 0x00
Pin Capacitance						
C_{IO}	All I/O pins	—	5	—	pF	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

Notes:

1. The negative current is defined as the current sourced by the pin.
2. The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. A higher leakage current may occur at different input voltages.

3.6 Electrical Characteristics - RSTCTRL and BOD

A clarification has been made to change the Brown-out Detect Voltage (V_{BOD}) in the *Reset, WDT, Oscillator Start-up Timer, Power-up Timer and Brown-out Detector Specifications* table.

Table 35-15. Reset, WDT, Oscillator Start-up Timer, Power-up Timer, Brown-out Detector Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
t_{RST} *	$\overline{\text{RESET}}$ pin pulse-width low to ensure a Reset	2.5	—	—	µs	
R_{RST_UP} *	$\overline{\text{RESET}}$ pin pull-up resistor	—	35	—	kΩ	
T_{OST} *	Oscillator start-up timer period(1)	—	1024	—	cycles	
V_{BOD+}	Brown-out Detect Voltage, rising slope(2)	—	1.75	**—**	V	BODLEVEL0
			1.90	**2.10**	V	BODLEVEL1
			2.60	**2.80**	V	BODLEVEL2
			4.30	**4.60**	V	BODLEVEL3
V_{BOD-}	Brown-out Detect Voltage, falling slope(2)	**1.62**	1.75	—	V	BODLEVEL0
		1.80	1.90		V	BODLEVEL1
		2.43	2.60		V	BODLEVEL2
		4.05	4.30		V	BODLEVEL3
V_{BOD_HYS}	Brown-out Detect hysteresis	—	25	—	mV	
t_{BOD_ST}	Brown-out Detect start-up time from sleep	—	30	—	µs	
t_{BOD}	BOD sampling time when used in Sampling mode	—	$1/f_{BOD}$	—	ms	
t_{BOD_RST}	Brown-out Reset response time	—	4	—	µs	$V_{DD} = V_{BOD}$ - 0.1V

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

***** These parameters are characterized but not tested in production.

Notes:

1. By design, the Oscillator Start-up Timer (T_{OST}) counts the first 1024 cycles, independent of frequency.
2. VDD and GND must be capacitively decoupled as close to the device as possible to ensure these voltage tolerances. Recommended values are 0.1 µF and 0.01 µF in parallel.

3.7 Electrical Characteristics - SPI

Some clarifications have been made to the *Timing Specifications in Host Mode* and *Timing Specifications in Client Mode* tables. Note that some rows have been deleted.

Table 35-19. SPI - Timing Specifications in Host Mode

Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
f_{SCK} *	SCK clock frequency	—	—	**$f_{CLK\_PER}/2$**	MHz	
T_{SCK} *	SCK period	**2 × T_{CLK_PER}**	—	—	ns	
t_{SCKW}	SCK high/low width	—	0.5 × T_{SCK}	—	ns	
t_{MIS}	MISO setup to SCK	—	**T_{CLK_PER}**	—	ns	
t_{MIH}	MISO hold after SCK	—	**0**	—	ns	
t_{MOS}	MOSI setup to SCK	—	0.5 × T_{SCK}	—	ns	
t_{MOH}	MOSI hold after SCK	—	**0.5 × T_{SCK}**	—	ns	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

***** These parameters are characterized but not tested in production.

Table 35-20. SPI - Timing Specifications in Client Mode

Symbol	Description	Min.	Typ. †	Max.	Unit	Condition
f_{SSCK} *	Client SCK clock frequency	—	—	**$f_{CLK\_PER}/6$**	MHz	
T_{SSCK} *	Client SCK period	**$6 \times T_{CLK\_PER}$**	—	—	ns	
t_{SSCKW} *	SCK high/low width	**$3 \times T_{CLK\_PER}$**	—	—	ns	
t_{SIS} *	MOSI setup to SCK	**0**	—	—	ns	
t_{SIH} *	MOSI hold after SCK	**$3 \times T_{CLK\_PER}$**	—	—	ns	
t_{SSS} *	SS setup to SCK	**T_{CLK_PER}**	—	—	ns	
t_{SSH} *	SS hold after SCK	**T_{CLK_PER}**	—	—	ns	
t_{SOS}	**MISO valid after SCK**	—	**t_{SR}**	—	ns	**$f_{SSCK} \geq f_{CLK\_PER}/6$**
			—			**$f_{SSCK} < f_{CLK\_PER}/6$**
t_{SOSS}	MISO setup after SS low	—	**t_{SR}**	—	ns	
t_{SOSH}	MISO hold after SS low	—	**t_{SR}**	—	ns	

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

***** These parameters are characterized but not tested in production.

3.8 Electrical Characteristics - AC

Some clarifications have been made to the *Analog Comparator Specifications* table.

Table 35-27. Analog Comparator Specifications

Operating conditions: V_{DD} = 3.0V T_A = 25°C						
Symbol	**Description**	**Min.**	**Typ. †**	**Max.**	**Unit**	**Conditions**
V_{IN} *	Input voltage range	-0.2	—	V_{DD}	V	
I_L	Input leakage current	—	5	—	nA	
V_{OFF}	**Input offset voltage**	**-30**	**±10**	**30**	**mV**	**0.1V < V_{IN} < (V_{DD} - 0.1V)**
CMRR *	Common mode input rejection ratio	—	**70**	—	dB	0.1V < V_{IN} < (V_{DD} - 0.1V)
V_{HYST}	**Hysteresis**	**—**	**10**	**—**	**mV**	**CTRLA.HYSMODE = 0x1**
		—	**20**	**—**		**CTRLA.HYSMODE = 0x2**
		—	**30**	**—**		**CTRLA.HYSMODE = 0x3**
t_{RESP} *	**Response time, rising edge**	**—**	**50**	**—**	**ns**	**CTRLA.POWER = 0x0,**
	Response time, falling edge	**—**	**150**	**—**	**ns**	**V_{CM} = V_{DD}/2**

† Unless otherwise specified, data in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V. These parameters are not tested and are for design guidance only.

***** These parameters are characterized but not tested in production.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
D	02/2024	Updated Silicon Revision: B2 Added errata: • Device: 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces Added Data Sheet Clarifications: • SPI: – 3.1. SPI - Serial Peripheral Interface – 3.2. SPI - Serial Peripheral Interface • Electrical Characteristics: – 3.5. Electrical Characteristics - I/O Pins – 3.7. Electrical Characteristics - SPI
C	11/2023	Added Silicon Revision: B2 Added errata: • Device: 2.2.4. Limitation on Flash Boot Size and Flash Code Size Fuses Added Data Sheet Clarifications: Electrical Characteristics: • 3.3. Electrical Characteristics - Supply Voltage • 3.4. Electrical Characteristics - Peripherals Power Consumption • 3.6. Electrical Characteristics - RSTCTRL and BOD • 3.8. Electrical Characteristics - AC
B	06/2023	Added errata: • Device: 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces • NVMCTRL: 2.4.2. Flash-Self Programming Failing When Flash Read During Programming Removed errata: • NVMCTRL: *Flash Page Erase/Write Operation Non-Functional*
A	02/2023	Initial document release

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