MICROCHIP

# TB3123

# Windowed Watchdog Timer on PIC® Microcontrollers

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## INTRODUCTION

The Windowed Watchdog Timer (WWDT) is an enhanced Watchdog Timer found on PIC® microcontrollers. This is an extension of the existing Watchdog Timer (WDT) on PIC microcontrollers. Microchip's WDT has both a configurable upper-time threshold limit and a fixed lower-time threshold of '0'. WWDT's both upper and lower-time threshold limits are configurable in software.

## WWDT OVERVIEW

**FIGURE 1: PERIPHERAL BLOCK DIAGRAM**

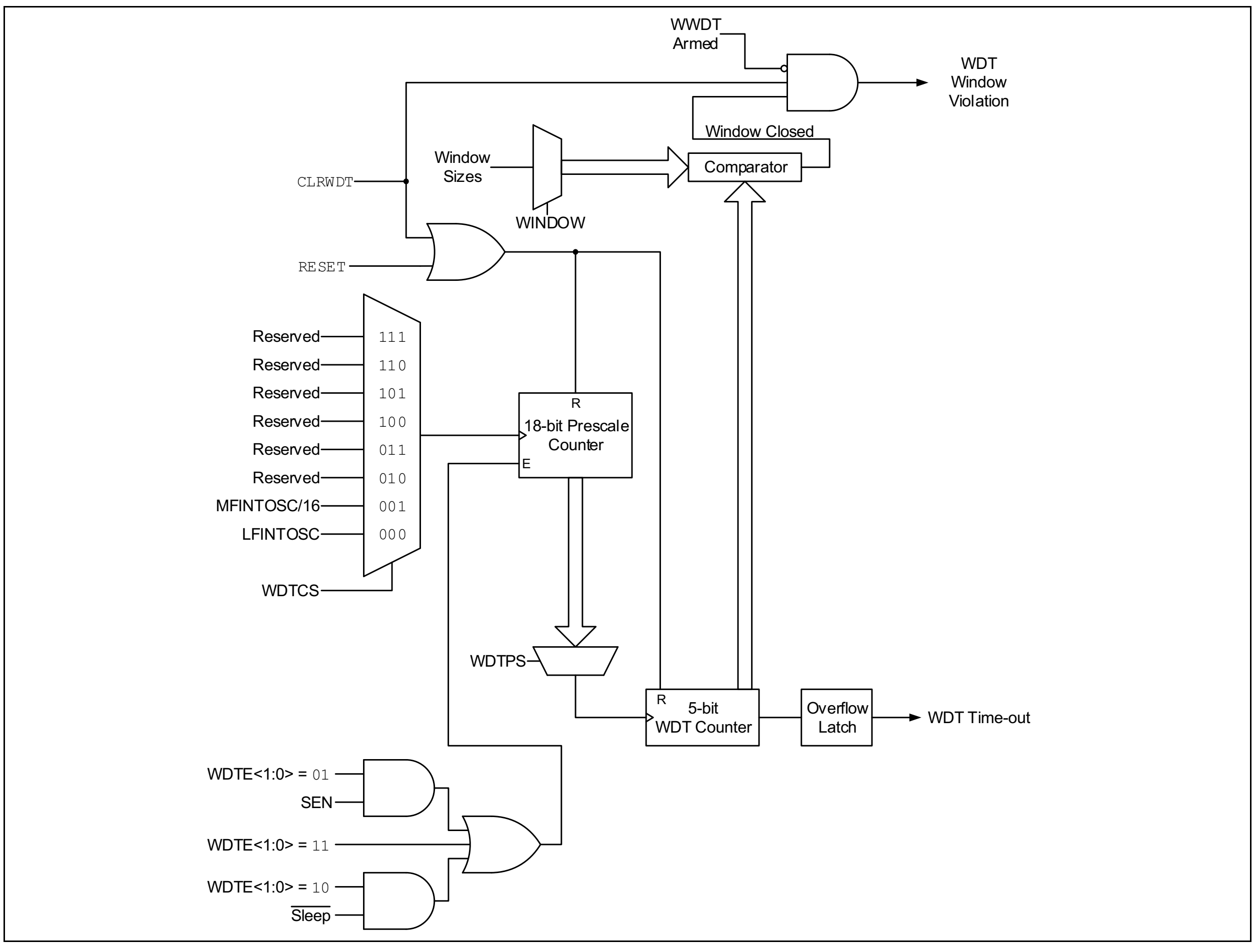

Figure 1 shows the block diagram for the WWDT.

The timer is set for time delay, which is required for one worst-case pass through the program main loop. The timer is configurable through the Control register. The user's application should periodically issue a `CLRWDT` instruction before the timer reaches its set maximum count and it overflows. If the user's application fails to reset the timer using the `CLRWDT` instruction, the watchdog overflows and resets the program execution back to the program entry point. This also resets the $\overline{TO}$ bit (Time-out bit) in the STATUS register and the $\overline{RWDT}$ bit in the PCON (Power Control) register to '0', which indicates that watchdog Reset has occurred. The WWDT is usually used to prevent a program execution lock-up or blocking caused by an infinite loop, code freeze or thread blocks. It is used as an ultimate fail-safe protection system for user code.

The PIC microcontroller supports the following watchdog modes as explained in Table 1.

### TABLE 1: WWDT MODES

| WWDT Modes | Explanation |
|---|---|
| WWDT always ON | WWDT is always ON and operational, including Sleep mode |
| WWDT OFF in Sleep | WWDT is always ON, except in Sleep mode |
| WWDT controlled by software | WWDT operation (i.e., the ON and OFF state for the WWDT is controlled through software using the WWDT Enable/Disable bit in the WWDT Control register) |
| WWDT always OFF | WWDT is always OFF irrespective of the CPU state |

The WWDT is an extension to the existing WWDT as explained below (see Figure 2):

1. The WWDT period is divided into two smaller time slots.
2. The first part of the WWDT period is called window close time. If the `CLRWDT` instruction is executed during this period, the program execution will reset to the program entry point and the $\overline{WDTWV}$ (WWDT Window Violation) bit in the PCON register will reset to '0'.
3. The second part of the WWDT period is called window open time. The `CLRWDT` instruction should be executed; otherwise, the WWDT time-out occurs and will reset the program execution. The $\overline{TO}$ bit in the STATUS register and the $\overline{RWDT}$ bit in the PCON register will reset to '0'.
4. The window close time and window open time represent the complete WWDT period.
5. The window size is configurable in the WDTCON1 register as shown in Table 2. For example, if the WDTCON1 window size bits set to `101b`, the window open time will be the last 75% of the total WWDT period, and the window close time will be the initial 25% of the WWDT period.

## ARMING OF THE WWDT

The WWDT is armed by reading the WDTCON0 register. Before executing the `CLRWDT` instruction, the WWDT must be armed in Windowed mode (WINDOW<2:0> = 111). There is no timing requirement as to the moment the timer is armed and the `CLRWDT` instruction is executed (i.e., the two events can be separated by any number of instructions). Executing the `CLRWDT` instruction without arming generates a window violation Reset. The STATE bit in the WDTTMR register determines if the WWDT is armed successfully.

> **Note:** When Windowed mode is used while interrupts are enabled, follow either of the two steps below:
> 1. Arm the WWDT before returning from the ISR
> 2. Outside the ISR, disable global interrupts, arm the WWDT, execute the `CLRWDT` instruction and re-enable the interrupts.

**FIGURE 2: WWDT WINDOW CLOSING AND OPENING TIME**

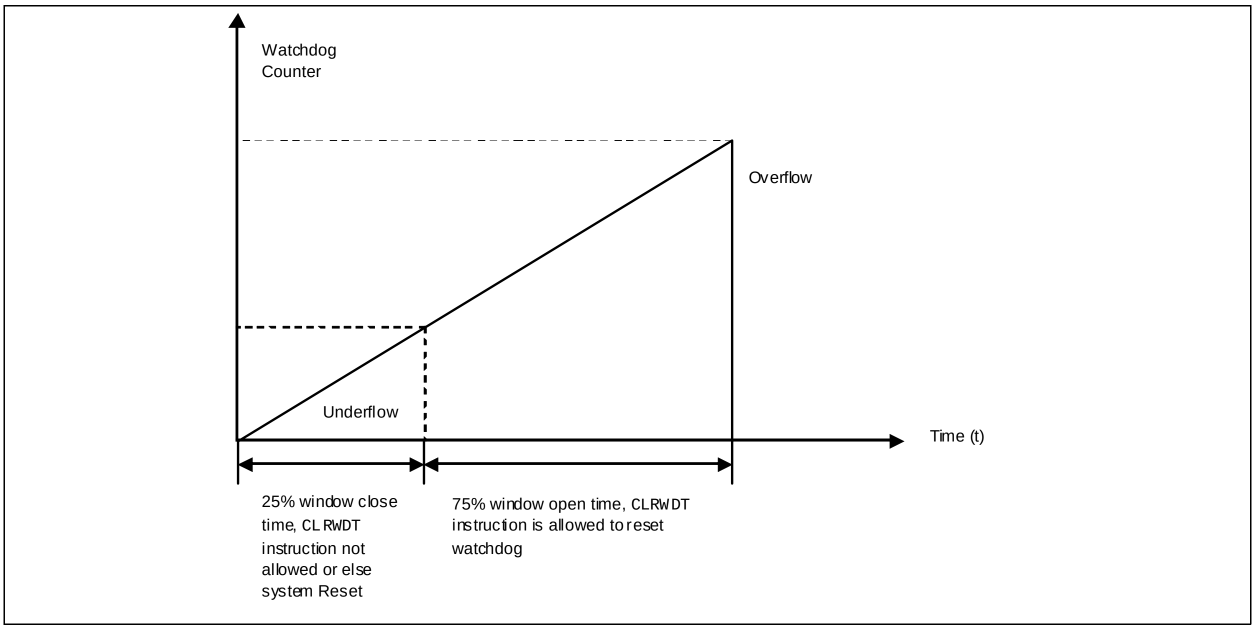


**TABLE 2: WINDOW SIZE IN WWDT**

| WDTCON1 (WINDOW<2:0>) | Window Delay/Window Closed Time in % | Window Opening Time in % |
|---|---|---|
| 111 | --- | 100 |
| 110 | 12.5 | 87.5 |
| 101 | 25 | 75 |
| 100 | 37.5 | 62.5 |
| 011 | 50 | 50 |
| 010 | 62.5 | 37.5 |
| 001 | 75 | 25 |
| 000 | 87.5 | 12.5 |

**FIGURE 3: WINDOWED WATCHDOG TIMER WINDOW OVERFLOW AND UNDERFLOW/ WINDOW VIOLATION**

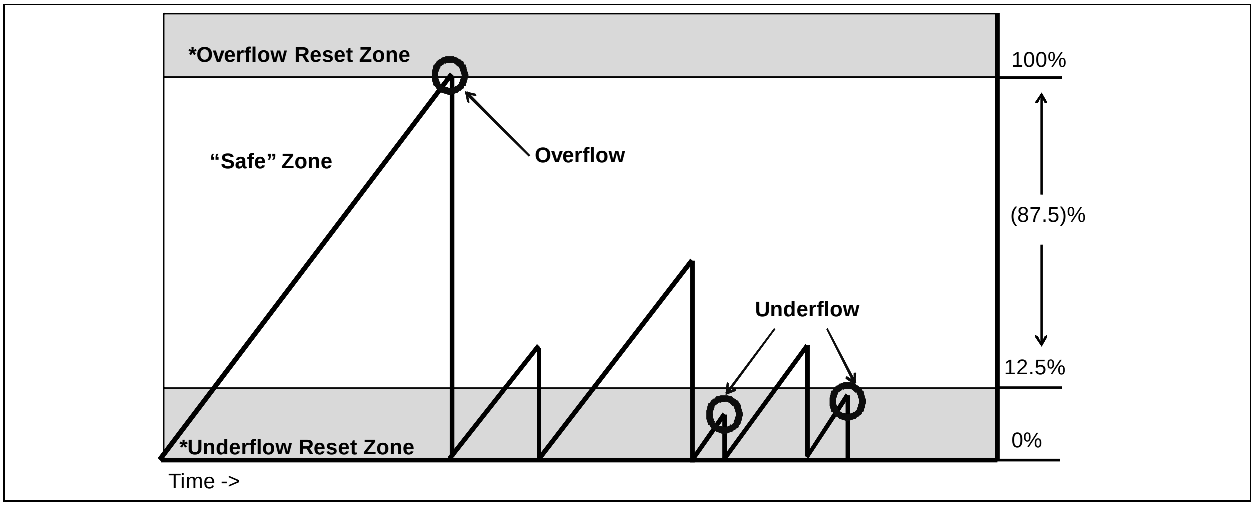


Figure 3 illustrates three cases of Overflow Reset and Underflow Reset conditions:

- Case 1: an Overflow Reset has occurred because of the WWDT time-out. If the `CLRWDT` instruction is not executed during the WWDT window open duration, Overflow Reset occurs. The zone above the WWDT period is the Overflow Reset zone.
- Case 2 and case 3: Underflow Resets have occurred triggered by the watchdog window violation (i.e., the execution of the `CLRWDT` instruction was done during the WWDT window closed duration).

The WWDT can be used in safety critical applications or in real-time applications such as the ones listed below:

1. Software execution is stuck or stalled.
2. The CPU main loop execution is too fast because of resource lock by threads, for example circular deadlock or blocked child threads
3. Real-time functions, where one has to locate the source of the problem, for example in diagnostic functions for peripherals or critical system functions – Watchdog Reset (underflow) occurs soon after entering the function or it does not reset the watchdog (overflow).
4. Class B security standard implementation – the WWDT can be used for time slot monitoring as mentioned in the H.2.18.10.4 standard of the IEC60730. Some scenarios are given below:
   a) Volatile memory testing with CRC and nonvolatile memory destructive testing, where every test takes a predetermined amount of time which can be tested with WWDT's window setting.
   b) Interrupt testing for timers, CPU registers and program counter
   c) The $\overline{\text{WDTWV}}$ bit in PCON will reset if WWDT window violation occurs. The bit in the STATUS register and the bit in the PCON register will reset if WWDT overflows. These bits can be checked after the program restarts for Fail conditions of class B test.

In all the above-mentioned scenarios, the WWDT can be used to reset the system as an ultimate Fail-Safe tool or for failure recovery.

## HOW TO CONFIGURE THE PERIPHERAL

The WWDT Configuration Special Function registers and Configuration Words are given in **Appendix A: "WWDT Registers"**.

The code in Example 1 is an illustration for configuring the WWDT.

### EXAMPLE 1:

```
WDTCON0bits.WDTPS  = 0b01011  //WWDT set for 2s interval, upper limit
WDTCON0bits.SEN    = 1        //WWDT is enabled
WDTCON1bits.WDTCS  = 0b000    //LFINTOSC at 31 kHz as clock source for WWDT
WDTCON1bits.WINDOW = 0b000    //WWDT lower time limit for WWDT window is set for last 12.5% of 2s
```

The WDTPS bits select the upper-time limit or threshold for the WWDT rollover. The SEN bit is a Software Enable bit for the WWDT. The WDTCS bit selects the clock source for the WWDT. The WINDOW bits select the percent of time of the total interval or upper-time limit threshold for which the WWDT timer clear window will open (i.e., the `CLRWDT` instruction can be issued).

The WWDT can also be configured using the Configuration bits of the CONFIG3 register shown in Table A-2. The WWDT modes explained in Table 1 are present in the WDTE<1:0> bits of the CONFIG3 register. The user application can use the WDTCON registers to program WWDT in software only if the WDTE is set to '`01`,' (i.e., the WWDT is controlled by software). If WDTE is set to any other modes, the bit setting of WDTCON has no effect on the WWDT and will work according to the bit settings in CONFIG.

## DEPENDENCY ON OTHER PERIPHERALS

The WWDT is not directly dependent on any on-chip peripheral other than the internal oscillator. The WWDT uses the Low-Frequency Internal Oscillator (LFINTOSC) for counting, and the system clock is used for execution of the `CLRWDT` instruction, which clears the WWDT. The tolerance of LFINTOSC and accuracy of the system clock will have a direct impact on the precision of the WWDT. Refer to each device specific data sheet for the tolerance value of LFINTOSC and the system clock.

## CONCLUSION

This technical brief explains the difference between the WDT and WWDT operation illustrating its different uses in applications. The code snippet for the configuration of the WWDT and the register definitions are also provided in this technical brief. The WWDT peripheral is very useful for applications as an ultimate Fail-Safe function and failure recovery, especially when real-time applications can benefit from this feature. It can also be used in safety critical applications and diagnostic testing such as Class B testing as explained in IEC 60730.

 

## APPENDIX A: WWDT REGISTERS

Table A-1 lists the registers used to set the WWDT and Table A-2 lists the Configuration bits.

### TABLE A-1: SPECIAL FUNCTION REGISTERS SUMMARY FOR WWDT

| Reg Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| OSCCON | SPLLEN | IRCF<3:0> | | | | — | SCS<1:0> | |
| PCON | STKOVF | STKUNF | $\overline{\text{WDTWV}}$ | $\overline{\text{RWDT}}$ | $\overline{\text{RMCLR}}$ | $\overline{\text{RI}}$ | $\overline{\text{POR}}$ | $\overline{\text{BOR}}$ |
| STATUS | — | — | — | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | Z | DC | C |
| WDTCON0 | — | — | WDTPS<4:0> | | | | | SEN |
| WDTCON1 | — | WDTCS<2:0> | | | — | WINDOW<2:0> | | |
| WDTPSL | PSCNT<7:0> | | | | | | | |
| WDTPSH | PSCNT<15:8> | | | | | | | |
| WDTTMR | — | WDTTMR<4:0> | | | | STATE | PSCNT<17:16> | |

### TABLE A-2: WWDT CONFIGURATION BITS

| Config. Reg | Bits | Bit -/7 | Bit -/6 | Bit 13/5 | Bit 12/4 | Bit 11/3 | Bit 10/2 | Bit 9/1 | Bit 8/0 |
|---|---|---|---|---|---|---|---|---|---|
| CONFIG 1 | 13:8 | — | — | — | — | $\overline{\text{CLKOUTEN}}$ | BOREN<1:0> | | — |
| | 7:0 | $\overline{\text{CP}}$ | MCLRE | $\overline{\text{PWRTE}}$ | — | — | — | FOSC<1:0> | |
| CONFIG 3 | 13:8 | — | — | WDTCCS<2:0> | | | WDTCWS<2:0> | | |
| | 7:0 | — | WDTE<1:0> | | WDTCPS<4:0> | | | | |

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