Atmel AVR32847: Migration from/to the UC3L0 64/32/16 from/to the UC3L0 256/128

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32-bit Atmel Microcontrollers

Application Note

Features

- Features comparison
- · Porting considerations and tools
- Pinout comparison

1 Introduction

This application note is a guide to assist Atmel[®] AT32UC3L0 64/32/16 devices users in converting existing designs to the Atmel AT32UC3L0 256/128 devices and vice versa.

For detailed information on these products; please refer to the datasheets available on the Atmel website.



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2 Features comparison

Atmel AT32UC3L0 64/32/16 and AT32UC3L0 256/128 share the same features set, except for a few features that the AT32UC3L0 256/128 extends.

Table 2-1. Feature differences between the AT32UC3L0 64/32/16 and 256/128 devices.

Feature	AT32UC3L0 64/32/16	AT32UC3L0 256/128		
Flash size	64/32/16kB	256/128kB		
Flash page size	256 bytes	512 bytes		
PLL	No	Yes (PLL0)		
PDCA: number of channels	12	16		
Number of generic clock	6	10		

3 Pinout comparison

AT32UC3L0 64/32/16 devices and AT32UC3L0 256/128 devices are pin-to-pin compatible.

4 Porting considerations

There are three major items to consider when migrating from one device to another:

- Device differences
- Software design for compatibility
- · Support of the devices in the tools

4.1 Device porting considerations and software design

4.1.1 Hardware module versions

For each hardware module, the parameter register (PR) and version registers (VR) may differ from one device to another, for example:

- On Atmel AT32UC3L0 64/32/16 FLASHCDW revision is 1.0.2(.0)
 - FLASHC.VFR = 0x102
 - FLASHC.FVR = 0x305
- On Atmel AT32UC3L0 256/128 FLASHCDW revision is 1.2.0(.0)
 - o FLASHC.VFR = 0x120
 - o FLASHC.FVR = 0x409

<u>Conditions for a successful migration</u>: Review all source code that was relying on module parameter and version register values.

4.1.2 Flash - page size

- The AT32UC3L0 64/32/16 flash page (FLASH_W) size is 256 bytes
- The AT32UC3L0 256/128 flash page (FLASH_W) size is 512 bytes

<u>Conditions for a successful migration</u>: Review all source code that was relying on a hard coded page size value. Use the toolchain flash page size definition: AVR®32_FLASHCDW_PAGE_SIZE to design portable software.

4.1.3 Flash - serial number

- Each AT32UC3L0 64/32/16 has a unique 120 bits serial number readable from address 0x80800284 to 0x80800292
- Each AT32UC3L0 256/128 has a unique 120 bits serial number readable from address 0x8080020C to 0x8080021A

<u>Conditions for a successful migration</u>: Use the correct device address when accessing the flash serial number.

4.1.4 ADCIFB

The time constant of the sample on hold formula in ADC (ADCIFB) ACR (ADC configuration register) register on AT32UC3L0 256/128 is 2, but on AT32UC3L0 64/32/16 the time constant is 3.

- AT32UC3L0 256/128: TSAMPLE&HOLD= (SHTIM+2) x TCLK ADC
- AT32UC3L0 64/32/16: TSAMPLE&HOLD= (SHTIM+3) x TCLK_ADC

<u>Conditions for a successful migration</u>: Use the correct sample on hold formula depending on the device used.





4.1.5 Frequency meter (FREQM)

The FREQM clock sources for clock measurement (CLK_MSR) 15:17 on the Atmel AT32UC3L0 64/32/16 are now clock 19:21 on the Atmel AT32UC3L0 56/128.

Table 4-1. Clock sources for CLK_MSR register.

CLKSEL on AT32UC3L0 256/128	CLKSEL on AT32UC3L0 256/128	Clock / Oscillator	Description
19	15	RC120M AW clock	Output clock from RC120M to AW
20	16	RC120M	Output clock from RC120M to main clock mux
21	17	RC32K	Output clock from RC32K

<u>Conditions for a successful migration</u>: Refer to the FREQM module configuration section in the datasheet for a full description of the clock sources for CLK_MSR and use the toolchain FREQM definitions: AVR32_FREQM_RC120M, AVR32_FREQM_RC32K, AVR32_FREQM_RC120M_AW.

4.1.6 Peripheral DMA controller (PDCA)

- The AT32UC3L0 64/32/16 devices have 12 PDCA channels
- The AT32UC3L0 256/128 devices have 16 PDCA channels

<u>Conditions for a successful migration</u>: Use only 12 channels on AT32UC3L0 256/128 devices if a migration to the AT32UC3L0 64/32/16 is planned.

4.1.7 System control interface (SCIF) - PLL

The phase locked loop (PLL) feature is only present on the AT32UC3L0 256/128 devices.

 $\underline{\text{Conditions for a successful migration}}\text{: Do not use the PLL on AT32UC3L0 256/128 devices if a migration to the AT32UC3L0 64/32/16 is planned.}$

4.1.8 System control interface (SCIF) – generic clock

There are six generic clocks on the AT32UC3L0 64/32/16 and 10 on the AT32UC3L0 256/128.

<u>Conditions for a successful migration</u>: Use maximum six generic clocks on the AT32UC3L0 256/128 if a migration to the AT32UC3L0 64/32/16 is planned.

4.1.9 Boot loader configuration

The UART boot loader uses two words in the flash user page to store its configuration:

- On AT32UC3L0 64/32/16:
 - o Configuration word 1 at address 0x808000FC
 - Configuration word 2 at address 0x808000F8
- On AT32UC3L0 256/128:
 - Configuration word 1 at address 0x808001FC
 - o Configuration word 2 at address 0x808001F8

<u>Conditions for a successful migration</u>: Refer to the device datasheet, Section Flash, sub section Module Configuration: Boot loader configuration and make sure the boot loader configuration words are used at the correct addresses.

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4.1.10 Electrical characteristics

Power consumptions in active and different sleep modes are slightly higher on Atmel AT32UC3L0 256/128 compared to the Atmel AT32UC3L0 64/32/16 devices.

<u>Conditions for a successful migration</u>: Refer to each device datasheet, Section Electrical Characteristic and make sure the application is properly designed. When porting from AT32UC3L0 64/32/16 to 256/128, keep a safety buffer in the power budget. When porting from the AT32UC3L0 256/128 to 64/32/16, there is nothing to mention.

4.1.11 Errata

Errata list is device revision specific.

<u>Conditions for a successful migration</u>: Refer to each device datasheet; Section Errata to make sure the application is properly designed.

4.2 Tools considerations

Selecting the correct part number in tools will affect:

- Device header files: The register address map will adjust to your part number
- Linker file: The flash and RAM memory map
- Interrupt map, GPIO alternate feature map

4.2.1 IAR Embedded Workbench®

In project properties:

- General options -> Target -> Device: Select the correct UC3L0 part number (uc3l0{256,128,64,32,16})
- Linker -> Config: If a specific linker file is specified (overriding default settings), make sure that the proper device one is selected

4.2.2 AVR Studio[®] 5

In project properties:

- Device: Select the correct UC3L0 part number (AT32UC3L0 256/128/64/32/16})
- Toolchain -> AVR32/GNU C Linker -> Miscellaneous: If a specific linker file is specified, make sure that the proper device one is selected

4.2.3 Standalone Makefile/GNU Toolchain

Using standalone makefile / config.mk: Open the associated config.mk and check the following parameter:

- PART = uc3l0 256/128/64/32/16 adjust the correct part number
- FLASH = internal@0x80000000,xKb: adjust the correct flash size
- INC_PATH (include path), CSRCS (list of C files) and ASRCS (list of assembly files) variables should be adjusted to match the part driver
- LINKER_SCRIPT: Adjust the correct linker script path if needed





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