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Application Note

SimpliPHY™ Fast Link Fail Indication

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

There were no changes to the technical content in revision 2.0 of this document.

1.2 Revision 1.1

In revision 1.1 of this document, referenced part numbers were updated.

1.3 Revision 1.0

Revision 1.0 was the first release of this document. It was published in 2016.

2 SimpliPHY™ Fast Link Fail Indication

This document explains the problem when using PHY link status for indicating link fail for applications requiring redundancy. Microsemi presents a solution for faster link fail indication by making use of the PMA descrambler lock state for 100BASE-TX and 1000BASE-T ("Fast Link Failover"). The solution described in this document is valid for all Microsemi PHYs and for all Microsemi switches with integrated 10/100/1000BASE-T PHYs, and supports fiber modes for FastLinkFail pin and extended LED outputs.

2.1 Problem Description

Ethernet is widely used in different areas including certain industrial and telecom applications where ensuring Ethernet communication is not interrupted is critical. Typically, in these applications, key Ethernet links are being monitored all the time to ensure that a link is not broken. When a link failure occurs, it should be detected quickly so that follow up actions can be applied immediately.
Ethernet link failure is normally detected on copper PHYs by monitoring the PHY link status bit, which is available for copper PHYs in all speeds through IEEE 802.3 standard register 1.2. However, this link status bit is sufficient for fast link fail indication only for 10BASE-T, and sometimes 100BASE-TX. The PHY link status bit is not sufficient for 1000BASE-T applications in practical use. The primary issue is it takes up to 750 ms for a 1000BASE-T PHY to indicate link failure after a 1000BASE-T PHY loses its receiving signal. The 750 ms requirement is part of the IEEE standard.
According to IEEE 802.3 Clause 0.4.6, all 1000BASE-T PHYs should comply with the following described behaviors after a loss of receiving signal.

- For a 1000BASE-T port configured as Master:

1. Start maxwait_timer. No PCS link state change can take place.
2. Before maxwait_timer expires, the PHY continuously transmits IDLEs.
3. After maxwait_timer expires, PHY link state changes from LINK UP to LINK DOWN by setting link_status to FAIL.

- For a 1000BASE-T port configured as Slave:

1. Start maxwait_timer. No PCS link state change can take place.
2. Before maxwait_timer expires, the PHY keeps in SILENT.
3. After maxwait_timer expires, PHY link state changes from LINK UP to LINK DOWN by setting link_status to FAIL.

So, in either case, the time required for the PCS link status bit to indicate a link failure is actually determined by maxwait_timer which is defined in IEEE 802.3 to be 750 ±10 ms for Master and 350 ±10 ms for Slave ports. This is the reason why link status can take up to 750 ms.

- For all links except 1000BASE-T, the fast link failure indication matches the link status register (address 1, bit 2). For 1000BASE-T links, the link failure is based on a circuit that will analyze the integrity of the link and, at the indication of failure, will assert.
- For new devices with Energy Efficient Ethernet (IEEE 802.3az) support, EEE goes quiet for up to 24 mS; therefore, it is not possible to detect link failure in less than 24 mS under all situations. Furthermore, for EEE, if the cable is unplugged, it will sometimes detect going quiet and require the full 24 mS before it can detect that the link has truly dropped. This applies to both 1000BASE-T EEE and 100BASE-TX EEE. For 100BASE-TX EEE, the quiet time is permitted to be up to 26 mS.

2.2 Microsemi PHY Solution

Instead of using the link status bit as the link fail indication, Microsemi Ethernet PHYs offer an alternate technique to reduce link fail indication time by making use of the PMA descrambler lock state. Data scrambling is used by 100BASE-TX and 1000BASE-T PMA to randomize the sequence of transmitted symbols and avoid the presence of spectral lines in the signal spectrum. Synchronization of the scrambler and descrambler of connected PHYs is required prior to PCS operation. So the descrambler lock loss event always takes place prior to the PCS link status determination to indicate link down. PHYs are not required by the standard to display this information to the user.

Fortunately, the descrambler lock-loss status is visible to users with all Microsemi Ethernet PHYs through register 26.7. That makes it possible for a much faster Ethernet link fail indication for 100BASE-TX, 1000BASE-T, and 100BASE-FX operating modes. For 10BASE-T rates, using PCS link status to indicate link failure already has sufficient performance, so there is no need to seek faster indication for 10BASE-T.

In newer devices, Microsemi has taken additional steps to simply Fast Link Failover indication management for users by providing a dedicated FastLinkFail pin selectable from GPIO. The FastLinkFail pin adds the ability to detect link failures in 1000BASE-X mode and can be dynamically assigned to a specific port by the user by setting Register 19G.

Furthermore, on the most recent PHY designs, Microsemi has provided a means of indicating link failures on any LED pin of a device (for any ports on such device). In 1000BASE-T, the FastLinkFail pin and extended LED will assert when a remote receiver-status is signaled as going low from the link partner. The 100BASE-TX has no such remote receiver status signaling. A summary of options for different devices is shown in the following table.

Table 1 • Available Options within Microsemi PHYs

Microsemi Product: 10 /100/1000BT	Monitoring PHY via Link Status Bit	Monitoring Status of Register 26.7	Monitoring with FastLinkFail Pin	Extended LED Functionality
All PHYs	Yes. 750 ± 10 ms for Master and 350 ± 10 ms for Slave port	Yes, except 1000BASEX mode. <1 mS accuracy (3 mS worst-case without EEE; 26 mS worst-case with EEE)	No	No
VSC8634, VSC8662, VSC8664	Yes. 750 ± 10 ms for Master and 350 ± 10 ms for Slave port	Yes, except 1000BASEX mode. <1 mS accuracy (3 mS worst-case without EEE; 26 mS worst-case with EEE)	Yes. <1 mS accuracy (3 mS worst-case without EEE; 26 mS worst-case with EEE)	No
VSC8512, VSC8522, VSC8552, VSC8504, VSC8572, VSC8574, VSC8564, VSC8575, VSC8582, VSC8582-10, VSC8584, VSC8584-10	Yes. 750 ± 10 ms for Master and 350 ± 10 ms for Slave port	Yes, except 1000BASEX mode. <1 mS accuracy (3 mS worst-case without EEE; 26 mS worst-case with EEE)	Yes. <1 mS accuracy (3 mS worst-case without EEE; 26 mS worst-case with EEE)	Yes

2.2.1 Solution 1: Monitoring Status of Register 26.7

Implementing the fast link fail indication depends on whether the PHY hardware interrupt pin is enabled.

2.2.1.1 Hardware Interrupt Pin Enabled

If the PHY's interrupt pin is enabled when a descrambler lock-loss event occurs, the hardware interrupt pin will be triggered. The interrupt service routine then should check register 26.7. The following is an example of what should be done if the hardware interrupt pin is enabled.

```
Phy_write 25 0x8080;
/* Enable PHY interrupt pin and enable descrambler lock-loss interrupt
mask. This should be done only once during PHY initialization*/
If ((Phy_read 26) & 0x0080 == 1)
Action(Link_Fail);
Else if((Phy_read 1) & 0x0004 == 0)
Action(Link_Fail);
Else return;

/* This should be done in the interrupt service routine for checking the monitored
ports (a port should be link-up to become a monitored port). The Register 26.7
assertion indicates descrambler lock-loss occurs for 100BASE-TX and 1000BASE-T, which
implies link drop is about to take place. Proper actions (for example failover to
backup link) should be taken. For 10BASE-T, PCS link status should be checked. */
```

2.2.1.2 Hardware Interrupt Pin Disabled

If the PHY's interrupt pin is not enabled, register 26.7 should be continuously polled. The following is an example of what should be done by software.

```
Phy_write 25 0x0080;
/* Enable descrambler lock-loss interrupt mask. This should be done only
once during PHY initialization */
If ((Phy_read 26) & 0x0080 == 1)
Action(Link_Fail);
Else if((Phy_read 1) & 0x0004 == 0)
Action(Link_Fail);
Else return;
/* This is a periodic software task checking the monitored ports (a port should be
linkup to become a monitored port) periodically. Register 26.7 assertion indicates
descrambler lock-loss occurs for 100BASE-TX and 1000BASE-T that implies link drop is
about to take place. Proper actions (for example failover to backup link) should be
taken. For 10BASE-T, PCS link status should be checked. */
```

2.2.1.3 Test Result

In Microsemi's lab, the link fail indication time has been tested to be approximately 165 us (microseconds) for 1000BASE-T by adopting the above described technique.

2.2.2 Solution 2: Monitoring FastLinkFailure Pin

2.2.2.1 FastLinkFail Pin

The FastLinkFail/GPIO9 pin serves as the main indicator for a fast link failure. To enable fast link failure indication, set PHY0 register 19E bit 4 to 1 (0 is the default, which sets GPIO9 for general purpose I/O use instead). Set the applicable PHY port in register 19G, bits 1:0. When a link on the selected port is failing, the GPIO9 pin asserts high and remains high until the link is re-established, or until register 19G.1:0 in the GPIO register space is changed to a PHY port with an established link.

> Register 19G in the GPIO register space controls the output of the fast link failure. The following table shows the settings available for the GPIO9 pin when enabled in PHY0 by register 19E, bit 4. See the datasheet for specific device values, as example, for VSC8664:

Table 2 • GPIO Input/Output Configuration, Address 19G (0x13)

Bit	Name	Access	Description	Default
3:0	Fast link failure port setting	R/W	Select fast link failure PHY source 00: PHY0 01: PHY1 10: PHY2 11: PHY3	00

For VSC8664, a quad port device, bits 3:2 default to ‘11’, which disables the FastLinkFail pin use on PHY ports that do not exist on the VSC8664. Similarly, for VSC8512, a 12-port PHY, where there are 12 PHY ports and the PHY selection uses bits 3:0 associated with PHY0 to PHY11.

2.2.3 Solution 3: Serial Management Interface Interrupts

The fast link failure indication is also available on the serial management interface interrupt pins (MDINTn) for each PHY port. To enable this function, set register 25 bit 7 to 1 (this is the Fast link failure interrupt mask sticky bit in the Interrupt Mask register with default set to 0). The MDINT pins assert if register 26, bit 7 is set to 1 (this is the fast link failure detect status self-clearing bit in the Interrupt Status register with default set to 0), and the pins clear once register 26 is read.

2.3 Summary

Microsemi’s Fast Failover Indication feature is a piece of the solution required to achieve effective redundancy in 10/100/1000BASE-T systems by providing less than 1 mS notification of a potential link fail. The solution described in this document is valid for all Microsemi PHYs and for all Microsemi switches with integrated 10/100/1000BASE-T PHYs.

Microsemi provides other technologies for applications requiring redundancy, for example: a Ring Resiliency technology that enables one to change the timing master/slave relationship without drop of link in 1000BASE-T systems, and protection switching in L2 switch products.

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