

AC423
Application Note
SmartFusion 2 SoC FPGA and IGLOO 2 FPGA
Ethernet Solutions



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 6.0

- Added a note under [Table 2](#), page 4.

1.2 Revision 5.0

- Updated [Figure 3](#), page 9.

1.3 Revision 4.0

The following is a summary of the changes made in revision 4.0 of this document.

- Information about the two versions of the CoreTSE IP was added. For more information, see [SmartFusion 2 and IGLOO 2 Ethernet IP Core Support](#), page 3.
- Information about GMII connections through the CoreSGMII IP was added. For more information, see [RJ45 Connections Through GMII](#), page 9.

1.4 Revision 3.0

The document title was updated.

1.5 Revision 2.0

The document was updated for SAR 60856.

1.6 Revision 1.0

Revision 1.0 was the first publication of this document.

2 SmartFusion 2 SoC FPGA and IGLOO 2 FPGA Ethernet Solutions

Microchip SmartFusion®2 SoC FPGAs and IGLOO®2 FPGAs provide a complete range of solutions to use with IEEE 802.3 standard-compliant Ethernet ports for chip-to-chip, board-to-board, or backplane interconnects. The device's features and soft fabric IP blocks offer solutions for use within embedded systems or for networking over copper or fiber-optic media. The solutions reduce design risk and shorten development times for Ethernet design applications.

The high-speed serial interface (SERDESIF) of SmartFusion 2 and IGLOO 2 devices supports IEEE 802.3 GbE physical medium attachment (PMA) layers of the protocol. The SerDes supports IEEE 802.3 1000Base-X (1GbE) PMA layer of the protocol and SGMII specifications. These integrate with soft IP, enabling complete protocols implemented in a single device for handling the data link layer and Ethernet frame creation.

This application note highlights the Ethernet features, interfaces, and modes supported by the SmartFusion 2 and IGLOO 2 families. It provides block diagrams to describe the connections required inside and outside the device to support Ethernet data rates ranging from 10M/100M up to 10G.

2.1 Introduction

SmartFusion 2 SoC FPGA integrates fourth-generation flash-based FPGA fabric, an ARM Cortex-M3 processor, and high-performance communication interfaces on a single-chip.

The microcontroller subsystem (MSS) of the SmartFusion 2 device has an instance of the triple-speed Ethernet (TSE) MAC peripheral. The MSS MAC can be configured to support the following data transfer rates (line speeds) between the SmartFusion 2 device and the Ethernet Network.

- 10 Mbps
- 100 Mbps
- 1000 Mbps

For more information about the MSS MAC, see the [SmartFusion2 Microcontroller Subsystem User Guide](#).

SmartFusion 2 SoC FPGA supports 10-Gbps attachment unit interface (XAUI) using the XAUI extender block inside the SERDESIF block. For more information about XAUI SERDESIF, see the [SmartFusion2 and IGLOO2 High-Speed Serial Interfaces User Guide](#).

The Core10100 and CoreTSE MAC IP cores run in the FPGA fabric to support 10/100 Mbps and 10/100/1000 Mbps Ethernet speeds, respectively, in SmartFusion 2 and IGLOO 2 devices.

In SmartFusion 2 devices, Ethernet functionality is achieved by using either the embedded MSS Ethernet MAC or the Core10100/CoreTSE MAC IP core, an Ethernet PHY, and standard Ethernet interfaces (MII/RMII/GMII/ RGMII/SGMII/1000BASE-X XAUI).

IGLOO 2 devices do not include an embedded MAC. In IGLOO 2 devices, Ethernet functionality is achieved by using the Core10100 or CoreTSE MAC IP core, an Ethernet PHY, and standard Ethernet interfaces (such as GMII/SGMII, 1000BASE-X, and XAUI). For more information about IGLOO 2 FPGA products, see <https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas>.

2.2 SmartFusion 2 and IGLOO 2 Hardware Kit Support

The following table lists SmartFusion 2 and IGLOO 2 hardware kits that support Ethernet interfaces.

Table 1 • Hardware Kits

Kit Name	Version
SmartFusion 2 Starter Kit. For more information, see the SmartFusion2 Starter Kit Guide .	Version 1A
SmartFusion 2 Development Kit. For more information, see the SmartFusion2 Development Kit Quickstart Guide .	Rev C or later
SmartFusion 2 Evaluation Kit. For more information, see the SmartFusion2 Security Evaluation Kit User Guide .	Rev C
IGLOO 2 evaluation Kit. For more information, see the IGLOO2 FPGA Evaluation Kit User Guide .	Rev C
SmartFusion 2 Advanced Development Kit. For more information, see UG0557: SmartFusion2 SoC FPGA Advanced Development Kit User Guide .	Rev A

2.3 SmartFusion 2 and IGLOO 2 Ethernet IP Core Support

IP cores included in the Microchip IP Catalog are pre-designed and verified to be used in Ethernet interface solutions. Some of the Ethernet IP cores, listed in this section, function independently to provide the complete Ethernet PHY and MAC functionality. Others work in collaboration with SmartFusion 2 MSS MAC to provide a solution.

Microchip provides the following IP cores for Ethernet Solutions.

CoreTSE (Optional PHY + MAC IP Core)

CoreTSE is a soft IP core that is implemented in the FPGA Fabric to achieve 10/100/1000 Mbps Ethernet speeds. CoreTSE provides a physical layer interface of either ten-bit interface (TBI) or GMII. CoreTSE is available in Libero® SoC SmartDesign IP catalog.

The CoreTSE IP is available in two versions:

- CoreTSE_AHB: Designed for AMBA AHB applications; uses the AHB interface for both transmit and receive paths.
- CoreTSE: Designed for wire-speed store-and-forward throughput (non-AMBA AHB applications); accesses the MAC directly using a streaming packet interface.

For more information, see the *CoreTSE Handbook* and *CoreTSE_AHB Handbook* from Libero SoC SmartDesign IP catalog.

Core10100 (MAC IP Core)

Core10100 is a MAC that supports 10/100 Mbps Ethernet traffic. Core10100 MAC supports an MII/RMII physical layer interface, and is a soft IP core that is available from Libero SoC SmartDesign IP catalog. For more information, see *Core10100 Handbook* from Libero SoC SmartDesign IP catalog.

Note: If the application requires two MACs, Core10100 MAC can be used in conjunction with the SmartFusion 2 embedded MSS MAC to provide the required functionality.

CoreRMII

CoreRMII provides an interface to convert standard media independent interface (MII) signals to reduced MII (RMII). The 16-signal MII is converted into six-signal RMII to achieve 10/100 Mbps Ethernet speed. This soft IP works in conjunction with the SmartFusion 2 embedded MSS MAC. For more information, see *CoreRMII Handbook* from Libero SoC SmartDesign IP catalog.

CoreRGMII

CoreRGMII provides an interface to convert standard gigabit MII (GMII) signals to reduced GMII (RGMII). The 24-signal GMII is converted into 12-signal RMII to achieve 10/100/1000 Mbps Ethernet speed. This soft IP works in conjunction with the SmartFusion 2 embedded MSS MAC. For more information, go to Microchip website [Microchip FPGAs and PLDs website](#).

10 Gigabit Ethernet Soft IP

Microchip does not provide a 10Gbps Ethernet MAC soft IP core. A licensed third-party 10-gigabit Ethernet soft IP core is required in the FPGA fabric to act as MAC to control the XAUI interface and handle 10-Gbps Ethernet traffic.

IP cores are accessed through the Libero suite of development tools available in the SmartDesign IP catalog. For a list of available Microchip IP Cores, see [Microchip FPGAs and PLDs website](#).

2.4 SmartFusion 2 MSS MAC Supported Features

The following table provides details about the Ethernet interfaces supported by SmartFusion 2 MSS MAC.

Notes:

- CoreRMII or CoreRGMII soft IP core is required in addition to the MSS MAC to achieve RMII, RGMII, and SGMII functionality in SmartFusion 2 devices.
- The SERDESIF block required for SGMII support in the MSS MAC requires the use of the high-speed serial interface configurator GUI in Libero, as well as the Libero SoC System Builder. For more information about SGMII support with the SmartFusion 2 SERDESIF block, see the [SmartFusion2 and IGLOO2 High-Speed Serial Interfaces User Guide](#).

Table 2 • SmartFusion 2 MSS MAC Ethernet Interface Support

Interface	Ethernet MAC and Additional IP Core(s) Required	Ethernet Mode Supported	SmartFusion 2 Board Support	Y/N
MII	MSS MAC	10/100BASE-T	Starter Kit	Yes
			Development Kit	Yes
			Evaluation Kit	Yes
			Advanced Development Kit	Yes
RMII	MSS MAC + CoreRMII	10/100BASE-T	Starter Kit	Yes
			Development Kit	Yes
			Evaluation Kit	Yes
			Advanced Development Kit	Yes
GMII	MSS MAC	10/100/1000BASE-T	Starter Kit	No
			Development Kit	Yes
			Evaluation Kit	Yes
			Advanced Development Kit	Yes
RGMII	MSS MAC + CoreRGMII	10/100/1000BASE-T	Starter Kit	No
			Development Kit	Yes
			Evaluation Kit	Yes
			Advanced Development Kit	Yes

Table 2 • SmartFusion 2 MSS MAC Ethernet Interface Support (continued)

Interface	Ethernet MAC and Additional IP Core(s) Required	Ethernet Mode Supported	SmartFusion 2 Board Support	Y/N
SGMII	MSS MAC + SERDESIF	10/100/1000BASE-T	Starter Kit	No
			Development Kit	Yes
			Evaluation Kit	Yes
			Advanced Development Kit	Yes

Note: MSS Ethernet MAC does not support full 1000 Mbps bandwidth in real-time applications. Best throughput results can be achieved by placing the MAC Transmit and Receive buffers into the eSRAM, enabling the cache controller, and configuring the processor clock to the maximum.

2.5 SmartFusion 2 and IGLOO 2 XAUI Mode Supported Features

The SmartFusion 2 device supports the XAUI interface for 10-Gbps Ethernet speed. The SmartFusion 2 MSS MAC supports only 10/100/1000 Mbps Ethernet speed. However, a third-party licensed 10-Gigabit Ethernet soft IP core can be used in SmartFusion 2 or IGLOO 2 FPGA fabric to achieve 10-Gbps Ethernet speed over the XAUI interface.

The following table provides details about SmartFusion 2 and IGLOO 2 board support for XAUI SERDESIF.

Table 3 • SmartFusion 2 XAUI SERDESIF Support

Interface	IP Core(s) Required	Ethernet Mode Supported	SmartFusion 2/IGLOO 2 Board Support	Y/N
XAUI	10-Gigabit Ethernet Soft IP + SERDESIF	10GBASE-T	SmartFusion 2 Starter Kit	No
			SmartFusion 2 Development Kit	Yes
			SmartFusion 2 Evaluation Kit	No
			SmartFusion 2 Advanced Development Kit	Yes
XAUI	10-Gigabit Ethernet Soft IP + SERDESIF	10GBASE-T	IGLOO 2 Evaluation Kit	No

The SERDESIF block required for XAUI support in the MSS block requires the use of the high-speed serial interfaces configurator GUI in Libero, as well as the Libero SoC System Builder. For more information about XAUI support with the SmartFusion 2/IGLOO 2 SERDESIF block, see the [SmartFusion2 and IGLOO2 High-Speed Serial Interfaces User Guide](#).

2.6 SmartFusion 2 and IGLOO 2 CoreTSE MAC (IP Core) Supported Features

The following table provides details about the CoreTSE MAC IP core, including supported Ethernet interfaces, Ethernet speeds, and hardware boards.

Table 4 • SmartFusion 2/IGLOO 2 CoreTSE MAC (IP Core) Support

Interface	IP Core(s) Required	Ethernet Mode Supported	SmartFusion 2/IGLOO 2 Board Support	Y/N
GMII	CoreTSE	10/100/1000BASE-T	SmartFusion 2 Starter Kit	No
			SmartFusion 2 Development Kit	Yes
			SmartFusion 2 Evaluation Kit	Yes
			SmartFusion 2 Advanced Development Kit	Yes
SGMII	CoreTSE+ SERDESIF	10/100/1000BASE-T	SmartFusion 2 Starter Kit	No
			SmartFusion 2 Development Kit	Yes
			SmartFusion 2 Evaluation Kit	Yes
			SmartFusion 2 Advanced Development Kit	Yes
SGMII	CoreTSE+ SERDESIF	10/100/1000BASE-T	IGLOO 2 Evaluation Kit	Yes

The SERDESIF block required for SGMII support in the CoreTSE MAC requires the use of the high-speed serial interfaces configurator GUI in Libero, as well as the Libero SoC System Builder. For more information on SGMII support with the SmartFusion 2/IGLOO 2 SERDESIF block, see the [SmartFusion2 and IGLOO2 High-Speed Serial Interfaces User Guide](#).

2.7 SmartFusion 2 and IGLOO 2 Core10100 MAC (IP Core) Supported Features

The following table provides details about the SmartFusion 2 and IGLOO 2 Core10100 MAC IP core, including supported Ethernet interfaces, Ethernet modes, and hardware boards.

Table 5 • SmartFusion 2 Core10100 MAC (IP Core) Support

Interface	IP Core Required	Ethernet Mode Supported	SmartFusion 2/IGLOO 2 Board Support	Y/N
MII	Core10100	10/100BASE-T	SmartFusion 2 Starter Kit	Yes
			SmartFusion 2 Development Kit	Yes
			SmartFusion 2 Evaluation Kit	Yes
			SmartFusion 2 Advanced Development Kit	Yes
RMII	Core10100	10/100BASE-T	SmartFusion 2 Starter Kit	No
			SmartFusion 2 Development Kit	Yes
			SmartFusion 2 Evaluation Kit	Yes
			SmartFusion 2 Advanced Development Kit	Yes
MII/RMII	Core10100	10/100BASE-T	IGLOO 2 Evaluation Kit	Yes

2.8 SmartFusion 2 and IGLOO 2 Hardware Evaluation Kit Ethernet PHY, RJ45, and SFP Support

The following table provides details about PHY, RJ45, and small form-factor pluggable (SFP) module support in SmartFusion 2 and IGLOO 2 hardware kits.

Table 6 • SmartFusion 2 and IGLOO 2 Hardware Kits PHY, RJ45, and SFP Module Support

SmartFusion 2/IGLOO 2 Board	Built-in Ethernet PHY	Ethernet Mode Supported	RJ45 Support	SFP Support
SmartFusion 2 Starter Kit	KSZ8051MNL1	10/100BASE-T	Yes	No
SmartFusion 2 Development Kit	M88E1340S	10/100/1000BASE-T	Yes	Yes
SmartFusion 2 Evaluation Kit	M88E1340S	10/100/1000BASE-T	Yes	No
SmartFusion 2 Advanced Development Kit	M88E1340S	10/100/1000BASE-T	Yes	No
IGLOO 2 Evaluation Kit	M88E1340S	10/100/1000BASE-T	Yes	No

2.9 SmartFusion 2 and IGLOO 2 Ethernet Features Block Diagrams

This section describes how to use the Ethernet features available in SmartFusion 2 and IGLOO 2 devices to interface the MAC with the PHY. It provides block diagrams for various types of connections.

Note: The external devices referenced in these diagrams have been used on evaluation kits and are recommended for use in Ethernet solutions. Sample schematics can be found in the user guides associated with the evaluation kits.

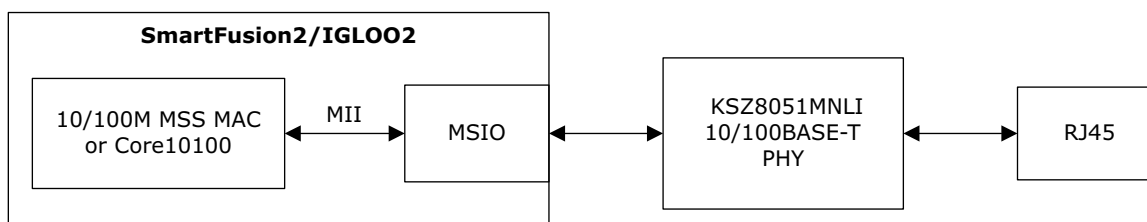
2.9.1 10M/100M Ethernet

This section provides information about connections for the MII and RMII interfaces, which support 10M/100M Ethernet.

2.9.1.1 RJ45 Connection through MII

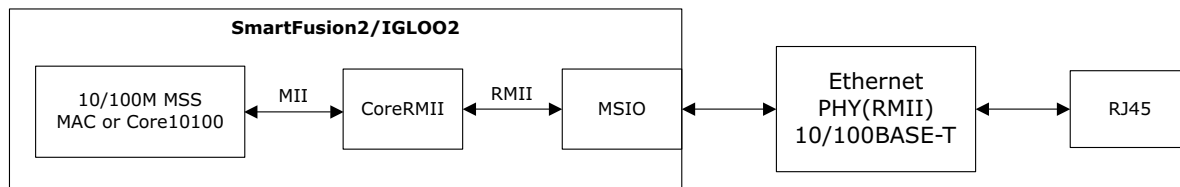
An RJ45 connector is connected to the SmartFusion 2 MSS MAC or the Core10100 IP through Micrel Ethernet PHY KSZ8051MNL1 through the MII interface to achieve 10/100 Mbps Ethernet speed, as shown in the following figure.

Figure 1 • RJ45 Connections Through MII



2.9.1.2 RJ45 Connection through RMII

As shown in the following figure, an RJ45 connector is connected to the SmartFusion 2 MSS MAC or the Core10100 IP through an external PHY through the RMII interface to achieve 10/100 Mbps Ethernet speed.

Figure 2 • RJ45 Connections Through RMII

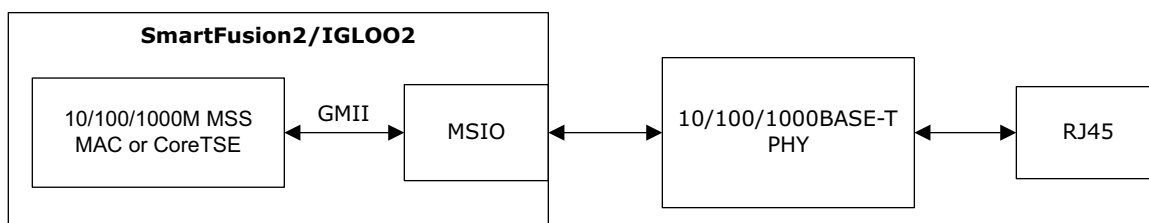
2.9.2 10M/100M/1000M Ethernet

This section provides information about connections for the GMII, RGMII, and SGMII interfaces, which support 10M/100M/1000M Ethernet.

2.9.2.1 RJ45 Connections Through GMII

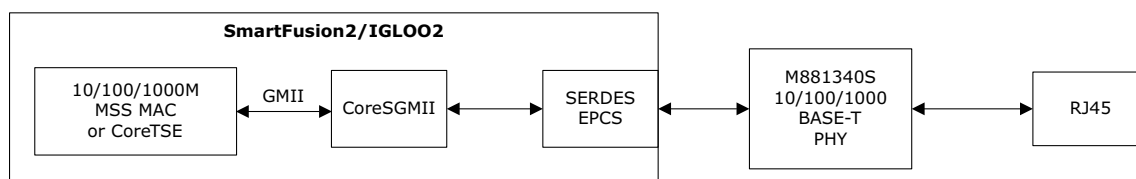
As shown in the following figure, an RJ45 connector is connected to the SmartFusion 2 MSS MAC or the CoreTSE IP through GMII-compatible Ethernet PHY using the GMII interface to achieve 10/100/1000 Mbps Ethernet speed.

Figure 3 • RJ45 Connections Through GMII



As shown in the following figure, an RJ45 connector is connected to the SmartFusion 2 MSS MAC or the CoreTSE IP through SGMII-compatible Ethernet PHY using the CoreSGMII IP to achieve 10/100/1000 Mbps Ethernet speed.

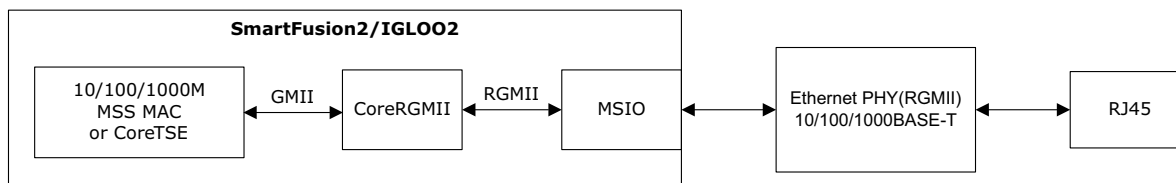
Figure 4 • RJ45 Connections Through CoreSGMII



2.9.2.2 RJ45 Connections Through RGMII

As shown in the following figure, an RJ45 connector is connected to the SmartFusion 2 MSS MAC or the CoreTSE IP through an RGMII-compatible Ethernet PHY using the RGMII interface to achieve 10/100/1000 Mbps Ethernet speed.

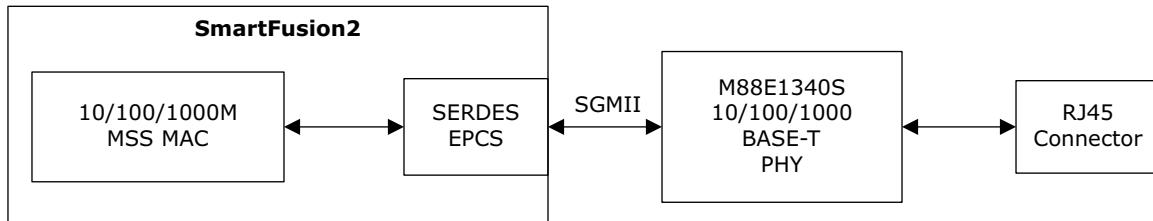
Figure 5 • RJ45 Connections Through RGMII



2.9.2.3 RJ45 Connections Through SGMII

As shown in the following figure, an RJ45 connector is connected to the SmartFusion 2 MSS MAC through Marvell Ethernet PHY(88E1340S) using the SGMII interface to achieve 10/100/1000 Mbps Ethernet speed.

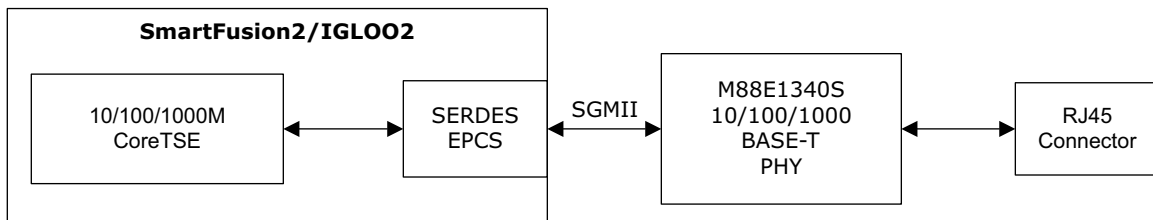
Figure 6 • RJ45 Connections Through SGMII with MSS MAC



Note: This diagram is SmartFusion2 specific.

As shown in the following figure, an RJ45 connector is connected to CoreTSE MAC through Marvell Ethernet PHY88E1340S through the SGMII interface to achieve 10/100/1000 Mbps Ethernet speed.

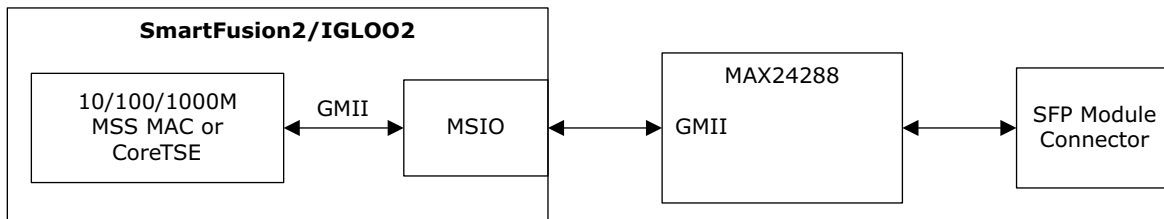
Figure 7 • RJ45 Connections Through SGMII with CoreTSE MAC



2.9.2.4 SFP Connections Through SGMII/1000BASE-X

As shown in the following figure, an SFP module is connected through a MAX24288 chip configured for GMII mode to achieve 10/100/1000 Mbps Ethernet speed over SFP.

Figure 8 • SFP Connections Through MAX24288 Chip



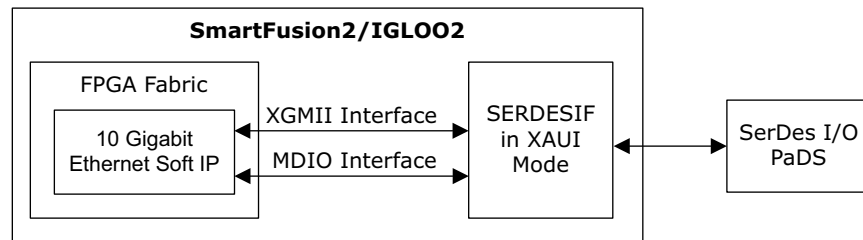
2.9.3 10G Ethernet

This section provides information about connections for the XAUI interface, which supports 10G Ethernet.

2.9.3.1 XAUI High-Speed Serial Interface

As shown in the following figure, 10-Gbps high-speed traffic over the XAUI interface is supported by using a gigabit Ethernet soft IP in the FPGA fabric and by configuring the SERDESIF block in XAUI mode.

Figure 9 • XAUI External PHY Connection

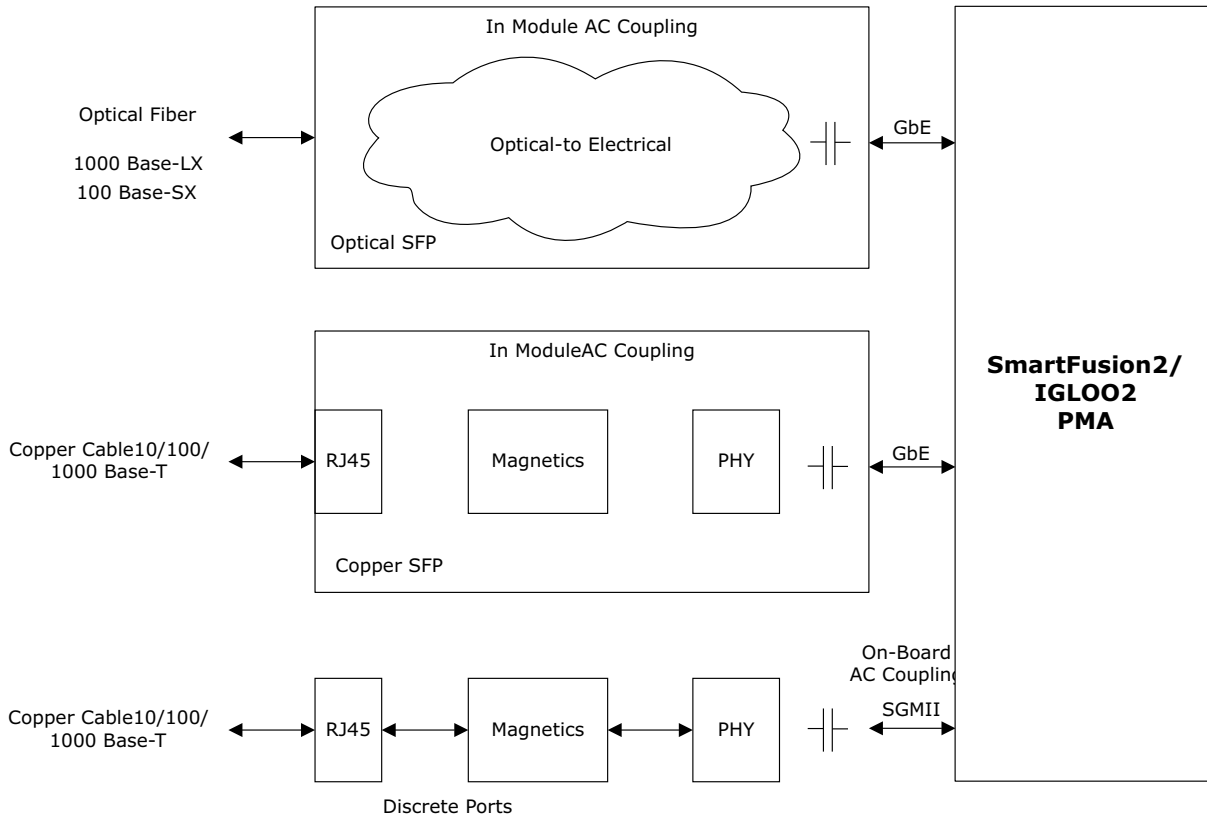


3 Appendix: Ethernet Interface with RJ45/SFP

The SERDESIF SGMII interface does not directly interface with 10Base-T (10 Mb over unshielded twisted pair copper cable), 100Base-T (100 Mb over copper), and 1000Base-T (1 Gb over copper) networks. Therefore, devices need an external 10/100/1000Base-T standard PHY device to connect to the Ethernet copper cable. The external PHY handles the physical signals, such as working mode, duplex, and negotiation signals.

The following figure is the block diagram of the Ethernet interface with an RJ45 or SFP connector.

Figure 10 • Ethernet Interface with RJ45/SFP



RJ45 connectors are used for copper cable physical transport layer, or 1000BASE-T. This interface requires a PHY device to inter-operate and to re-time the interface.

1000-BASE-X is an optical-fiber interface physical transport layer, and RJ45 connectors are not used with optical fiber.

4 Glossary

MAC

Media access control

The Ethernet media access control (MAC) is a sub-level within the data link layer of the OSI reference model. The Ethernet MAC is defined by the IEEE-802.3 Ethernet standard. The hardware that implements the MAC is referred to as a medium access controller.

PHY

Physical interface transceiver

The IEEE-802.3 standard defines the Ethernet PHY. It implements the physical layer. An instantiation of PHY connects a link layer device (often called MAC) to a physical medium such as an optical fiber or copper cable.

MII

Media Independent Interface

MII, defined in IEEE Std 802.3-2005, clause 22, is a parallel interface that connects a 10/100 Mbps-capable MAC to the PHY.

RMII

Reduced Media Independent Interface

RMII is a standard developed to reduce the number of signals required in MII to connect a 10/100 Mbps capable MAC to PHY.

GMII

Gigabit Media Independent Interface

GMII, defined in IEEE Std 802.3-2005, clause 35, is an extension of MII used to connect a 10/100/1000 Mbps-capable MAC to the PHY.

RGMII

Reduced Gigabit Media Independent Interface

RGMII is a standard developed to reduce the number of signals required in GMII interface to connect a 10/100/1000Mbps-capable MAC to PHY.

SGMII

Serial Gigabit Media Independent Interface

SGMII, a variant of MII, is a standard interface used to connect a 10/100/1000 Mbps-capable Ethernet MAC to a PHY. See [Appendix: Ethernet Interface with RJ45/SFP](#), page 12 to know more about SGMII Interface with RJ45/SFP connectors.

XAUI

10-Gigabit Attachment Unit Interface

XAUI is a standard interface for extending the XGMII (10-Gigabit Media Independent Interface) between the MAC and PHY layer of 10-Gigabit Ethernet (10GbE). It supports 10 Gbps Ethernet Speed.

RJ45

Registered jack

RJ45 is a type of connector commonly used for Ethernet networking. It is used to transmit or receive data from Ethernet PHY over the Ethernet Cable.

SFP

Small form-factor pluggable

The small form-factor pluggable (SFP) connector is a compact, hot-pluggable transceiver (transmitter/receiver in a single package) used to carry data over optical or copper wires.