MICROCHIP

Section 55. Charge Time Measurement Unit (CTMU)

HIGHLIGHTS

This section of the manual contains the following major topics:

> **Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.
>
> Please consult the note at the beginning of the **"Charge Time Measurement Unit (CTMU)"** chapter in the current device data sheet to check whether this document supports the device you are using.
>
> Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

55.1 INTRODUCTION

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides accurate differential time measurement between pulse sources and asynchronous pulse generation. By working with other on-chip analog modules, the CTMU can be used to precisely measure time, capacitance, relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

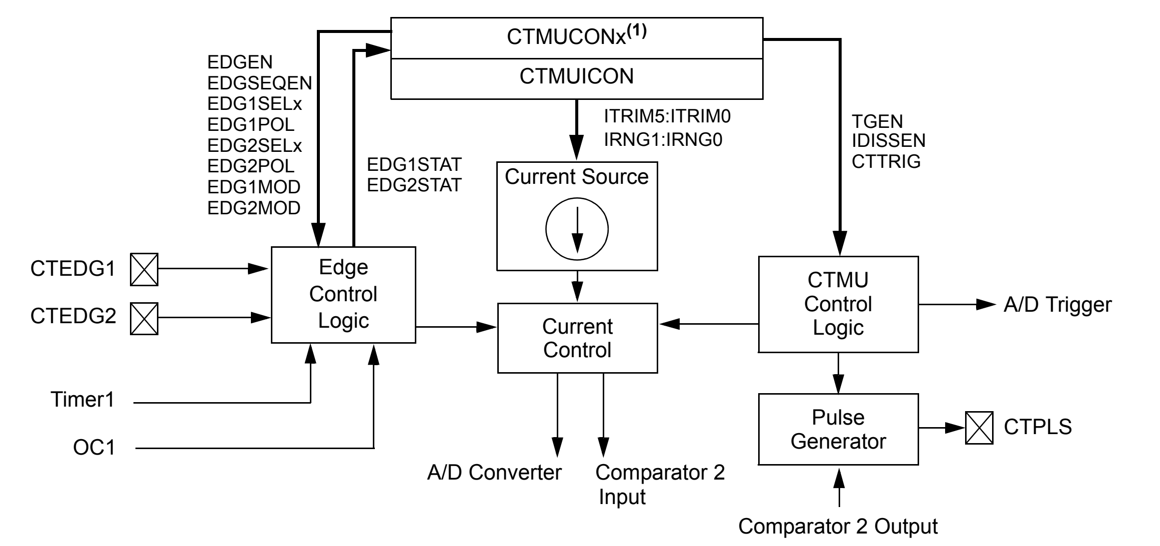
The CTMU module includes the following key features:

- Up to 16 channels available for capacitive or time measurement input
- On-chip precision current source
- Four-edge input trigger sources
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock

The CTMU works in conjunction with the A/D Converter to provide up to 16 channels for time or charge measurement, depending on the specific device and the number of A/D channels available. When configured for time delay, the CTMU is connected to one of the analog comparators. The level-sensitive input edge sources can be selected from four sources: two external inputs, Timer1 or Output Compare Module 1. For device-specific information on available input sources, refer to the appropriate dsPIC33F/PIC24H data sheet.

A block diagram of the CTMU is illustrated in Figure 55-1.

Figure 55-1: CTMU Block Diagram



Note 1: Refer to the specific device data sheet to determine which registers are available on your particular device.

55.2 REGISTERS

Depending on the device variant there are up to three control registers available for the CTMU: CMTUCON1, CTMUCON2, and CTMUICON.

The CTMUCON1 and CTMUCON2 registers (Register 55-1 and Register 55-2) contain control bits for configuring the CTMU module edge source selection, edge source polarity selection, edge sequencing, A/D trigger, analog circuit capacitor discharge and enables. The CTMUICON register (Register 55-3) has bits for selecting the current source range and current source trim.

Register 55-1: CTMUCON1: CTMU Control Register 1(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CTMUSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 10 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: Refer to the specific device data sheet to determine whether this register is available on your particular device.

Register 55-2: CTMUCON2: CTMU Control Register 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
EDG1MOD	EDG1POL	EDG1SEL<3:0>(1)				EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL<3:0>(1)				—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Input mode selection bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 programmed for a positive level response
0 = Edge 1 programmed for a negative level response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits(1)
1111 = Edge 1 Source 15 selected
1110 = Edge 1 Source 14 selected
1101 = Edge 1 Source 13 selected
1100 = Edge 1 Source 12 selected
1011 = Edge 1 Source 11 selected
1010 = Edge 1 Source 10 selected
1001 = Edge 1 Source 9 selected
1000 = Edge 1 Source 8 selected
0111 = Edge 1 Source 7 selected
0110 = Edge 1 Source 6 selected
0101 = Edge 1 Source 5 selected
0100 = Edge 1 Source 4 selected
0011 = Edge 1 Source 3 selected
0010 = Edge 1 Source 2 selected
0001 = Edge 1 Source 1 selected
0000 = Edge 1 Source 0 selected

bit 9 **EDG2STAT:** Edge 2 Status bit
1 = Edge 2 event has occurred
0 = Edge 2 event has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
1 = Edge 1 event has occurred
0 = Edge 1 event has not occurred

bit 7 **EDG2MOD:** Input Mode Selection bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 programmed for a positive level response
0 = Edge 2 programmed for a negative level response

Note 1: Refer to the particular device data sheet for specific edge source types and assignments.

Register 55-2: CTMUCON2: CTMU Control Register (Continued)2

bit 5-2	**EDG2SEL<3:0>:** Edge 2 Source Select bits(1) `11` = Edge 2 Source 3 selected `10` = Edge 2 Source 2 selected `01` = Edge 2 Source 1 selected `00` = Edge 2 Source 0 selected
bit 1-0	**Unimplemented:** Read as '`0`'

Note 1: Refer to the particular device data sheet for specific edge source types and assignments.

Register 55-3: CTMUICON: CTMU Current Control Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM<5:0>						IRNG<1:0>	
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **ITRIM<5:0>:** Current Source Trim bits

`011111` = Maximum positive change from nominal current
`011110`
•
•
•
`000001` = Minimum positive change from nominal current
`000000` = Nominal current output specified by IRNG1:IRNG0
`111111` = Minimum negative change from nominal current
•
•
•
`100010`
`100001` = Maximum negative change from nominal current

bit 9-8 **IRNG<1:0>:** Current Source Range Select bits

`11` = 100 × base current
`10` = 10 × base current
`01` = Base current level (0.55 μA nominal)
`00` = Current source disabled or 1000 × base current(1)

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: Refer to the specific device data sheet to determine which setting is available on your particular device.

55.3 CTMU OPERATION

The CTMU works by using a fixed current source to charge a circuit. The type of circuit depends on the type of measurement is made. In the case of charge measurement, the current and the amount of time the current is applied to the circuit is fixed. The amount of voltage read by the A/D is then a measurement of the capacitance of the circuit. In the case of time measurement, the current and the capacitance of the circuit is fixed. In this case, the voltage read by the A/D is then representative of the amount of time elapsed from the time the current source starts and stops charging the circuit.

If the CTMU is used as a time delay, both capacitance and current source are fixed, and the voltage supplied to the comparator circuit also fixed. The delay of a signal is determined by the amount of time it takes the voltage to charge to the comparator threshold voltage.

55.3.1 Theory of Operation

The operation of the CTMU is based on the equation for charge, as shown in Equation 1.

Equation 55-1:

$$I = C \cdot \frac{dV}{dT}$$

The amount of charge measured in coulombs in a circuit is defined as current in amperes (I) multiplied by the amount of time in seconds that the current flows (t). Charge is also defined as the capacitance in farads (C) multiplied by the voltage of the circuit (V), as shown in Equation.

Equation 55-2:

$$I \cdot t = C \cdot V$$

The CTMU module provides a constant current source. The A/D Converter is used to measure (V) in the equation, leaving two unknowns: capacitance (C) and time (t). Equation 55-2 can be used to calculate capacitance or time either using the known fixed capacitance of the circuit as shown in Equation 55-3 or using a fixed time that the current source is applied to the circuit as shown in Equation 55-4.

Equation 55-3:

$$t = \frac{(C \cdot V)}{I}$$

Equation 55-4:

$$C = \frac{(I \cdot t)}{V}$$

55.3.2 Current Source

At the heart of the CTMU is a precision current source, designed to provide a constant reference for measurements. The level of current is user-selectable across three ranges or a total of two orders of magnitude, with the ability to trim the output in ±2% increments (nominal). The current range is selected by the IRNG1:IRNG0 bits (CTMUICON<9:8>), with a value of '00' representing the lowest range.

Current trim is provided by the ITRIM5:ITRIM0 bits (CTMUICON<15:10>). These six bits allow trimming of the current source in steps of approximately 2% per step. The half of the range adjusts the current source positively and another half reduces the current source. A value of '000000' is the neutral position (no change). A value of '100000' is the maximum negative adjustment (approximately -62%), and '011111' is the maximum positive adjustment (approximately +62%).

55.3.3 Edge Selection and Control

CTMU measurements are controlled by edge events occurring on the module's two input channels. Each channel, referred to as Edge 1 and Edge 2, can be configured to receive input pulses from one of the edge input pins (CTEDG1 and CTEDG2), Timer1 or Output Compare Module 1. The input channels are level-sensitive, responding to the instantaneous level on the channel rather than a transition between levels. The inputs are selected using the EDG1SEL and EDG2SEL bit pairs (CTMUCON2<5:2> and <13:9>).

In addition to source, each channel can be configured for event polarity using the EDGE2POL and EDGE1POL bits (CTMUCON2<14:6>). The input channels can also be filtered for an edge event sequence (Edge 1 occurring before Edge 2) by setting the EDGSEQEN bit (CTMUCON1<10>).

55.3.4 Edge Status

The CTMUCON register also contains two status bits, EDG2STAT and EDG1STAT (CTMUCON2<9:8>). Their primary function is to show if an edge response has occurred on the corresponding channel. The CTMU automatically sets a bit when an edge response is detected on its channel. The level-sensitive nature of the input channels also means that the status bits become set immediately if the channel's configuration is changed and the input channels remain at their current state.

The module uses the edge status bits to control the current source output to external analog modules like A/D Converter. Current is supplied to external modules only when one (but not both) of the status bits is set, and shuts current off when both the bits are either set or cleared. This allows the CTMU to measure current only during the interval between edges. After both status bits are set, it is necessary to clear them before another measurement is taken. If possible, both the bits should be cleared simultaneously to avoid re-enabling the CTMU current source.

In addition to being set by the CTMU hardware, the edge status bits can also be set by software. This is also the user's application to manually enable or disable the current source. Setting either one (but not both) of the bits enables the current source. Setting or clearing both bits at once disables the source.

55.3.5 Interrupts

The CTMU sets its interrupt flag (IFS4<13>) whenever the current source is enabled and disabled. An interrupt is generated only if the corresponding interrupt enable bit (IEC4<13>) is also set. If edge sequencing is not enabled (that is Edge 1 must occur before Edge 2), it is necessary to monitor the edge status bits and determine which edge occurred last and caused the interrupt.

55.4 CTMU MODULE INITIALIZATION

The following sequence is a general guideline used to initialize the CTMU module:

1. Select the current source range using the IRNG bits (CTMUICON<9:8>).
2. Adjust the current source trim using the ITRIM bits (CTMUICON<15:10>).
3. Configure the edge input sources for Edge 1 and Edge 2 by setting the EDG1SEL and EDG2SEL bits (CTMUCON2<13:10> and <5:2>).
4. Configure the input polarities for the edge inputs using the EDG1POL and EDG2POL bits (CTMUCON2<14:6>). The default configuration is for negative edge polarity (high-to-low transitions).
5. Enable edge sequencing using the EDGSEQEN bit (CTMUCON1<10>). By default, edge sequencing is disabled.
6. Select the operating mode (Measurement or Time Delay) with the TGEN bit. The default mode is Time/Capacitance Measurement.
7. Configure the module to automatically trigger an A/D conversion when the second edge event has occurred using the CTTRIG bit (CTMUCON1<8>). The conversion trigger is disabled by default.
8. Discharge the connected circuit by setting the IDISSEN bit (CTMUCON1<9>); after waiting a sufficient time for the circuit to discharge, clear IDISSEN.
9. Disable the module by clearing the CTMUEN bit (CTMUCON1<15>).
10. Clear the Edge Status bits, EDG2STAT and EDG1STAT (CTMUCON2<9:8>).
11. Enable both edge inputs by setting the EDGEN bit (CTMUCON1<11>).
12. Enable the module by setting the CTMUEN bit.

Depending on the type of measurement or pulse generation being performed, one or more additional modules may also need to be initialized and configured with the CTMU module:

- Edge Source Generation: In addition to the external edge input pins, both Timer1 and the Output Compare/PWM1 module can be used as edge sources for the CTMU.
- Capacitance or Time Measurement: The CTMU module uses the A/D Converter to measure the voltage across a capacitor that is connected to one of the analog input channels.
- Pulse Generation: When generating system clock independent output pulses, the CTMU module uses Comparator 2 and the associated comparator voltage reference.

For specific information on initializing these modules, refer to the applicable dsPIC33F/PIC24H Family Reference chapter for the appropriate module.

55.5 CALIBRATING THE CTMU MODULE

The CTMU requires calibration for precise measurements of capacitance and time, and also for accurate time delay. If the application only requires measurement of a relative change in capacitance or time, calibration is usually not necessary. An example of this type of application would include a capacitive touch switch, in which the touch circuit has a baseline capacitance, and the added capacitance of the human body changes the overall capacitance of a circuit.

If actual capacitance or time measurement is required, two hardware calibrations must take place: the current source needs calibration to set it to a precise current, and the circuit being measured needs calibration to measure and/or nullify all other capacitance other than that to be measured.

55.5.1 Current Source Calibration

The current source onboard the CTMU module has a range of ±62% nominal for each of three current ranges. Therefore, for precise measurements, it is possible to measure and adjust this current source by placing a high precision resistor, R_{CAL}, on the analog channel AN2. An example circuit is illustrated in Figure 55-2. The current source measurement is performed using the following steps:

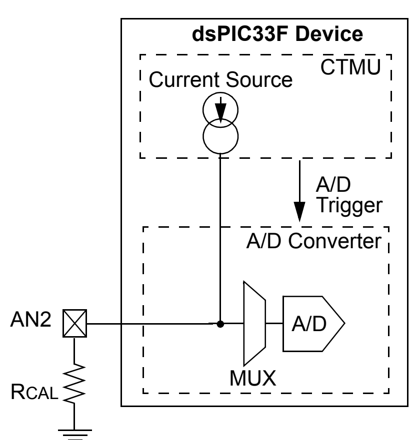
1. Initialize the A/D Converter.
2. Initialize the CTMU by configure the module for Pulse Generation mode (TGEN = `1`).
3. Enable the current source by setting EDG1STAT (CTMUCON1<8>).
4. Issue settling time delay.
5. Perform A/D conversion.
6. Calculate the current source current using $I = V/R_{CAL}$, where R_{CAL} is a high precision resistance and V is measured by performing an A/D conversion.

The CTMU current source may be trimmed with the trim bits in CTMUICON using an iterative process to get an exact desired current. Alternatively, the nominal value without adjustment may be used and it may be stored by the software for use in all subsequent capacitive or time measurements.

When the module is configured for pulse generation delay by setting the TGEN bit (CTMUCON1<12>), the internal current source is connected to one of the inputs of Comparator 2. Figure 55-2 illustrates the external connections for current source calibration and the relationship of the different analog modules required.

To calculate the value for R_{CAL}, the nominal current must be chosen, and then the resistance can be calculated. For example, if the A/D Converter reference voltage is 3.3V, use 70% of full scale, or 2.31V as the desired approximate voltage to be read by the A/D Converter. If the range of the CTMU current source is selected to be 0.55 µA, the resistor value needed is calculated as $R_{CAL} = 2.31\text{V}/0.55\ \mu\text{A}$, for a value of 4.2 MΩ. Similarly, if the current source is chosen to be 5.5 µA, R_{CAL} will be 420,000Ω, and 42,000Ω if the current source is set to 55 µA.

Figure 55-2: CTMU Current Source Calibration Circuit



Preliminary

A value of 70% full-scale voltage is chosen to ensure that the A/D Converter was in a range that is well above the noise floor. If an exact current is chosen that is to incorporate the trimming bits from CTMUICON, the resistor value of RCAL may need to be adjusted accordingly. RCAL may be adjusted to allow for available resistor values. RCAL should be of the highest precision available, the amount of precision required for the circuit that the CTMU will be used to measure. A recommended minimum precision will be 0.1% tolerance.

The following examples show a typical method for performing a CTMU current calibration. Example 55-1 shows how to initialize the A/D Converter and the CTMU; this routine is typical for the applications using both the modules. Example 55-2 shows one method for the actual calibration routine. This method manually triggers the A/D Converter and it is performed to demonstrate the entire stepwise process. It is also possible to automatically trigger the conversion by setting the CTTRIG bit (CTMUCON1<8>).

Example 55-1: Setup for CTMU Calibration Routines for Devices with CTMUCON1 and CTMUCON2 Registers

```
#include “p33Fxxxx.h”

/**************************************************************************/
/ Set up CTMU ************************************************************/
/**************************************************************************/

void setup(void)
{   //CTMUCON - CTMU Control register
        CTMUCON1 = 0x1000;     //make sure CTMU is disabled
        CTMUCON2 = 0xC0C0;
        // CTMU continues to run when emulator is stopped, CTMU continues
        // to run in idle mode, Time Generation mode enabled, Edges are
        // blocked. No edge sequence order, Analog current source not
        // grounded, trigger output disabled, Edge2 polarity = positive level,
        // Edge2 source = source 0, Edge1 polarity = positive level,
        // Edge1 source = source 0, Set Edge status bits to zero

    //CTMUICON - CTMU Current Control Register
        CTMUICON = 0x0100; // 0.55uA, Nominal - No Adjustment
/**************************************************************************/
/ Set up AD converter ****************************************************/
/**************************************************************************/
        TRISB = 0x0001;    // Set channel 2 as an input
        AD1PCFG = 0x0001;  //
        AD1CHS = 0x002;    // Select the analog channel(2)
        AD1CSSL = 0x0000;  //

        AD1CON1 = 0x8000;  // Turn On A/D Converter, continue in Idle mode,
                           // Unsigned fractional format, Clear SAMP bit to
                           // start conversion, Sample when SAMP bit is set,
                           // sampling on hold
        AD1CON2 = 0x0000;  // VR+ = AVDD, V- = AVSS, Don't scan,
                           // always use MUX A inputs
        AD1CON3 = 0x0000;  // A/D uses system clock, conversion clock = 1xTcy

}
```

Example 55-2: Current Calibration Routine for Devices With CTMUCON1 and CTMUCON2 Registers

```
#include "p33Fxxxx.h"

#define     COUNT   500        //@ 8MHz = 125uS.
#define     DELAY   for(i=0;i<COUNT;i++)
#define     RCAL    .027       //R value is 4200000 (4.2M)
                               //scaled so that result is in
                               //1/100th of uA
#define     ADSCALE 1023       //for unsigned conversion 10 sig bits
#define     ADREF   3.3        //Vdd connected to A/D Vr+

int main(void)
{
    int i;
    int j = 0;                           //index for loop
    unsigned int Vread = 0;
    double VTot = 0;
    float Vavg=0, Vcal=0, CTMUISrc = 0;  //float values stored for calcs

    //assume CTMU and A/D have been setup correctly
    //see Example 11-1 for CTMU & A/D setup
    setup();

    CTMUCON1bits.CTMUEN = 1;             //Enable the CTMU

    for(j=0;j<10;j++)
    {
        AD1CON1bits.SAMP = 1;            //Manual sampling start
        CTMUCON1bits.IDISSEN = 1;        //drain charge on the circuit
        DELAY;                           //wait 125us
        CTMUCON1bits.IDISSEN = 0;        //end drain of circuit

        CTMUCON2bits.EDG1STAT = 1;       //Begin charging the circuit
                                         //using CTMU current source
        DELAY;                           //wait for 125 us

        IFS0bits.AD1IF = 0;              //make sure A/D Int not set
        AD1CON1bits.SAMP = 0;            //and begin A/D conv.
        while(!IFS0bits.AD1IF);          //Wait for A/D convert complete
        AD1CON1bits.DONE = 0;
        CTMUCON2bits.EDG1STAT = 0;       //Stop charging circuit
        Vread = ADC1BUF0;                //Get the value from the A/D
        IFS0bits.AD1IF = 0;              //Clear A/D Interrupt Flag
        VTot += Vread;                   //Add the reading to the total

    }

        Vavg = (float)(VTot/10.000);     //Average of 10 readings
        Vcal = (float)(Vavg/ADSCALE*ADREF);
        CTMUISrc = Vcal/RCAL;            //CTMUISrc is in 1/100ths of uA
}
```


55.5.2 Capacitance Calibration

A small amount of capacitance from the internal A/D Converter sample capacitor and stray capacitance from the circuit board traces and pads that affect the precision of capacitance measurements. A measurement of the stray capacitance can be taken to ensure the desired capacitance to be measured is removed. The measurement is then performed using the following steps:

1. Initialize the A/D Converter and the CTMU.
2. Set EDG1STAT (= `1`).
3. Wait for a fixed delay of time t.
4. Clear EDG1STAT.
5. Perform an A/D conversion.
6. Calculate the stray and A/D sample capacitances using Equation 55-5.

Equation 55-5:

$$C_{OFFSET} = C_{STRAY} + C_{AD} = \frac{(I \cdot t)}{V}$$

where I is known from the current source measurement step, t is a fixed delay and V is measured by performing an A/D conversion.

This measured value is then stored and used for calculations of time measurement, or subtracted for capacitance measurement. For calibration, it is expected that the capacitance of $C_{STRAY} + C_{AD}$ is approximately known. C_{AD} is approximately 4 pF.

An iterative process must be used to adjust the time t, that the circuit is charged to obtain a reasonable voltage reading from the A/D Converter. The value of **t** may be determined by setting C_{OFFSET} to a theoretical value, then solving for t. For example, if C_{STRAY} is theoretically calculated to be 11 pF, and V is expected to be 70% of V_{DD}, or 2.31V, t would be equal to Equation 55-6 or 63 µs.

Equation 55-6: :

$$(4\ pF + 11\ pF) \bullet \frac{2.31V}{0.55\mu A}$$

A typical routine for CTMU capacitance calibration is shown in Example 55-3.

Example 55-3: Capacitance Calibration Routine for Devices With CTMUCON1 and CTMUCON2 Registers

```
#include “p33Fxxxx.h”

#define COUNT 25           //@ 8MHz INTFRC = 62.5 us.
#define ETIME COUNT*2.5    //time in uS
#define DELAY for(i=0;i<COUNT;i++)
#define ADSCALE 1023       //for unsigned conversion 10 sig bits
#define ADREF 3.3          //Vdd connected to A/D Vr+


int main(void)
{
    int i;
    int j = 0;             //index for loop
    unsigned int Vread = 0;
    float CTMUISrc, CTMUCap, Vavg, VTot, Vcal;

                           //assume CTMU and A/D have been setup correctly
                           //see Example 11-1 for CTMU & A/D setup
    setup();

    CTMUCON1bits.CTMUEN = 1;//Enable the CTMU

    for(j=0;j<10;j++)
    {
        AD1CON1bits.SAMP = 1;         //Manual sampling start
        CTMUCON1bits.IDISSEN= 1;      //drain any charge on the circuit
        DELAY;                        //wait 62.5 us
        CTMUCON1bits.IDISSEN = 0;     //end drain of circuit
        CTMUCON2bits.EDG1STAT = 1;    //Begin charging the circuit
                                      //using the CTMU current source
        DELAY;                        //wait for 62.5 us for circuit
                                      //to charge
        CTMUCON2bits.EDG1STAT = 0;    //Stop charging circuit and begin
                                      //A/D conversion
        AD1CON1bits.SAMP = 0;
        while(!IFS0bits.AD1IF);   //Wait for A/D conversion to complete
        Vread = ADC1BUF0;         //Get the value from the A/D converter
        IFS0bits.AD1IF = 0;       //Clear AD1IF
        VTot += Vread;            //Add the reading to the total
    }

    Vavg = (VTot/10); //Average of 10 readings
    Vcal = (Vavg/ADSCALE*ADREF);
    CTMUCap = (CTMUISrc*ETIME/Vcal)/100;
    //CTMUISrc is in 1/100ths of uA,
    //calculated in Example 1-2
    //time is in us
    //CTMUCap is in pF
}
```


55.6 MEASURING CAPACITANCE WITH THE CTMU

The two methods of measuring capacitance with the CTMU are:

- Absolute Capacitance Measurement: The actual capacitance value is required
- Relative Charge Measurement: The actual capacitance value is not required instead an indication of change in capacitance is required.

55.6.1 Absolute Capacitance Measurement

For absolute capacitance measurements, both the current and capacitance calibration steps found in **55.5 "Calibrating the CTMU Module"** should be followed. Capacitance measurements are then performed using the following steps:

1. Initialize the A/D Converter.
2. Initialize the CTMU.
3. Set EDG1STAT.
4. Wait for a fixed delay, T.
5. Clear EDG1STAT.
6. Perform an A/D conversion.
7. Calculate the total capacitance, $C_{TOTAL} = (I * T)/V$, where I is known from the current source measurement step (**55.5.1 "Current Source Calibration"**), T is a fixed delay and V is measured by performing an A/D conversion
8. Subtract the stray and A/D capacitance (C_{OFFSET} from **55.5.2 "Capacitance Calibration"**) from C_{TOTAL} to determine the measured capacitance.

55.6.2 Relative Charge Measurement

An application may not require precise capacitance measurements. For example, when detecting a valid press of a capacitance-based switch, detecting a relative change of capacitance is of interest. In this application, when the switch is open (or not touched), the total capacitance is the capacitance of the combination of the board traces, the A/D Converter, etc. A larger voltage will be measured by the A/D Converter. When the switch is closed (or is touched), the total capacitance is larger due to the addition of the capacitance of the human body to the above listed capacitances, and a smaller voltage will be measured by the A/D Converter.

Detecting capacitance changes can be done with the CTMU using these steps:

1. Initialize the A/D Converter and the CTMU
2. Set EDG1STAT
3. Wait for a fixed delay
4. Clear EDG1STAT
5. Perform an A/D conversion

The voltage measured by performing the A/D conversion is an indication of the relative capacitance. In this case, no calibration of the current source or circuit capacitance measurement is required. A sample software routine for a capacitive touch switch is shown in Example 55-4.

Example 55-4: Routine for Capacitive Touch Switch for Devices With CTMUCON1 and CTMUCON2 Registers

```
#include "p33Fxxxx.h"

#define     COUNT   500     //@ 8MHz = 125uS.
#define     DELAY   for(i=0;i<COUNT;i++)
#define     OPENSW  1000    //Unpressed switch value
#define     TRIP    300     //Difference between pressed
                            //and unpressed switch
#define     HYST    65      //amount to change
                            //from pressed to unpressed
#define     PRESSED 1
#define     UNPRESSED0

int main(void)
{
    unsigned int Vread;       //storage for reading
    unsigned int switchState;
    int i;

                              //assume CTMU and A/D have been setup correctly
                              //see Example 11-1 for CTMU & A/D setup
    setup();

    CTMUCON1bits.CTMUEN = 1;  //Enable the CTMU

    AD1CON1bits.SAMP = 1;     //Manual sampling start
    CTMUCON1bits.IDISSEN = 1; //drain charge on the circuit
    DELAY;                    //wait 125us
    CTMUCON1bits.IDISSEN = 0; //end drain of circuit

    CTMUCON2bits.EDG1STAT = 1;//Begin charging the circuit
                              //using CTMU current source
    DELAY;                    //wait for 125us
    CTMUCON2bits.EDG1STAT = 0;//Stop charging circuit

    IFS0bits.AD1IF = 0;       //make sure A/D Int not set
    AD1CON1bits.SAMP = 0;     //and begin A/D conv.
    while(!IFS0bits.AD1IF);   //Wait for A/D convert complete
    AD1CON1bits.DONE = 0;
    Vread = ADC1BUF0;         //Get the value from the A/D
    if(Vread < OPENSW - TRIP)
    {
        switchState = PRESSED;
    }
    else if(Vread > OPENSW - TRIP + HYST)
    {
        switchState = UNPRESSED;
    }

}
```

55.7 MEASURING TIME WITH THE CTMU MODULE

Time can be precisely measured after the ratio (C/I) is measured from the current and capacitance calibration step by following these steps:

1. Initialize the A/D Converter and the CTMU.
2. Set EDG1STAT.
3. Set EDG2STAT.
4. Perform an A/D conversion.
5. Calculate the time between edges as $T = (C/I) * V$, where I is calculated in the current calibration step (**55.5.1 "Current Source Calibration"**), C is calculated in the capacitance calibration step (**55.5.2 "Capacitance Calibration"**) and V is measured by performing the A/D conversion.

It is assumed that the time measured is small enough that the capacitance C_{OFFSET} provides a valid voltage to the A/D Converter. For the smallest time measurement, set the A/D Channel Select register (AD1CHS) to an unused A/D channel; the corresponding pin for which is not connected to any circuit board trace. This minimizes added stray capacitance by keeping the total circuit capacitance close to the A/D Converter (4-5 pF). To measure longer time intervals, an external capacitor may be connected to an A/D channel, and this channel is selected when making a time measurement.

55.8 CREATING A DELAY WITH THE CTMU MODULE

A unique feature of the CTMU module is to generate system clock independent output pulses based on an external capacitor value. This is accomplished using the internal comparator voltage reference module, Comparator 2 input pin and an external capacitor. The pulse is output onto the CTPLS pin. To enable this mode, you need to set the TGEN bit.

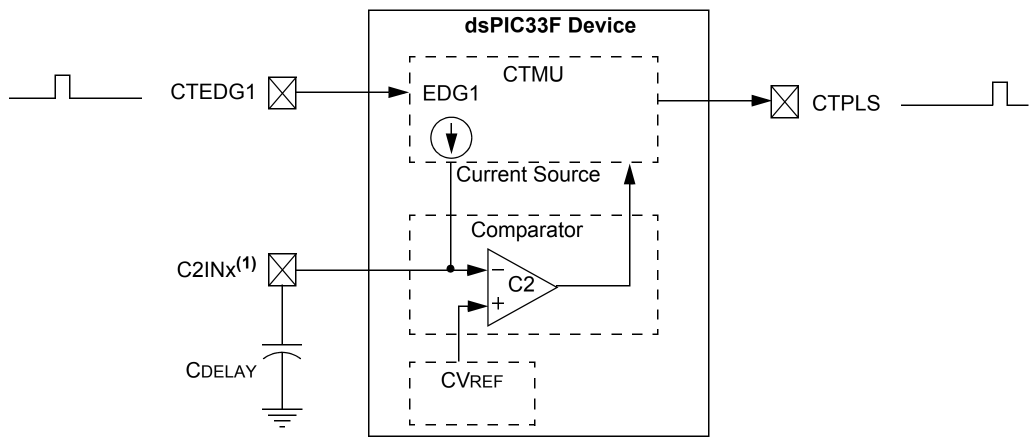
An example circuit is illustrated in Figure 55-3. C_{PULSE} is chosen by the user to determine the output pulse width on CTPLS. The pulse width is calculated by $T = (C_{PULSE}/I) * V$, where I is known from the current source measurement step (**55.5.1 "Current Source Calibration"**) and V is the internal reference voltage (CV_{REF}).

An example use of this feature is for interfacing with variable capacitive-based sensors like a humidity sensor. As the humidity varies, the pulse-width output on CTPLS will vary. The CTPLS output pin can be connected to an input capture pin and the varying pulse width is measured to determine the humidity in the application.

Follow these steps to use this feature:

1. Initialize Comparator 2.
2. Initialize the comparator voltage reference.
3. Initialize the CTMU and enable time delay generation by setting the TGEN bit.
4. Set EDG1STAT.
5. When C_{PULSE} charges to the value of the voltage reference trip point, an output pulse is generated on CTPLS.

Figure 55-3: Typical Connections and Internal Configuration for Pulse Delay Generation



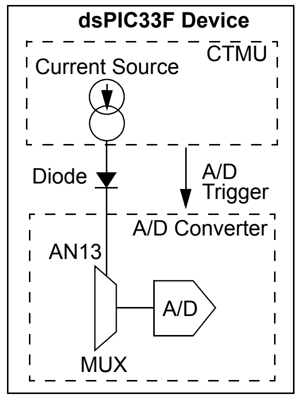
Note 1: Refer to the specific device data sheet for information related to the comparator input used in this mode.

55.9 MEASURING ON-CHIP TEMPERATURE WITH THE CTMU

The CTMU module can be used to measure the internal temperature of the device through an internal diode that is available for such purposes. When EDGE1 is not equal to EDGE2 and TGEN = 0, the current is steered into the temperature sensing diode. The voltage across the diode is available as an input to the ADC module (AN13).

Figure 55-4 illustrates how this module can be used for temperature measurement. As the temperature rises, the voltage across the diode will drop by about 300 mV over a 150ºC range. Selecting a higher current drive strength will raise the voltage value by a few 100 mV.

Figure 55-4: CTMU Temperature Measurement Circuit



At 25ºC, the forward voltage of the temperature diode is 0.83V. The rate of change between the forward voltage of the diode and its temperature is 1.87 mV per degree Celsius. The formula shown in Equation 55-7 can be used to calculate the forward voltage.

Equation 55-7: Voltage versus Temperature

$$Vf\,(\text{in mV}) = 783.24mV + 1.87mV \cdot T$$

Where:

Vf = Forward voltage of temperature diode

T = Temperature in degrees Celsius

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Charge Time Measurement Unit (CTMU)

55.10 OPERATION DURING SLEEP OR IDLE MODE

55.10.1 Sleep Mode and Deep Sleep Modes

When the device enters any Sleep mode, the CTMU module current source is always disabled. If the CTMU is performing an operation that depends on the current source when Sleep mode is invoked, the operation may not terminate correctly. Capacitance and time measurements may return erroneous values.

55.10.2 Idle Mode

The behavior of the CTMU in Idle mode is determined by the CTMUSIDL bit (CTMUCON1<13>). If CTMUSIDL is cleared, the module will continue to operate in Idle mode. If CTMUSIDL is set, the CTMU module's current source is disabled when the device enters Idle mode. If the CTMU module is performing an operation when Idle mode is invoked, the results will be similar to those with Sleep mode.

55.11 EFFECTS OF A RESET ON CTMU

Upon Reset, all registers of the CTMU are cleared. This leaves the CTMU module disabled, its current source is turned off and all configuration options return to their default settings. The module needs to be re-initialized following any Reset.

If the CTMU is in the process of taking a measurement at the time of Reset, the measurement will be lost. A partial charge may exist on the circuit that was being measured, and should be properly discharged before the CTMU makes subsequent attempts to make a measurement. The circuit is discharged by setting and then clearing the IDISSEN bit (CTMUCON1<9>) while the A/D Converter is connected to the appropriate channel.

55.12 REGISTER MAPS

A summary of the registers associated with the dsPIC33F/PIC24H CTMU is given in Table 55-1.

Table 55-1: CTMU Register Map

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1(1)	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2(1)	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
CTMUICON	ITRIM<5:0>						IRNG<1:0>		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Refer to the specific device data sheet to determine whether this register is available on your particular device.

55.13 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the CTMU module are:

Title	**Application Note #**
No related application notes are available.	N/A

Note:	Visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33F/PIC24H family of devices.

55.14 REVISION HISTORY

Revision A (June 2010)

This is the initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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