PLC Performance Validation

AN4914

Introduction

The purpose of this document is to explain how to validate the physical performance of a hybrid PLC product using Microchip platforms, devices, or products. It also describes several tests, including the hardware and software, defined for this validation.

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Table of Contents

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1. Overview

Microchip provides a set of PLC reference designs which passes all required certifications and performance tests to ensure a successful field deployment.

This application note describes how to perform these tasks:

- Check the performance of a prototype at PHY layer level.
- Compare the performance of the prototype to Microchip PLC reference designs.
- Adjust the PHY layer configuration of the PLC modem to improve the performance.

By analyzing and comparing the behavior of the physical layer of the HW prototype with the behavior of Microchip PLC reference designs, customers can increase the confidence in their designs.

This application note is valid for any G3-PLC or PRIME design regardless of the communication frequency band.

Important:
This application note describes some tests to evaluate the G3-PLC or PRIME PHY performance of any prototype based on any Microchip PLC reference design.

For G3-PLC: In any case, these tests cannot replace the *Performance Test Suite for G3-PLC Device Certification* and *G3-PLC Conformance Tests Suite Specification* defined by the G3-PLC Alliance nor ensure that they will be passed. They are only the first step to pass them.

For PRIME: In any case, these tests cannot replace the *PRIME Certification TestBooks* defined by the PRIME Alliance nor ensure that they will be passed. They are only the first step to pass them.

Final PLC products may comply with additional normative or specifications depending on the legal terms of the end purpose. Describing the complete set of specifications to comply by the final product is out of scope of this document.

Attention: Microchip strongly recommends following the PLC design guidelines available together with the following documents:

- PLC Hardware Design Guidelines
- Crystal Selection Guidelines

This document describes a method to evaluate the PHY performance of any PLC design where a calibration process was already carried out. The main goal of the device calibration is to adapt the PLC transmission to be compliant in G3-PLC with section 2 of the Performance Test Suite for G3-PLC Device Certification and in PRIME with the *Electrical Specification* section of the 6. DUT must be EN50065-1 /-2 /-3 /-7 compliant.

The features required by the standards to be complied are the following:

- Section 6.3.1.2 of EN50065 standard. TX power < 134 dBμV over CISPR 16-1 LISN (impedance around 50Ω).
- Section 2.1 of G3-PLC device certification. A minimum signal level is not defined when DUT is connected to an LISN with impedance of 2Ω (PRIME LISN). Anyway we defined a TX power > 120 dBμV over PRIME LISN (impedance of 2Ω).

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Due to that mismatch between transmission power requirements of section 6.3.1.2 of EN50065 standard and section 2.1 of G3-PLC device certification, our devices have to transmit in two different ways:

1. Certification Mode (AKA "High Z" mode or "High Impedance" mode).
2. Field Mode (AKA "Very Low Z" mode, "Very Low Impedance" mode).

Important:

1. Normal operation is "Field mode" and every device in the field must transmit in this way. This mode is fully compliant with G3-PLC and PRIME Spec.
2. The Microchip PLC device is able to select the transmission mode automatically depending on the observed amplitude of the transmitted signal (directly related with impedance). This feature lets the same FW to be compliant with both EN50065 and G3-PLC or PRIME device certification.

The process to calibrate the PHY parameters to be used by the automatic transmission mode are detailed in 3. Physical TX Calibration. This is a process necessary depending on the results obtained when evaluating the communication performance detailed in 4. SNR and EVM Tests. Additionally some design problems like noise on the PLC communications band and XTAL configuration can be analyzed using 5. Noise Test and 6. Frequency Deviation sections.

Microchip provides open source software tools to allow the automation of any process that involves serial communication with Microchip PLC devices.

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2. Setup

To implement the PHY performance validation tests, it is important to have the most noise-free environment possible, without external electrical noise sources or interferences that could affect the final results.

Important: Power supplies of computers, battery chargers, light dimmers, low-consumption lights, or USB isolators produce noise in the mains that can affect the final results of the PHY performance validation test. Make sure that the setup is noise free to get the most reliable results.

2.1 Hardware Requirements

For the implementation of the PHY performance validation test measurements, the following devices are necessary:

- AC mains (230 V_{AC} / 50 Hz or 100 V_{AC} / 60 Hz). For steady, error-free operation of the setup, the voltage level must be as stable as possible. Therefore, the voltage variation range must be no more than 2%. Therefore, an AC automatic voltage regulator is required.
- Two electrical transformers 1:1 (minimum 1 KVA).
- One Device Under Test (DUT). This is the device users want to test.
- One reference device when using PL360. Microchip PLC evaluation board like PL360MB with the same coupling board, ATPLCOUP*xxx*, PL360G55-CF, or PL360G55-CB.
- One reference platform when using PL460. PL460-EK requires an additional EK with XPLAINED PRO connector acting like Host Controller. Some of the tested Host controllers are SAMG55-EK, SAME70-EK, PIC32CXMTG-EK or PIC32CXMTx-DB.
- For PLC hybrid profiles, an ATREB215-EK that requires and additional EK acting like Host Controller. Some of the tested Host controllers are SAMG55-EK, SAME70-EK, or PIC32CXMTx-DB (require an additional board to adapt microBUS to Xplained Pro connector).
- Two LISN CISPR 16-1 (see Figure 2-1). For example, use the PMM single phase LISN, model L2-16B.
- One 50Ω (1%, 1W) BNC terminator to fix the impedance load.
- Two LISN PRIME (see Figure 2-2). LISN PRIME is defined in PRIME Specification (refer to the Section 3.9 *Electrical specification of the transmitter*). Microchip developed its own internal adapter to convert a CENELEC LISN into PRIME LISN.
- One BNC Attenuator from 0 to 100 dB. Use a single rotary attenuator, such as model 50R-043 of JFW Industrie, or an automatic attenuation control unit, such as model J7211A of Agilent.

Attention: If using an automatic attenuation control unit as described above, it is recommended to set a fixed BNC attenuator of 3 dB at every input port of the device to protect the unit against dangerous level signals.

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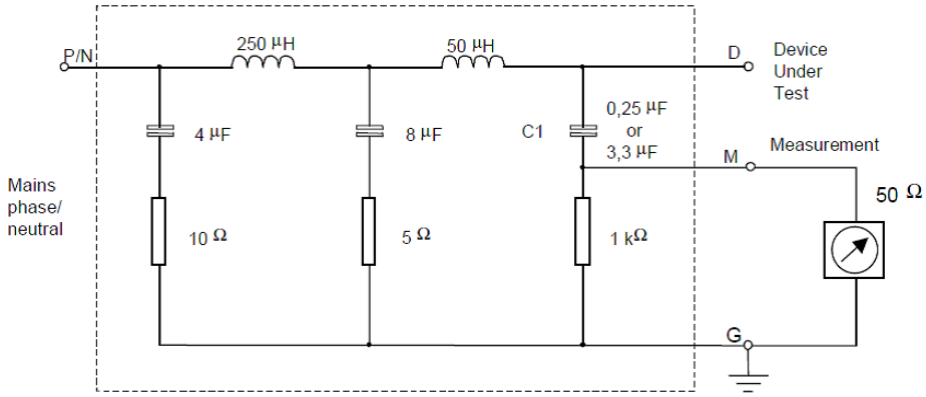
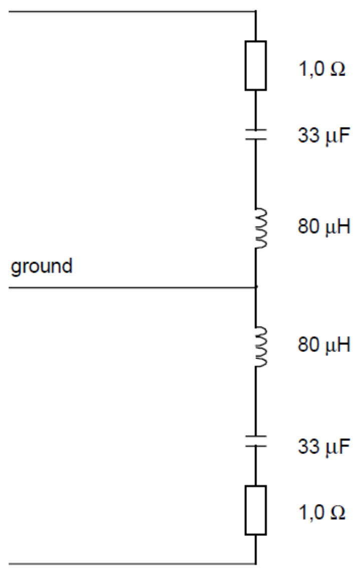
Figure 2-1. Artificial Networks Conforming to CISPR 16-1



C1 = 3.3 µF for 9 to 95 kHz

Figure 2-2. PRIME Artificial Networks (To Use in Conjunction with Artificial Networks Conforming to CISPR 16-1)



2.2 Software and Tools Requirements

Microchip provides the necessary firmware or software and tools to perform different measurements:

- Microchip PLC PHY Tester Firmware – The *Apps_Phy_Tester_Tool* application configures PLC PHY layer and its serial interface to communicate with any application that implements the corresponding Universal Serial Interface (USI) protocol, PROTOCOL_PHY, like the Microchip PLC PHY Tester Tool, to send and receive PLC messages from/to the PLC line and check the PLC transmission or reception processes between boards. This firmware will be loaded into the DUT and the Reference Device. For the DUT, the user must adapt the original PHY Tester Tool project to the hardware specifications of the design. The *Apps_Phy_Tester_Tool* project is part of the Microchip Smart Energy G3-PLC and PRIME suites.
- Microchip PLC PHY Tester Tool – A PC tool developed to enable users to check basic characteristics of the physical layer with Microchip PLC products.
- A Python® Library Package, `mchp_plc_tools` – A collection of Python code to help users create their own Python scripts able to communicate with Microchip PLC boards and check the features

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of the physical layer. To install the different Python packages, a self-installable executable is included for 32-bit and 64-bit Windows or Python installation. Refer to the following packages:
  - *mchp_plc_tools_utils*
  - *mchp_plc_tools_common*
  - *mchp_[plc|rf]_tools_phy_tester_public*
- Python PLC PHY Performance Validation Package – Includes the application for hardware validation analyzing the main parameters considered at communication level:
  - *PHY Calibration Tool*: Mainly helps to calibrate the transmission parameters according with the coupling design in terms of power transmission.
  - *SNR and EVM Analysis*: Mainly validates the TX in terms of linearity and TX power and the RX path in terms of sensitivity, EVM, and SNR.
  - *Noise Analysis*: Mainly validates the background and spurious noise floor present on the design.
  - *Frequency Deviation Analysis*: Mainly validates the main clock oscillator configuration for the PLC communications.

2.3 Setup Configurations

The setup configuration depends on if the measurement requires a reference device (tester) transmitting/receiving information to evaluate it, defining these scenarios:

- Single-Side: The measurement requires a DUT in a solo configuration. The setup is ready to connect a Spectrum Signal Analyzer or Oscilloscope to measure a parameter like the TX power or the background noise.
- Side-by-Side: The measurement requires a configuration point-to-point that simulates a transmission path between a tester and the DUT.

In both cases, depending on the impedance network connected to the DUT, the measurements will be different. So, the user will need to analyze the DUT by means of two different configurations of the setups:

- **Configuration A.** DUT (and reference device when needed) connected to CENELEC CISPR16-1 LISN (High Impedance Mode). Mostly used on laboratory and certification processes.
- **Configuration B.** DUT (and reference device when needed) connected to PRIME Adaptation LISN (Low Impedance Mode). Mostly similar to a real network scenario in the field.

To implement any tests, it is important to have the cleanest environment possible, without external noise sources or interferences that could affect to the final results.

If using an unique host PC to control the setup, USB isolators must be used to avoid coupling in the PLC signal with the common reference signal of USB cables and the boards.

In the case of FCC band, the environment has to be double controlled due to:

- High PLC coupling due to using high frequency channels. It is important to keep all the cables as separated as possible due to magnetic coupling being higher in the FCC frequencies, and this could cause incorrect measurements.
- If using USB isolators to connect the devices to the computer, take into account the possible noise that these isolators could be adding to the network. Some of these USB isolators use frequencies of the FCC band that could affect the communications.

2.3.1 Setup Configurations – Single-Side

The measurement requires a DUT in a solo configuration. The setup is ready to connect a Spectrum Signal Analyzer or Oscilloscope to measure parameters like the TX power (on Physical TX calibrations) or the background noise (on a Noise Test).

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There are two different configurations of the setups:

- **Configuration A.** DUT connected to CENELEC CISPR16-1 LISN. See Figure 2-3.
- **Configuration B.** DUT connected to PRIME Adaptation LISN. See Figure 2-4.

Both of these setup configurations are described in the next figures.

Figure 2-3. Configuration A: Single Side Setup with DUT in High Impedance Mode

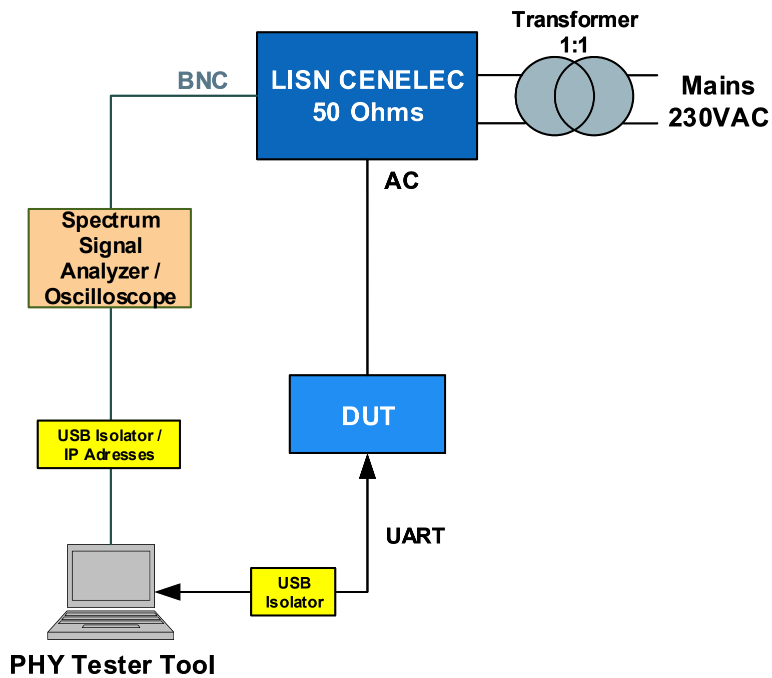
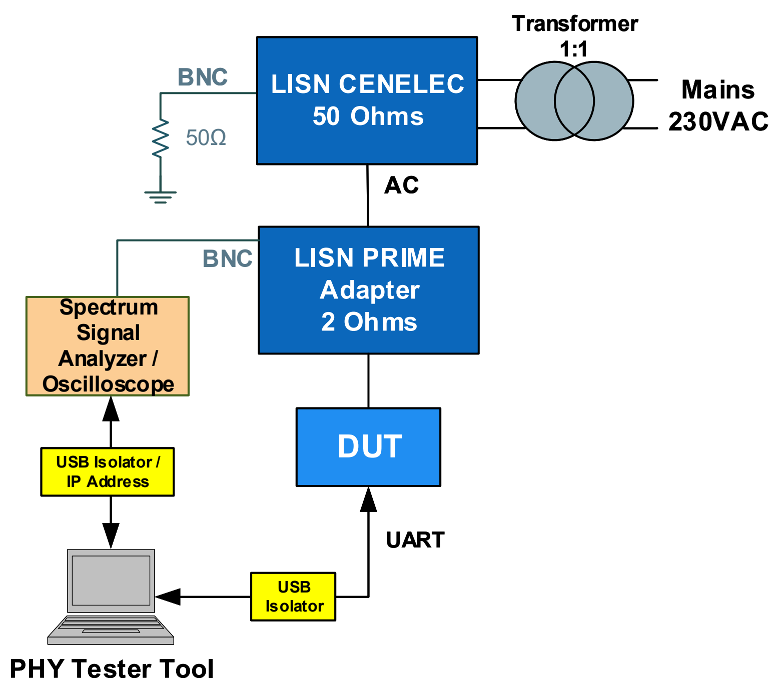


Figure 2-4. Configuration B: Single Side Setup with DUT in Low Impedance Mode



It is advisable at the input of the Spectrum Signal Analyzer, to include a pulse limiter that protects the measuring receiver's input against high RF input levels and high-energy interfering pulses, for

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example, when the DUT is switched on and off. Additionally, a characterized 20 dB attenuator must be included to reduce the signal level that reaches the pulse limiter.

2.3.2 Setup Configurations – Side-by-Side

The measurement requires a configuration point-to-point that simulates a transmission path between a tester and the DUT. The setup is ready to connect a digital attenuator (controlled through Virtual Instrument Software Architecture VISA) in the middle to simulate a transmission path with different attenuations to measure transmission power or sensibility. There are two different configurations of the setups:

- **Configuration A.** DUT and reference device connected to CENELEC CISPR16-1 LISN (High Impedance Mode). Mostly used on laboratory and certification processes. See Figure 2-5.
- **Configuration B.** DUT and reference device connected to PRIME Adaptation LISN (Low Impedance Mode). Mostly similar to real network scenario in the field. See Figure 2-6.

Both of these setup configurations are described in the next figures.

Figure 2-5. Configuration A: Side by Side Setup with DUT in High Impedance Mode

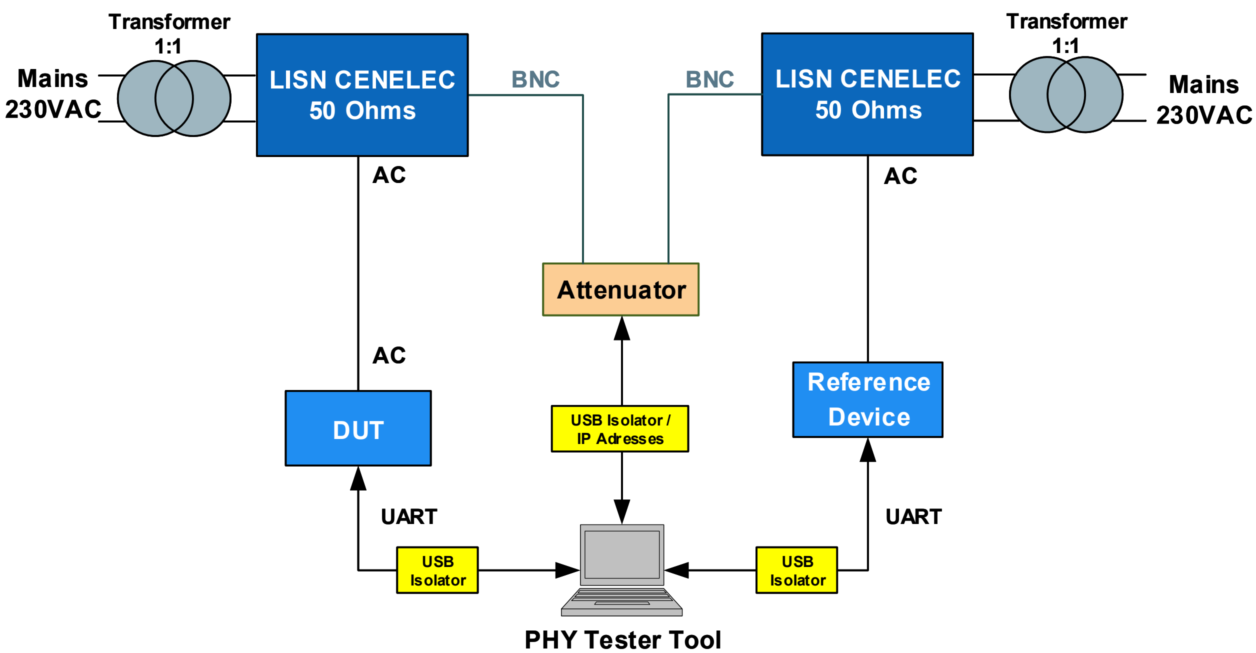

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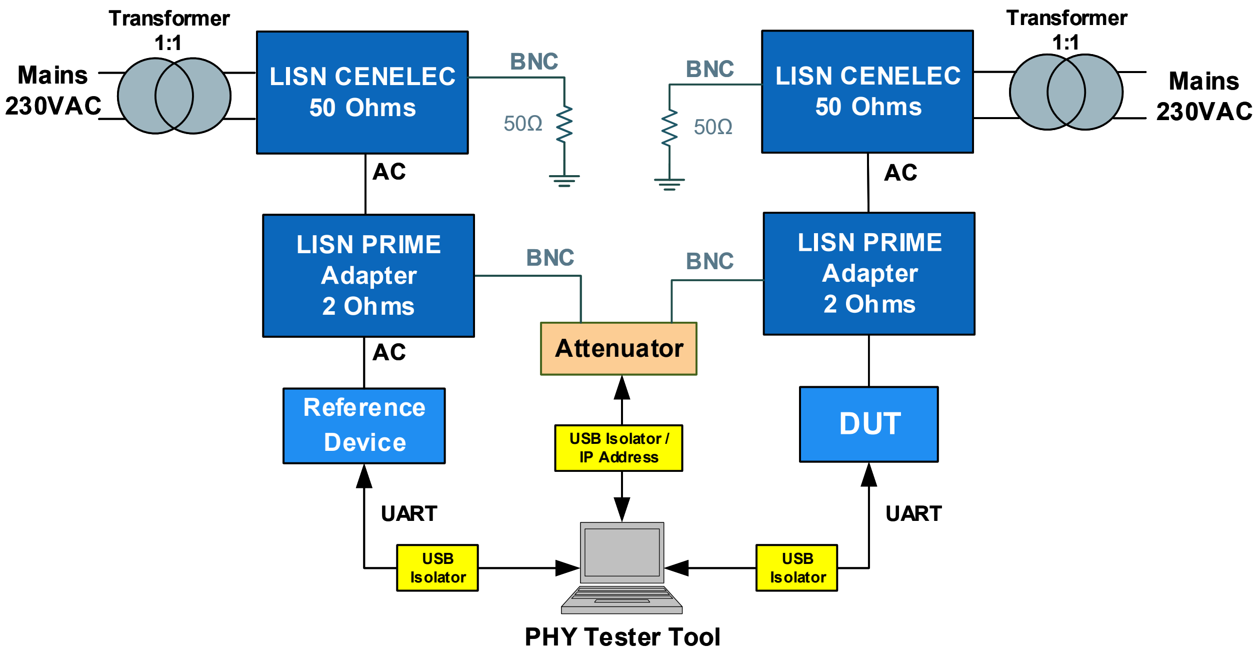
Figure 2-6. Configuration B: Side by Side Setup with DUT in Low Impedance Mode



Additional fixed attenuators are recommended at the output of LISNs (3 dB in each device) and at the ports of the Digital Attenuator (6 dB in each port) to reduce the possibility of breaking them when the value of the attenuator is changed during the tests. In addition, a guard time in any transmission must be included before and after reprogramming the digital attenuator.

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3. Physical TX Calibration

Microchip provides a set of PLC reference designs that passed all required certifications and performance tests to ensure a successful field deployment.

Implementation of firmware protocols over PLC_PHY requires some values to be calculated by calibration; therefore, the calibration process is essential to get the optimal PLC signal transmission behavior in accordance with customer specifications.

The objective is to explain the transmission stage of the Physical layer (PHY) in the PLC protocols, then show how to obtain more accurate calibration values to:

- Meet power injection requirements.
- Meet signal quality requirements.
- Compensate non-linearities of the power supply related to components' tolerances and PCB layout.
- Compensate non-linearities of the coupling design related to components' tolerances and PCB layout.

The Microchip PLC implementations include default PHY layer configuration values optimized for the Evaluation Kits. With the help of the PHY Calibration Tool, it is possible to obtain the optimal configuration values for the customer´s hardware implementation.

Refer to the PLC Host Controller document for more details about the available configuration values and their purpose.

3.1 Physical Layer Capabilities

The firmware implementation for PLC protocols makes use of the following concepts related to the transmission and reception stages:

- Transmission modes
- Impedance detection
- Equalization

3.2 Transmission Modes

The transmission modes are configurations applied to the PHY layer to improve the performance, efficiency and spectrum ripple of the output driver according to the impedance detected in the line.

Depending on the detected impedance, two transmission modes are defined in register REG_CFG_IMPEDANCE:

- HIGH. Mode optimized for high impedance (Z > 20Ω)
- VERY_LOW. Mode optimized for very low impedance (Z < 10Ω)

Additionally, the PHY layer can modify the signal gain in a way that offers optimum results when combined with the Transmission mode. This behavior is controlled by the REG_CFG_AUTODETECT_IMPEDANCE. There are three operation modes:

- OFF: Transmission mode and gain are fixed
- AGC: Transmission mode is fixed but the gain is managed by the Automatic Gain Control (AGC) block to achieve the signal level injection target
- ON: Transmission mode and gain are managed dynamically to optimize the output according to the line impedance and signal level injection target

Each Transmission mode is optimized within an impedance range; therefore, the PHY layer does not work properly in terms of performance/efficiency when operating outside of such range. Suppose there is a set signal injection objective of 110 dBuV for both HI and VLO modes. The following figures show the response of forced modes in an impedance range from 0 to 50Ω.

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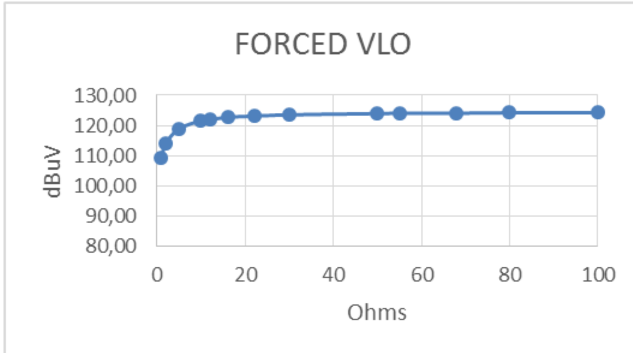
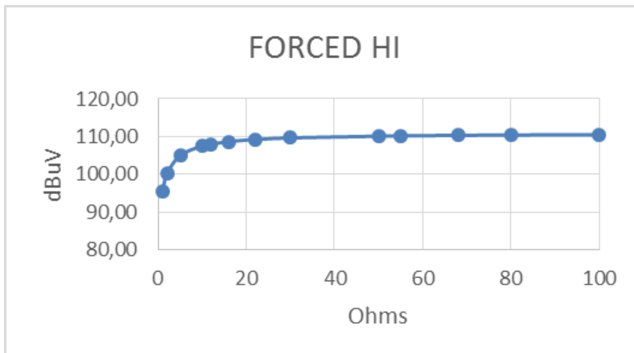
Figure 3-1. Transmission Power on HI and VLO Modes Depending on the Line Impedance





The figures above show the signal level when both Transmission mode and gain are fixed (OFF mode). In each mode, the injected transmission signal is reaching the objective in its intended range, but out of such range, each mode is not achieving the injection objectives. Also, the response has a much more stable trend for impedance above 20Ω, but for lower values, the transmission driver is more dependent on the detected impedance.

It is also possible to enable a configuration feature where the Transmission mode is fixed but slight changes in gain are allowed (AGC mode). This allowed variation in gain is probably not enough to meet the injection objective.

To meet the objective in the entire impedance range (with some limitations in low impedance as explained above), rely on the operation mode recommended where an Impedance Detection and Adaptation algorithm is implemented in the Physical layer (ON mode).

3.3 Impedance Detection

The following figure shows the response in ON operation mode, where the system updates its response depending on the impedance detected in reception and following the objective of transmitted signal level, compared to the fixed modes:

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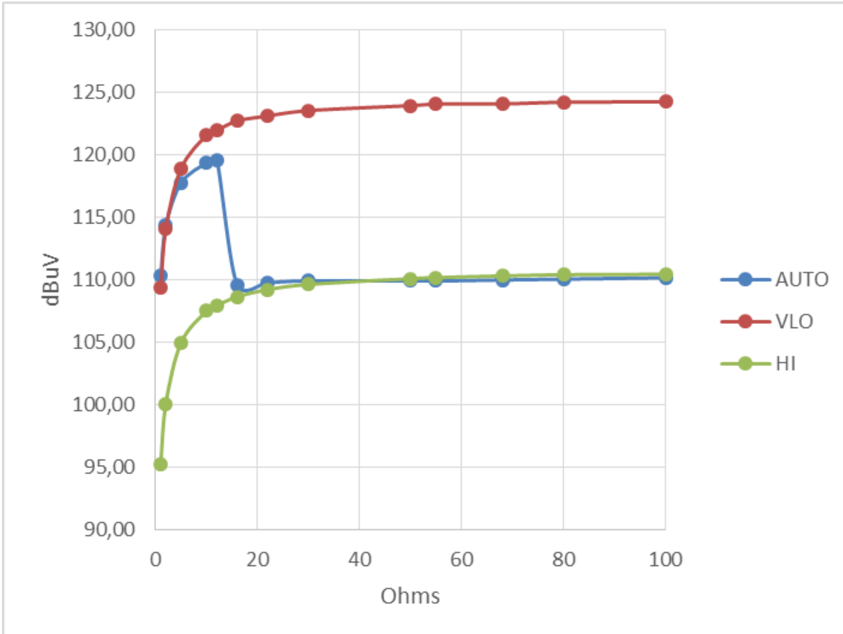
Figure 3-2. Transmission Power Response When Auto Impedance Detection is Configured

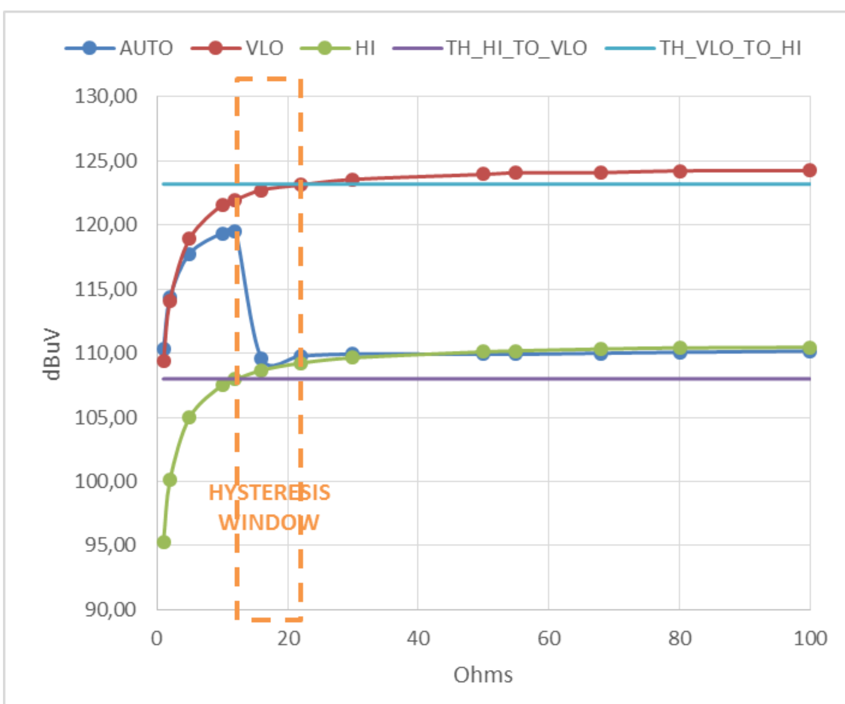


This adaptation is achieved by defining thresholds to switch from HI to VLO mode, and vice versa, which determine the points where Transmission mode is changed.

These thresholds are defined such that the switch from HI to VLO is done in a lower impedance than the switch from VLO to HI, obtaining a hysteresis window to avoid continuous switching between states which will lead to a continuous change in signal injection, which is an undesirable scenario.

The following figure illustrates such thresholds and the hysteresis window they achieve:

Figure 3-3. Thresholds and Hysteresis Window on the Auto Impedance Detection Configuration



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As shown in the figure, the Auto response has been obtained sweeping from high to low impedance; this is why the switch is done near the lower value of the hysteresis window (some point between 10 and 15Ω). If the sweep is done in the opposite way, from low to high impedance, the transition will be done near the higher value of the hysteresis window, so the curve will follow the VLO curve inside the window and then switch to HI curve just above 20Ω.

It is also seen that the Auto curve does not follow the trend of the forced ones exactly. This is because the algorithm performs a fine tuning in each transmission according to the detected signal value, trying to adjust more closely to the signal injection objectives.

3.4 Equalization

Usually the output transmission driver has a non-flat spectrum response inside the working band (ripple).

Depending on the transmitted power difference between carriers, it is possible that the response is not as flat as desired.

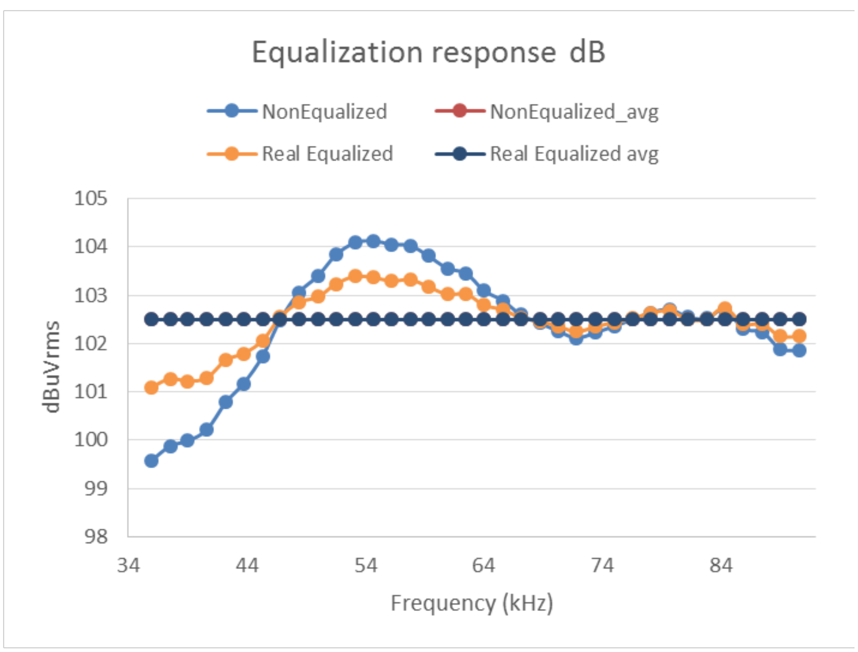
The physical layer is able to perform this equalization by means of signal pre-distortion, which compensates the effect of the external driver, effectively reducing the ripple and obtaining a final response closer to a flat one.

Equalization has a tight relationship with the transmission modes covered in previous sections; in fact, each transmission mode defines a particular equalization. As configurations are different for each mode, the response is also different, which requires different equalization.

An important aspect to take into account is that the objective of the equalization is to reduce ripple, giving a flatter response but keeping the average signal injection. Therefore, care must be taken to reduce the signal in some carriers and increase it in others, resulting in the same response after integrating the signal level inside the operation band.

The following figure shows an example of equalization in the PLC Cenelec-A band:

Figure 3-4. Equalization Response Depending on the Frequency on Cenelec-A Band



The figure shows how the ripple is reduced after equalization, keeping the same signal average in band (overlapped curves).

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3.5 How to Get Calibration Values

Microchip provides a Python script named "phycalibrationtool.py" to get optimal calibration values implied in the signal emission characterization, which could affect the ripple, amplitude and impedance algorithm detection used by PLC protocol implementations (Figure 3-7).

The script is intended to communicate with a physical PLC-based board running phy_tester_tool firmware.

Along the test process, the PLC signal may be connected to different impedance loads; therefore, it is strongly recommended to uncouple the PLC signal from the mains power supply of the device under test (see the figure below).

Figure 3-5. Calibration Setup

The physical calibration process implies the following steps:

- Initialization: Set the default equalization and gain calibration values used by the PLC PHY Calibration Tool.
- Equalization: The objective is to get a flatter frequency response of the signal on the band in use; for that, a maximum ripple must be defined below the customer limits. As a general rule, Microchip recommends a margin of 0.5-1 dB to handle the different impedance load of the equalization performed.
- Gain Calibration: The objective of gain calibration is to get the desired signal power in a range of variable gain for AUTO GAIN mode. An initial gain must be defined and the customer must decide minimum and maximum values for AUTO GAIN mode. The minimum value could have an impact on the performance of VLOW mode when emitting against high impedance if the system cannot emit low enough to maintain the signal on the PLC line. After modifying the gain values, it is strongly recommended to measure the ripple again to check if it was affected due to non-linearity when using a high level of power.
- Max RMS Level Process: It obtains the target RMS values for each transmission mode.
- Thresholds Process: The process calculates the threshold values to switch between transmission modes (HIGH to VLOW and opposite).

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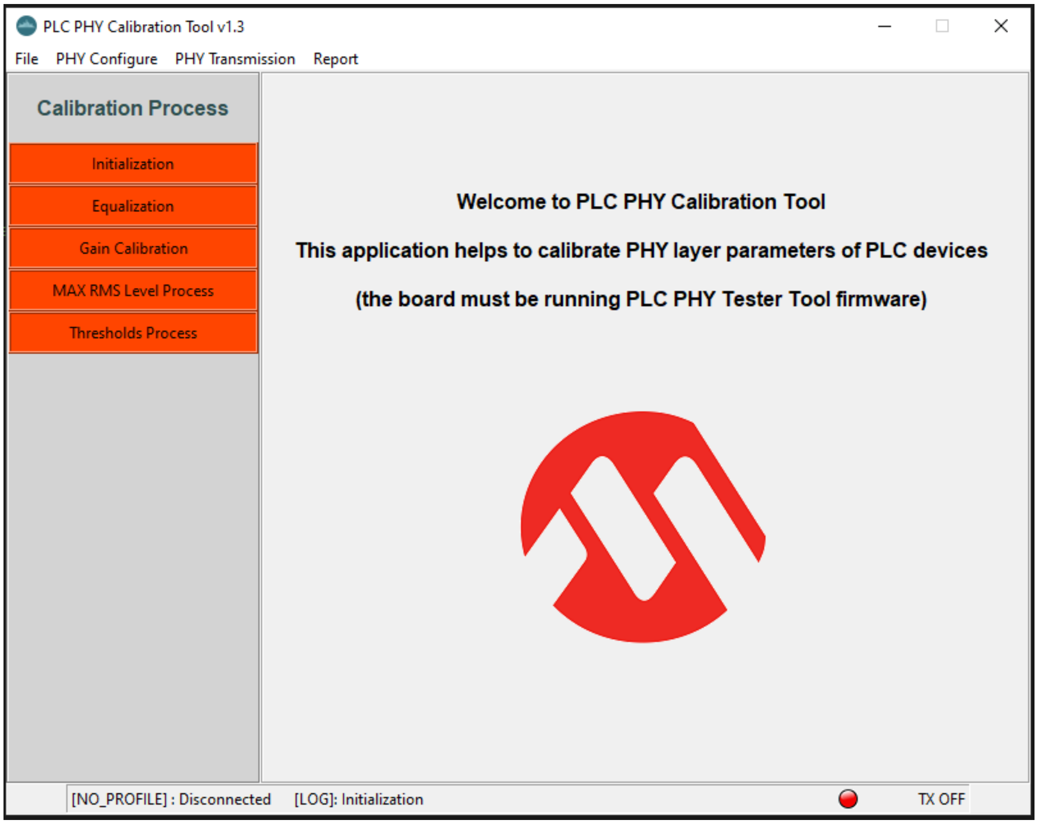
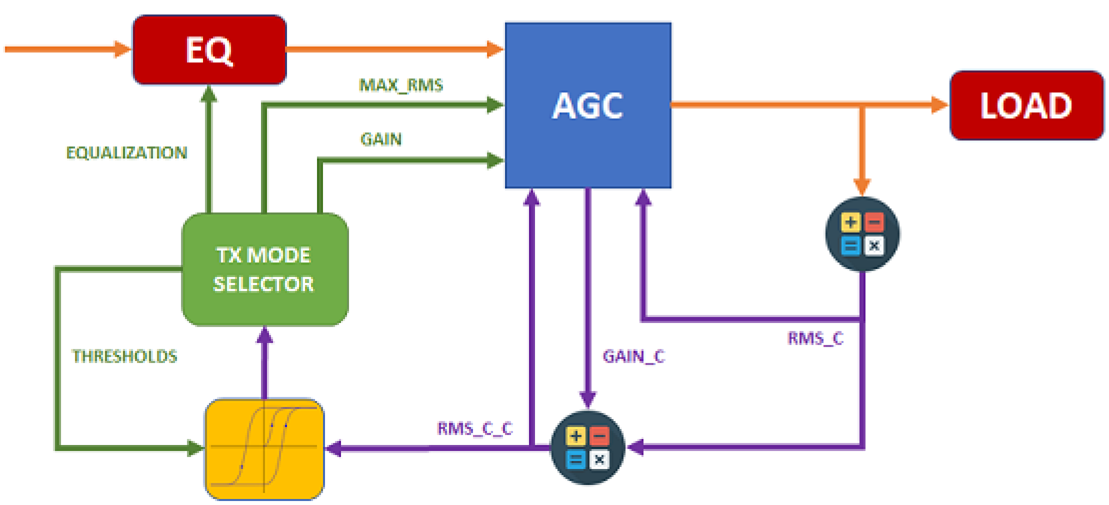
Figure 3-6. PHY Calibration Tool Main Window



The figure below shows the relationship between the steps and the firmware implementation, where:

- GAIN_C: Present Gain Value: a valid value between the maximum and minimum set on calibration
- RMS_C: RMS Power Calculated
- RMS_C_C: RMS Power Calculated Corrected used for threshold comparing to change the TX mode

Figure 3-7. Firmware Transmission Path Implementation



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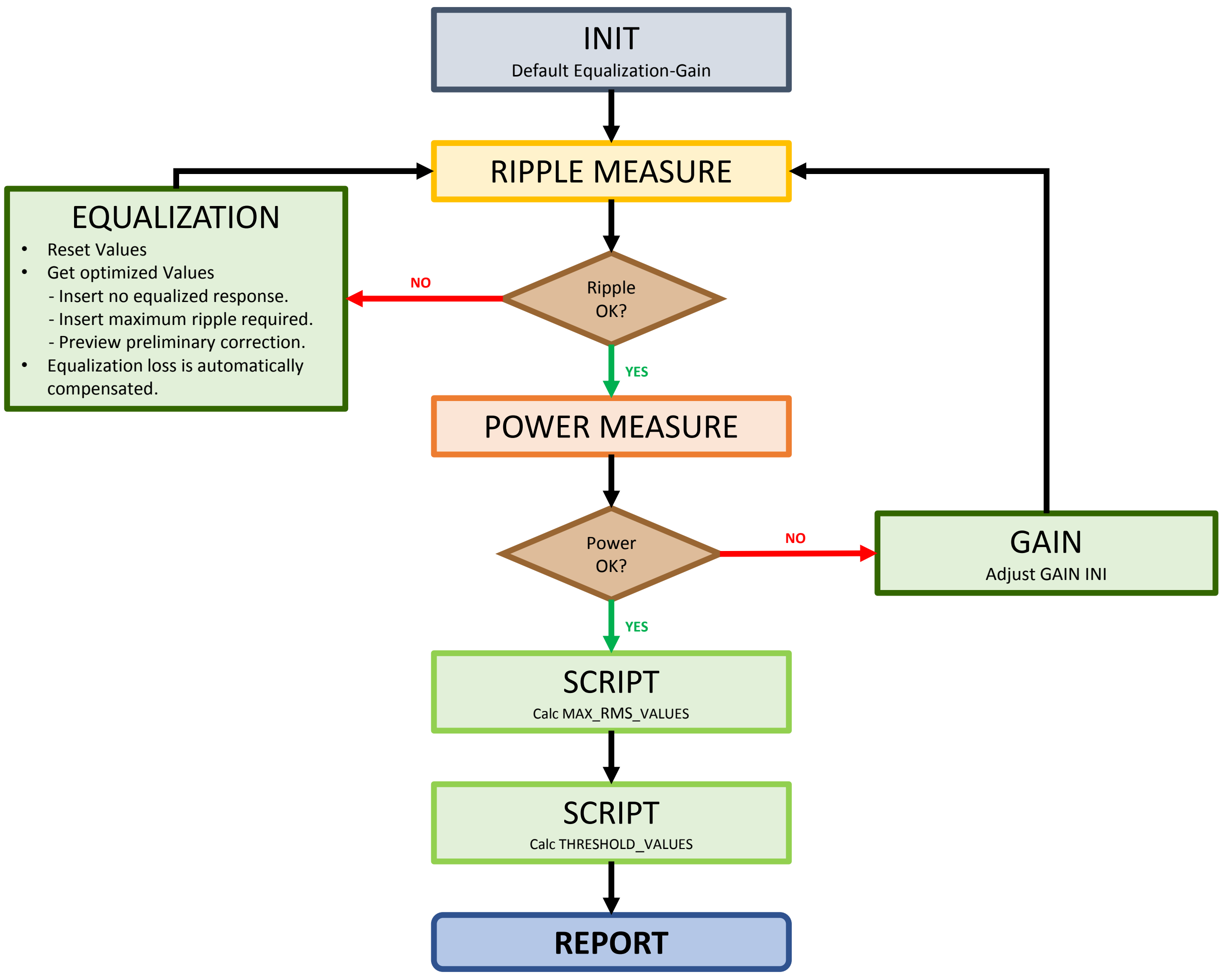
All the calibration steps require a similar setup to Figure 3-5 (more information about setup in the Setup section).

"Equalization" and "Gain Calibration" steps must be run iteratively and require the user to perform ripple and power measurements. On the other hand, the PHY Calibration Tool will automatically look for the best values on the "Max RMS Process" and "Thresholds Process" steps.

Important: In each iteration, equalization must be reset to restore default values.

Figure 3-8. PHY Calibration Tool Workflow



3.6 How to Use Calibration Values

The PHY Calibration Tool generates the report file named "*conf_app_example.h*", which provides the required information to include on PLC projects to apply the custom calibration.

Depending on the PLC protocol stack version and platform, the process to include the calibration information into the PLC projects is different. By default, the contents are simplified to be included in MPLAB® projects.

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3.6.1 MPLAB Projects

The PHY Calibration Tool generates an output configuration file (Figure 3-9) that provides the required information to include in PLC projects to apply the custom calibration on MPLAB projects.

Figure 3-9. Configuration File Report

conf_app_example.h

```
/* PLC PHY Coupling parameters for XXX branch */
/* Coupling Values to define RMS values in Hi/Vlow impedance */
#define SRV_PCOUP_RMS_HIGH_TBL                    {1313, 937, 667, 477, 342, 247, 180, 131}
#define SRV_PCOUP_RMS_VLOW_TBL                    {4329, 3314, 2387, 1692, 1201, 853, 608, 432}

/* Coupling Values to define Threshold values to check in Hi/Vlow impedance */
#define SRV_PCOUP_THRS_HIGH_TBL                   {0, 0, 0, 0, 0, 0, 0, 0, 1025, 729, 519, 372, 265,
#define SRV_PCOUP_THRS_VLOW_TBL                   {0, 0, 0, 0, 0, 0, 0, 0, 10242, 7302, 5197, 3708,

#define SRV_PCOUP_DACC_TBL                        {0x0, 0x0, 0x100, 0x100, 0x0, 0x0, \
                                                  0x4f5000ff, 0x1b1b1b1b, 0x0, 0x0, 0x6, 0x355, \
                                                  0x0, 0x1020f0, 0x355, 0x0, 0x1020ff}

/* Coupling Values to define IFFT Gain in Hi/Vlow impedance */
#define SRV_PCOUP_GAIN_HIGH_TBL                   {49, 20, 256}
#define SRV_PCOUP_GAIN_VLOW_TBL                   {364, 180, 408}
/* Number of TX levels */
#define SRV_PCOUP_NUM_TX_LEVELS                   8
#define SRV_PCOUP_LINE_DRV_CONF                   5
/* Coupling Values to define Predistorsion Coefficients in Hi/Vlo impedance */
#define SRV_PCOUP_PRED_HIGH_TBL                   {0x7399, 0x6D5B, 0x6982, 0x671E, 0x6699, 0x6730,
                                                  0x76BF, 0x77FE, 0x7905, 0x7A70, 0x7BC9, 0x7C88,
                                                  0x7F96, 0x7F76, 0x7F9D, 0x7EF8, 0x7E1B, 0x7D55,
                                                  0x7560, 0x7498, 0x72B8, 0x7185, 0x7049, 0x6F5D,
                                                  0x6676, 0x6567, 0x654C, 0x6546, 0x651F, 0x65CD,
                                                  0x72F9, 0x74E0}
#define SRV_PCOUP_PRED_VLOW_TBL                   {0x7FEC, 0x7D9A, 0x7BBA, 0x7987, 0x7752, 0x75E3,
                                                  0x66CC, 0x655C, 0x63F4, 0x6318, 0x626F, 0x6186,
                                                  0x6024, 0x608F, 0x615F, 0x61D9, 0x61E3, 0x6265,
                                                  0x6959, 0x6A44, 0x6A93, 0x6B1F, 0x6C52, 0x6D4F,
                                                  0x7348, 0x7371, 0x7453, 0x7566, 0x75C8, 0x764F,
                                                  0x7DE6, 0x7FFF}

/*****************************************************************************************************
```

Most of the changes can be done through MPLAB MCC Configurator for the `PLC PHY Coupling` module.

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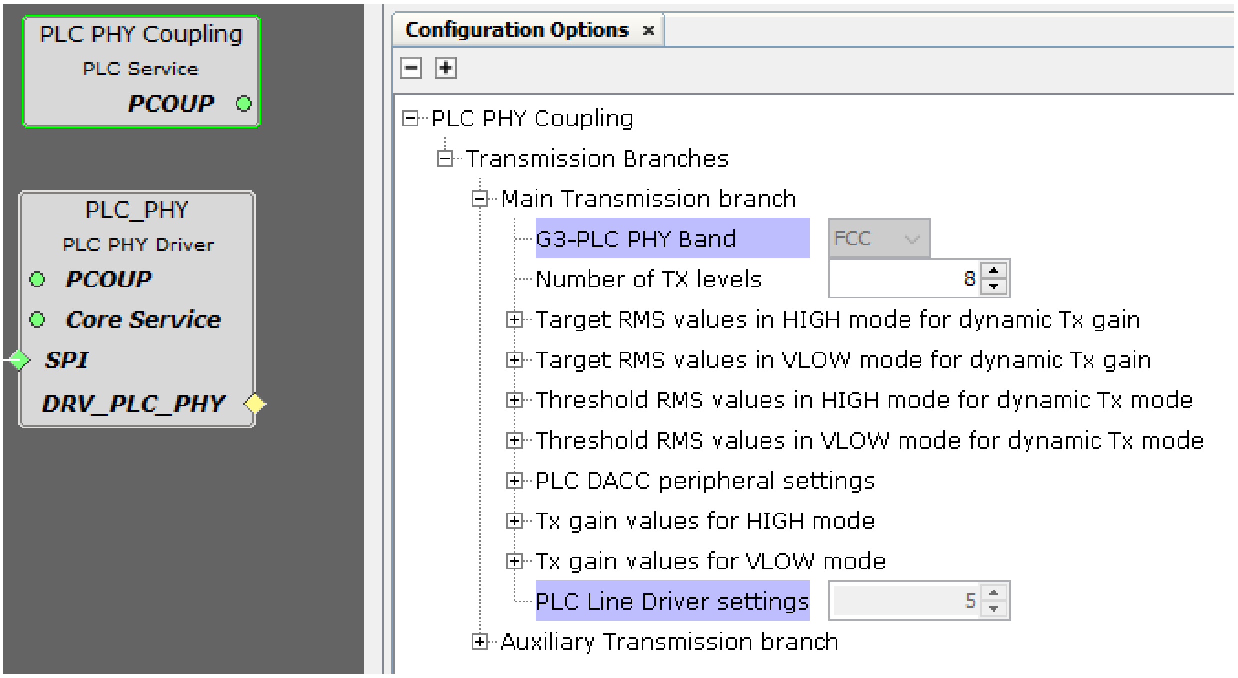
Figure 3-10. MPLAB Code Configurator for PLC PHY Coupling Module



Modifying the configuration of the PLC PHY Coupling in MCC is the recommended method, as it will be reflected in the source code automatically by clicking the Generate button of the tool. The Table 3-1 table shows the correspondence between the report file definitions and the MCC PLC PHY Coupling fields.

Table 3-1. Correspondence on MCC PLC PHY Coupling Fields

SRV_PCOUP_RMS_HIGH_TBL	Target RMS values in HIGH mode for dynamic TX gain
SRV_PCOUP_RMS_VLOW_TBL	Target RMS values in VLOW mode for dynamic TX gain
SRV_PCOUP_THRS_HIGH_TBL	Threshold RMS values in HIGH mode for dynamic TX mode
SRV_PCOUP_THRS_VLOW_TBL	Threshold RMS values in VLOW mode for dynamic TX mode
SRV_PCOUP_DACC_TBL	PLC DACC peripheral settings
SRV_PCOUP_GAIN_HIGH_TBL	TX gain values for HIGH mode
SRV_PCOUP_GAIN_VLOW_TBL	TX gain values for VLOW mode
SRV_PCOUP_NUM_TX_LEVELS	Number of TX levels

When pre-distortion values need to be updated, it is mandatory to modify the source files generated by the MCC directly, specifically the file `config\PLATFORM\service\pcoup\srv_pcoup.h`.

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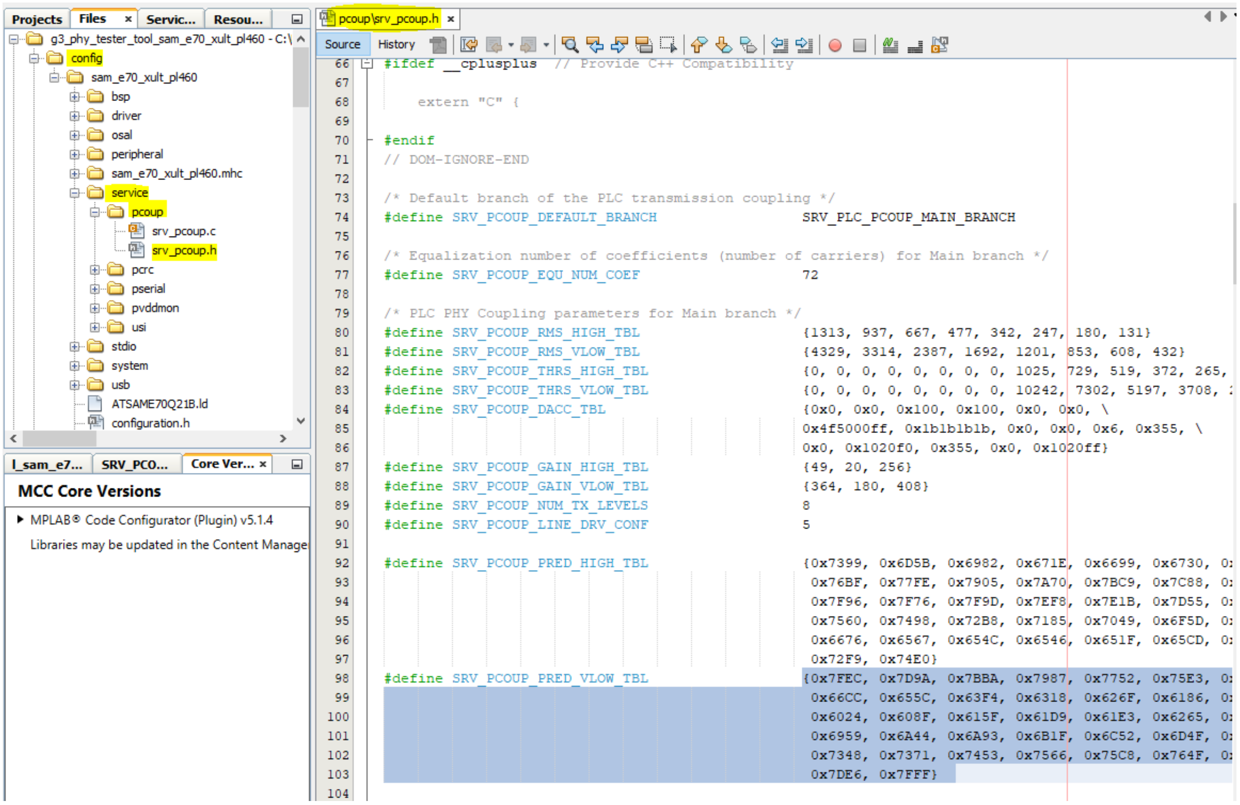
Figure 3-11. PLC PHY Coupling Header File Generated by MCC



Depending on the platform and the protocol, the values from the PHY calibration Tool configuration file must update the associated definitions to that platform and protocol on the source file. For example:

- If the calibration was done for the PL460-EK auxiliary branch, the definitions associated in the source file include an `_AUX_`.

```
#define SRV_PCOUP_AUX_PRED_HIGH_TBL    {0x670A, 0x660F, 0x676A, 0x6A6B, 0x6F3F, 0x7440, 0x74ED, 0x7792, 0x762D, 0x7530, 0x7938, 0x7C0A, 0x7C2A, 0x7B0E, \
                                        0x7AF2, 0x784B, 0x7899, 0x76F9, 0x76D6, 0x769F, 0x775D, 0x70C0, 0x6EB9, 0x6F18, 0x6F1E, 0x6FA2, 0x6862, 0x67C9, \
                                        0x68F9, 0x68A5, 0x6CA3, 0x7153, 0x7533, 0x750B, 0x7B59, 0x7FFF}
#define SRV_PCOUP_AUX_PRED_VLOW_TBL    {0x7FFF, 0x7DB1, 0x7CE6, 0x7B36, 0x772F, 0x7472, 0x70AA, 0x6BC2, 0x682D, 0x6618, 0x6384, 0x6210, 0x61D7, 0x6244, \
                                        0x6269, 0x63A8, 0x6528, 0x65CC, 0x67F6, 0x693B, 0x6B13, 0x6C29, 0x6D43, 0x6E26, 0x6D70, 0x6C94, 0x6BB5, 0x6AC9, \
                                        0x6A5F, 0x6B65, 0x6B8C, 0x6A62, 0x6CEC, 0x6D5A, 0x6F9D, 0x6FD3}
```

- If the calibration was done for a PRIME channel, the definitions associated in the source file include a `_CHNx_`.

```
#define SRV_PCOUP_CHN6_RMS_HIGH_TBL        {1243, 1108, 987, 880, 784, 699, 623, 556}
#define SRV_PCOUP_CHN6_RMS_VLOW_TBL        {3694, 3368, 3037, 2713, 2416, 2149, 1911, 1698}
#define SRV_PCOUP_CHN6_THRS_HIGH_TBL       {0, 0, 0, 0, 0, 0, 0, 0, 1081, 963, 858, 765, 682, 607, 541, 483}
#define SRV_PCOUP_CHN6_THRS_VLOW_TBL       {0, 0, 0, 0, 0, 0, 0, 0, 100000, 100000, 100000, 100000, 100000, 100000, 100000, 100000}
#define SRV_PCOUP_CHN6_GAIN_HIGH_TBL       {60, 30, 256}
#define SRV_PCOUP_CHN6_GAIN_VLOW_TBL       {256, 128, 287}
#define SRV_PCOUP_CHN6_LINE_DRV_CONF       5
#define SRV_PCOUP_CHN6_MAX_NUM_TX_LEVELS   8
```

- If the calibration was done for a PRIME dual channel configuration, the definitions associated in the source file include a `_2CHN_`.

```
#define SRV_PCOUP_CHN45_RMS_HIGH_TBL        {1206, 1074, 957, 853, 760, 678, 604, 539}
#define SRV_PCOUP_CHN45_RMS_VLOW_TBL        {3138, 2804, 2480, 2186, 1928, 1701, 1506, 1338}
#define SRV_PCOUP_CHN45_THRS_HIGH_TBL       {0, 0, 0, 0, 0, 0, 0, 0, 1024, 912, 814, 725, 647, 577, 515, 459}
#define SRV_PCOUP_CHN45_THRS_VLOW_TBL       {0, 0, 0, 0, 0, 0, 0, 0, 100000, 100000, 100000, 100000, 100000, 100000, 100000, 100000}
#define SRV_PCOUP_CHN45_GAIN_HIGH_TBL       {120, 60, 256}
#define SRV_PCOUP_CHN45_GAIN_VLOW_TBL       {256, 128, 256}
#define SRV_PCOUP_CHN45_LINE_DRV_CONF       5
#define SRV_PCOUP_CHN45_MAX_NUM_TX_LEVELS   8
```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4. SNR and EVM Tests

The SNR parameter refers to the Signal-to-Noise Ratio, defined as the ratio of measured received signal level to noise level of the last received PPDU.

The EVM parameter refers to the Error Vector Magnitude, defined as the quality of the measured received signal of the last received PPDU.

NOTICE The SNR and EVM tests provides an idea of the design performance compared to Microchip reference designs.

This test enables the user to verify the reception and transmission levels of any PLC prototype. This prototype is also named as Device Under Test (DUT).

The SNR and EVM tests consist of transmitting and receiving predefined PLC messages between the DUT and reference device. Both devices are connected to the side-by-side setup as described before. The shipping message process between the devices is repeated in both ways, increasing the attenuation level step-by-step. At the end of the test, measurement results for the DUT can be compared with the performance of the reference design provided by Microchip.

In the following sections, procedure and measurement analysis are commented.

4.1 SNR and EVM Measurement Process With Python

The SNR and EVM test procedure is the same for both setups, but there are some firmware configurations that the user must consider depending on which TX and RX impedance mode is evaluated (High or Low-Impedance mode).

Steps to implement in the SNR and EVM measurement process are as follows:

1. Setup initialization
2. DUT Transmission and Reception in the High-Impedance mode
3. DUT Transmission and Reception in the Low -mpedance mode

These three steps can be done for any modulation scheme and type.

To facilitate the SNR and EVM measurements, Microchip developed a Python Package, *microchip_plc_tools.* This package is a collection of Python code to help users to create their own Python scripts which can communicate with Microchip PLC boards. This Microchip Python Package enables the user to develop their own application to automate the test process.

NOTICE Python is a widely used high-level programming language, and its design philosophy emphasizes code readability and simplicity. For this reason Python is suitable to create scripts to automate tasks or tests that improve development times.

For additional information about the Microchip package installation, structure, and practical examples of use, refer to the "PLC Tools Python Package User Guide".

Attention: To implement this test using the Microchip Python Package, users must install Python 3.X. Refer to the https://www.python.org/downloads/ for additional information.

Ensure that these microchip_plc_tools packages are installed:

- microchip_plc_tools_common
- microchip_plc_tools_utils

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- microchip_plc_tools_phy_tester_public

Additionally, verify that the latest version of the required Python packages and dependencies refered in the corresponding readme.txt are installed

4.1.1 Initialization

Important: Install Microchip Python Libraries and dependencies for the corresponding Python version needed by the PHY Performance script TestATT_g3.py for G3-PLC or TestATT_prime.py for PRIME validation

Once boards are supplied and programmed with the PHY Tester tool firmware example, connect both DUT and reference boards to the PC by means of a USB or USB to Serial Port cables.

Important: If DUT is not isolated from mains, the data cable needs to be isolated to establish communication.

Open and edit the **TestATT_g3.config** or **TestATT_prime.config** file.

Configure the property **name** to form the name of the output files, and identify the results.

Configure the **paths** setting:

- **rx**: Data from Reference Tester to DUT. Helps to analyze DUT reception path.
- **tx**: Data from DUT to Reference Tester. Helps to analyze DUT transmission path.
- **tx_rx**: First evaluates TX path, then RX path.
- **rx_tx**: First evaluates RX path, then TX path.

Configure the **port_dut** and **port_reference** that defines the connection to the DUT and the Reference Tester:

- **COMX:SPEED** – Local Serial COM Port connection and baudrate speed.
- **IP:PORT** – TCP/IP connection. Physical connection to DUT and Reference Tester is always a Serial Port connection, but it can be accessed remotely through additional software like socat, COMbyTCP, SerialToIP, and so on.

Configure the **band** or **channels** setting corresponding to testbed frequencies to evaluate.

Configure the **schemes** and **modulations** to test (by default all the combinations must be tested).

Configure the platform **device** under test. By default ATPL360 (valid for PL460 too).

Configure the **tester_autodetect_branch** and **tester_impedance** settings corresponding with the setup being evaluated. By default, the tester_autodetect_branch must be set to 0 to force the transmission mode:

- High-Impendance mode: Configure the tester_impedance to 2.
- Low-Impedance mode: Configure the tester_impedance to 0.

Configure the attenuation plan for the test:

- Configure the Attenuator Instrument **attenuator_device_id** using the **Virtual instrument software architecture** (VISA) address. If the setup does not include a digital attenuator instrument, comment the line and the script will ask for manual attenuation setting during the test.
- Configure the **att_start**, **att_step** and **att_stop** values.
- Configure the **att_fixed** present on the setup. Typically:

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- att_fixed = 30 dB = 6 dB (CISPR 16-1) + 3 dB (Fixed Att on CISPR 16-1 BNC) + 6 dB (Fixed Att on Input BNC Attenuator Instrument) + 6 dB (Fixed Att on Input BNC Attenuator Instrument) + 3 dB (Fixed Att on CISPR 16-1 BNC) + 6 dB (CISPR 16-1).

If needed, configure the message length, **msg_len** between:

- **max**: Configures the maximum physical size for the frame.
- **fixed**: Configures the value defined by **msg_len_value**.
- **random**: Configures a random value between the minimum and maximum allowed.

If needed, configure the message content: **msg_content**:

- **random**.
- **fixed**: Concatenate the pattern "[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY" in loop.

Additionally, there are some configurations for file report sending and storing:

- **email_server**: Email server for SMTP request.
- **email_notification**: Email address for sending the reports (no SQL databases included).
- **repo_server**: Windows shared folder where store reports and databases.

4.1.2 DUT TX and RX on a High-Impedance Network

CAUTION For this part of the test, the user must set up Configuration A, refer to the Figure 2-5.

Important: Modify the TestATT_[g3|prime].conf file, setting the 'path' as 'tx_rx' and 'tester_impedance' as '0' (High-Impedance mode).

Run the **TestATT_[g3|prime].py** script according to customer-specific configuration depending on their possibilities:

```
C:\PHYperformance>python.exe TestATT_g3.py
C:\Python37\lib\site-packages\visa.py
Physical G3 DUT Testing Tool
Physical Attenuator NOT present!!!
Physical DUT Testing Tool
Set Attenuation to  0
Press Enter to continue...
Completed: 0.000000 %
ATTENUATION: 0
BPSK_ROBO , DIFFERENTIAL
FER = 0.000000 %
Completed: 8.333333 %
ATTENUATION: 0
BPSK , DIFFERENTIAL
FER = 0.000000 %
Completed: 16.666667 %
ATTENUATION: 0
BPSK_ROBO , COHERENT
FER = 0.000000 %
Completed: 25.000000 %
ATTENUATION: 0
BPSK , COHERENT
FER = 0.000000 %
Set Attenuation to  5
Press Enter to continue...
Completed: 33.333333 %
ATTENUATION: 5
BPSK_ROBO , DIFFERENTIAL
FER = 0.000000 %
Completed: 41.666667 %
ATTENUATION: 5
BPSK , DIFFERENTIAL
```


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```
FER = 0.000000 %
Completed: 50.000000 %
ATTENUATION: 5
BPSK_ROBO , COHERENT
FER = 0.000000 %
Completed: 58.333333 %
ATTENUATION: 5
BPSK , COHERENT
FER = 0.000000 %
Set Attenuation to  10
Press Enter to continue...
Completed: 66.666667 %
ATTENUATION: 10
BPSK_ROBO , DIFFERENTIAL
FER = 0.000000 %
Completed: 75.000000 %
ATTENUATION: 10
BPSK , DIFFERENTIAL
FER = 0.000000 %
Completed: 83.333333 %
ATTENUATION: 10
BPSK_ROBO , COHERENT
FER = 0.000000 %
Completed: 91.666667 %
ATTENUATION: 10
BPSK , COHERENT
FER = 0.000000 %
FINISHED with completed: 100.000000 %
Test finished, Duration:0:09:33
Sending e-mail report to username@domain.com
E-mail sent.
```

4.1.3 DUT TX and RX on a Low-Impedance Network

CAUTION For this part of the test, the user must set up the Configuration B, refer to the Figure 2-6.

Important: Modify the TestATT_[g3|prime].conf file, setting the ‘path’ as ‘tx_rx’ and ‘tester_impedance’ as ‘2’ (Vlow-Impedance mode).

Run the **TestATT_[g3|prime].py** script according to the customer-specific configuration depending on their possibilities:

```
C:\PHYperformance>python.exe TestATT_g3.py
C:\Python37\lib\site-packages\visa.py
Physical G3 DUT Testing Tool
Physical Attenuator NOT present!!!
Physical DUT Testing Tool
Set Attenuation to  0
Press Enter to continue...
Completed: 0.000000 %
ATTENUATION: 0
BPSK_ROBO , DIFFERENTIAL
FER = 0.000000 %
Completed: 8.333333 %
ATTENUATION: 0
BPSK , DIFFERENTIAL
FER = 0.000000 %
Completed: 16.666667 %
ATTENUATION: 0
BPSK_ROBO , COHERENT
FER = 0.000000 %
Completed: 25.000000 %
ATTENUATION: 0
BPSK , COHERENT
FER = 0.000000 %
Set Attenuation to  5
Press Enter to continue...
Completed: 33.333333 %
ATTENUATION: 5
```


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```
BPSK_ROBO , DIFFERENTIAL
FER = 0.000000 %
Completed: 41.666667 %
ATTENUATION: 5
BPSK , DIFFERENTIAL
FER = 0.000000 %
Completed: 50.000000 %
ATTENUATION: 5
BPSK_ROBO , COHERENT
FER = 0.000000 %
Completed: 58.333333 %
ATTENUATION: 5
BPSK , COHERENT
FER = 0.000000 %
Set Attenuation to  10
Press Enter to continue...
Completed: 66.666667 %
ATTENUATION: 10
BPSK_ROBO , DIFFERENTIAL
FER = 0.000000 %
Completed: 75.000000 %
ATTENUATION: 10
BPSK , DIFFERENTIAL
FER = 0.000000 %
Completed: 83.333333 %
ATTENUATION: 10
BPSK_ROBO , COHERENT
FER = 0.000000 %
Completed: 91.666667 %
ATTENUATION: 10
BPSK , COHERENT
FER = 0.000000 %
FINISHED with completed: 100.000000 %
Test finished, Duration:0:09:33
Sending e-mail report to username@domain.com
E-mail sent.
```

4.2 SNR and EVM Measurement Process With PLC PHY Tester Tool

The SNR and EVM test procedure is the same for both setups, but there are some firmware configurations that the user will have to take into account depending on the Network Impedance mode (High or Low Impedance).

There are five steps to implement in the SNR and EVM measurement process:

1. Setup initialization
2. DUT Transmission in the High-Impedance mode
3. DUT Reception in the High-Impedance mode
4. DUT Transmission in the Low-Impedance mode
5. DUT Reception in the Low-Impedance mode

These five steps can be done for any modulation scheme and type.

The Microchip PLC PHY Tester Tool can be used for performing simple PHY tests.

Important: Before starting the test, the user must program both boards with the PHY Tester Tool Firmware provided by Microchip. Prior to programming the DUT, the user will have to adapt the original PHY Tester Tool project to the hardware specifications of their design.

In any case, the process is similar to using the PHY Performance validation Python scripts.

4.2.1 Initialization

Launch the PHY Tester Tool application in the PC and configure the serial port communication:

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- When the boards are supplied and programmed, connect both the DUT and reference boards to the PC by means of a USB cable.

> **Important:** If DUT is not isolated from mains, the cable must be isolated to establish communication.

- Users have to execute two instances of the PHY Tester Tool, which was previously installed in the host(s) PC(s), to enable communication between both boards (one for the DUT and another one for the reference). Note that these two instances may or may not run on the same computer.
- When the application is launched, configure the corresponding COM port for each board in the Serial Port combo box of the *Starting Window*, and select the baud rate combo box of 230400 bauds.
- When the COM port is selected, click the **Connect** button. After few seconds, the button text will change to *Disconnect*. This means that the identification process finished. A new Tab (*Product Information*) is appended to the wizard. Press the **Next** button to go to the following step of the configuration.

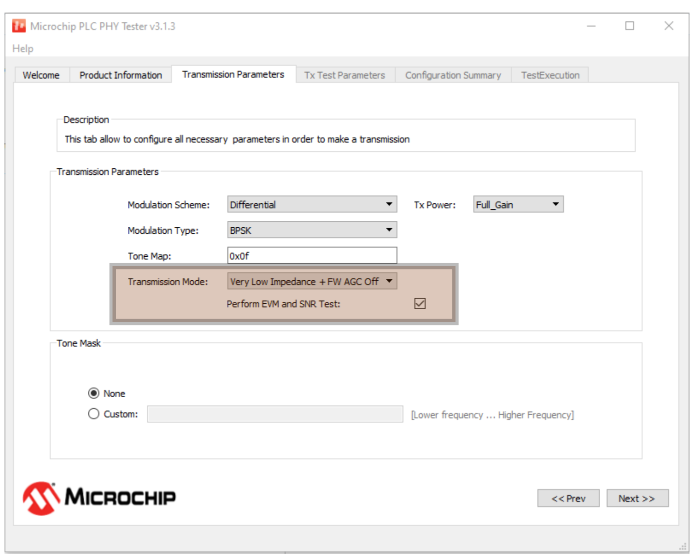
4.2.2 DUT Transmission in Low Impedance Mode

> **CAUTION** For this part of the test, the user has to set up the Configuration B, refer to the Figure 2-6.

Configure the DUT as transmitter:

- Select “Transmission” in the DUT instance of the PHY Tester Tool, then press the **Next** button to continue.
- In the *Transmission Parameters* tab:
  - Select “Perform EVM and SNR Test” in the reception parameters setup.
  - As DUT is connected in the low impedance setup, select the branch configuration as “Very Low Impedance”.
- Click the **Next** button to continue.

Figure 4-1. Transmission Parameters Tab of DUT (Transmitter) for G3-PLC



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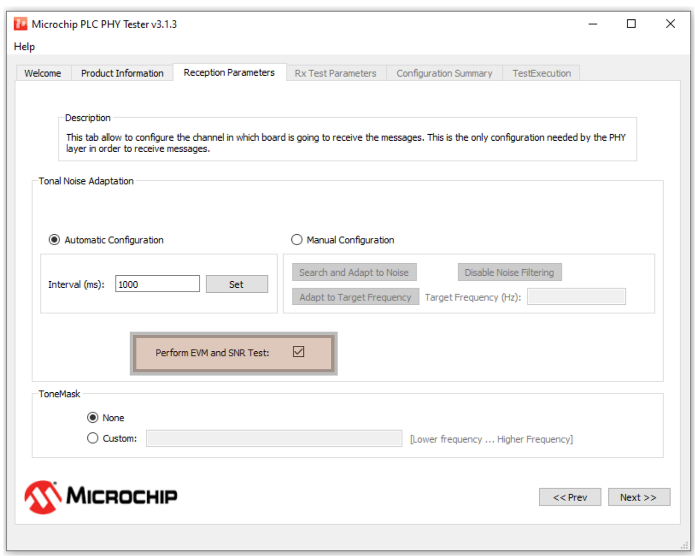
Configure the DUT frames (transmitter):

- Configuration of the frames must be already done with the following values:
  - Time Interval (ms): 100.
  - Number of frames: 100.
  - Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Configure the Reference Board as receiver:

- Select "Reception" in the Reference instance of the PHY Tester Tool, then press the **Next** button to continue.
- In the *Reception Parameters* tab:
  - Select "Perform EVM and SNR Test" in the reception parameters setup.
- Click the **Next** button to continue.

Figure 4-2. Reception Parameters Tab of Reference Device (Receiver)



Configure the Reference Board frames (receiver):

- Configuration of the frames must be already done with the following values:
  - Time Interval (ms): 100.
  - Number of frames: 100.
  - Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Run the test:

1. Set an attenuation level of 0 dB.
2. Perform the transmission test.

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- First, click the **Start Test** button of the receiver PHY Tester Tool instance (Reference board in this case).
- Next, click the **Start Test** button transmitter PHY Tester Tool instance (DUT in this case).
- Test with 0 dB of attenuation starts. Now, the transmission and reception process is observable in both *Test Executions* windows. If messages are different, the receiver will not recognize them as a valid. If the configured interval and number of frames are different, the statistics computed at the end of the test may be inaccurate. In both board's displays, the transmitted/received messages display.

Store the EVM and SNR results in a spreadsheet:

Tip: Remember to mark the following information:
DUT operation (TX or RX) + DUT Position (HIGH or LOW) + AttenuationdB

- Copy the table with the EVM and SNR results that appear in the receiver PHY Tester Tool instance (reference board in this case) by clicking the **Copy Table** button.
- Paste the table in the corresponding spreadsheet created. Marking information can be `TxLOW0dB` where:
  - TX: DUT is operating as transmitter.
  - LOW: DUT is connected in the Low impedance mode.
  - 0 dB: The attenuation between the DUT and the reference is 0 dB.
- The user must repeat the above steps varying the attenuation in each process of measurement (0 dB, 10 dB, 20 dB, 30 dB, 40 dB, 50 dB) and updating the spreadsheet with the obtained values. The user will find some attenuation (normally 50 dB or 60 dB) where the transmission will not be successful.

Remember: More attenuation points provide more accurate results.

4.2.3 DUT Reception at High Impedance Mode

CAUTION For this part of the test, the user has to set up the Configuration A, refer to the Figure 2-6.

Configure the DUT as receiver:

- Select "Reception" in the DUT instance of the PHY Tester Tool, then press the **Next** button to continue.
- In the *Reception Parameters* tab:
  - Select "Perform EVM and SNR Test" in the reception parameters setup.
- Click the **Next** button to continue.

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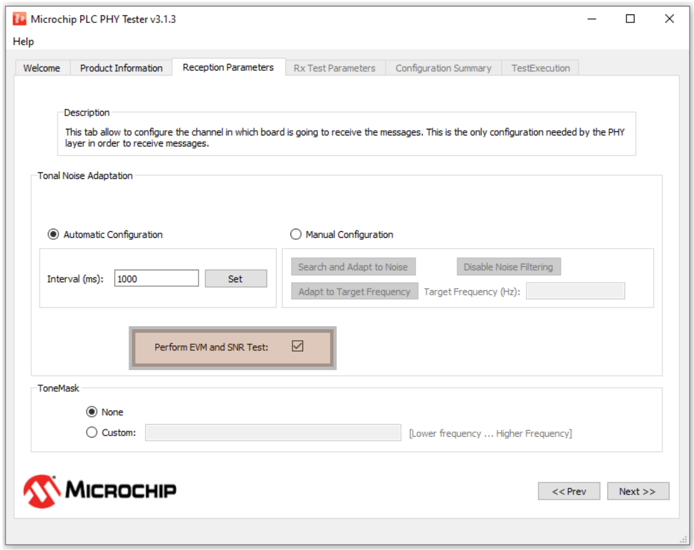
Figure 4-3. Reception Parameters Tab of DUT (Receiver)



Configure the DUT frames (receiver):

- If the EVM and SNR test were checked in the previous tab, the configuration of the frames will be already done with the following values:
  - Time Interval (ms): 100.
  - Number of frames: 100.
  - Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Configure the Reference Board as transmitter:

- Select “Transmission” in the reference instance of the PHY Tester Tool, then press the **Next** button to continue.
- In the *Transmission Parameters* tab:
  - Select the modulation scheme and type.
  - Enable “Perform EVM and SNR Test” in the configuration setup.
  - As a reference is connected in a high impedance network, set the branch configuration as “High Impedance”.
- Click the **Next** button to continue.

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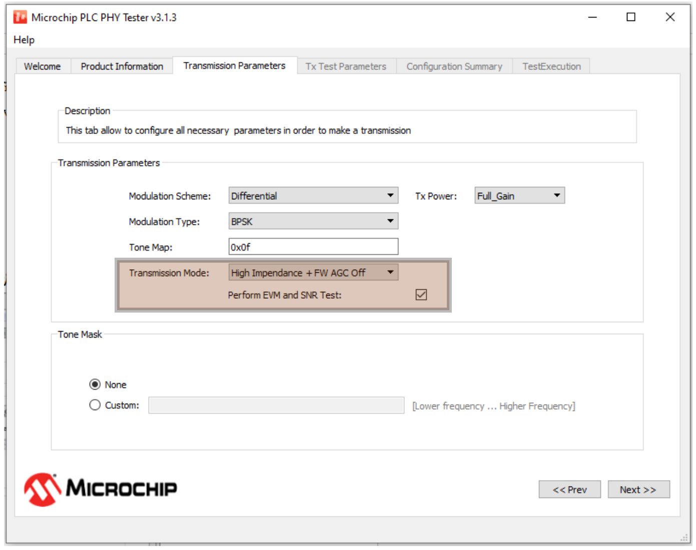
Figure 4-4. Transmission Parameters Tab of Reference (Transmitter) for G3-PLC



Configure the Reference Board frames (transmitter):

- If you have checked the EVM and SNR test in the previous tab, the configuration of the frames will be already done with the following values:
  - Time Interval (ms): 100.
  - Number of frames: 100.
  - Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PLC] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Run the test;

1. Set an attenuation level of 0 dB.
2. Execute the transmission.

- Go to the receiver PHY Tester Tool instance (DUT in this case), then click the **Start Test** button.
- Go to the transmitter PHY Tester Tool instance (Reference in this case), then click the **Start Test** button.
- After that, the test with 0 dB of attenuation starts. Now, the transmission and reception process is observable in both *Test Executions* windows. If messages are different, the receiver will not recognize them as a valid. If the configured interval and number of frames are different, the statistics computed at the end of the test may be inaccurate. In both board's displays the transmitted/received messages display.

Store the EVM and SNR results in a spreadsheet:

Tip: Remember to mark the following information:
DUT operation (TX or RX) + DUT Position (HIGH or LOW) + AttenuationdB

- Copy the table with the EVM and SNR results that appear in the receiver PHY Tester Tool instance (reference board in this case) by clicking the **Copy Table** button.

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- Paste the table in the corresponding spreadsheet created. Marking information can be `RxLOW0dB` where:
  - RX: DUT is operating as receiver.
  - LOW: DUT is connected in the low impedance side.
  - 0 dB: The attenuation between the DUT and the reference is 0 dB.
- The user must repeat the above steps, varying the attenuation in each process of measurement (0 dB, 10 dB, 20 dB, 30 dB, 40 dB, 50 dB) and updating the spreadsheet with the obtained values. The user will find some attenuation (normally 50 dB or 60 dB) where the transmission will not be successful.

Remember: More attenuation points provide more accurate results.

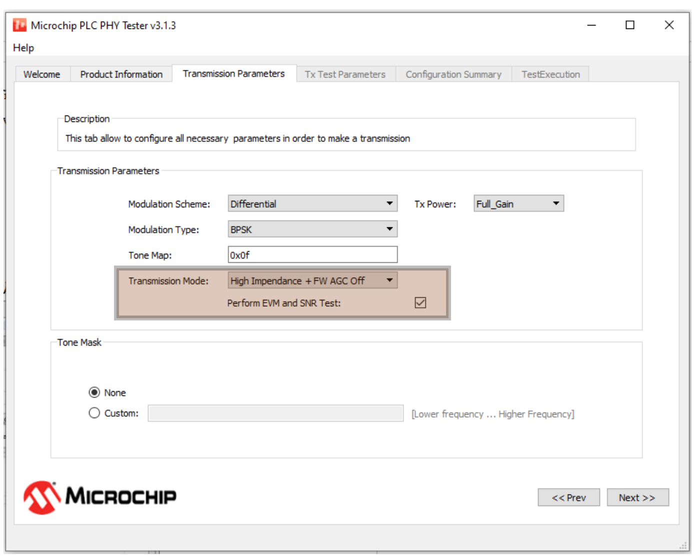
4.2.4 DUT Transmission at High Impedance (CENELEC LISN)

CAUTION For this part of the test, the user has to set up Configuration B. See Figure 2-5.

Configure the DUT as the transmitter:

- Select “Transmission” in the DUT instance of the PHY Tester Tool, then click the **Next** button to continue.
- In the *Transmission Parameters* tab:
  - Select “Perform EVM and SNR Test” in the transmission parameters setup.
  - As DUT is connected in a High Impedance Network, select the branch configuration as “High Impedance”.
- Click the **Next** button to continue.

Figure 4-5. Transmission Parameters Tab of DUT (Transmitter) in G3-PLC



Configure the DUT frames (transmitter):

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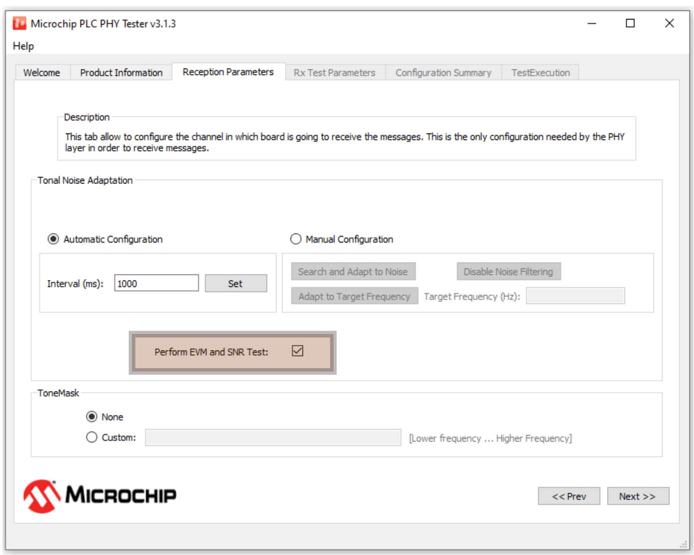
- If the EVM test is checked in the previous tab, the configuration of the frames is already done with the following values:
  – Time Interval (ms): 100.
  – Number of frames: 100.
  – Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Configure the Reference Board as the receiver:

- Select "Reception" in the Reference instance of the PHY Tester Tool, then click the **Next** button to continue.
- In the *Reception Parameters* tab:
  – Select "Perform EVM and SNR Test" in the reception parameters setup.
- Click the **Next** button to continue.

Figure 4-6. Reception Parameters Tab of Reference Device (Receiver)



Configure the reference frames (receiver):

- If the EVM and SNR tests were checked in the previous tab, the configuration of the frames is already done with the following values:
  – Time Interval (ms): 100.
  – Number of frames: 100.
  – Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Run the test:

1. Set an attenuation level of 0 dB.

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2. Execute the transmission.

- Go to the receiver PHY Tester Tool instance (Reference board in this case), then click the **Start Test** button.
- Go to the transmitter PHY Tester Tool instance (DUT in this case), then click the **Start Test** button.
- After that, the test with 0 dB of attenuation starts. Now, the transmission and reception processes are visible in both *Test Executions* windows. If the messages are different, the receiver will not recognize them as valid. If the configured interval and number of frames are different, the statistics computed at the end of the test may be inaccurate. In both boards' displays, the transmitted/received messages show.

Store the EVM and SNR results in a spreadsheet:

Tip: Remember to mark the following information:
DUT operation (TX or RX) + DUT Position (HIGH or LOW) + AttenuationdB

- Copy the table with the EVM and SNR results that appear in the receiver PHY Tester Tool instance (reference board in this case) by clicking the **Copy Table** button.
- Paste the table in the corresponding spreadsheet created. Marking information can be `TxHIGH0dB`, where:
  - TX: DUT is operating as transmitter.
  - LOW: DUT is connected in High Impedance Network (50R).
  - 0 dB: The attenuation between the DUT and the reference is 0 dB.
- The user must repeat the above steps, varying the attenuation in each process of measurement (0 dB, 10 dB, 20 dB, 30 dB, 40 dB, 50 dB) and updating the spreadsheet with the obtained values. The user will find some attenuation where the transmission will not be successful.

Remember: More attenuation points provide more accurate results.

4.2.5 DUT Reception at Low Impedance (PRIME LISN)

CAUTION For this part of the test, the user has to set up Configuration B. See Figure 2-5.

Configure the DUT as the receiver:

- Select "Reception" in the DUT instance of the PHY Tester Tool, then click the **Next** button to continue.
- In the *Reception Parameters* tab:
  - Select "Perform EVM and SNR Test" in the reception parameters setup.
- Click the **Next** button to continue.

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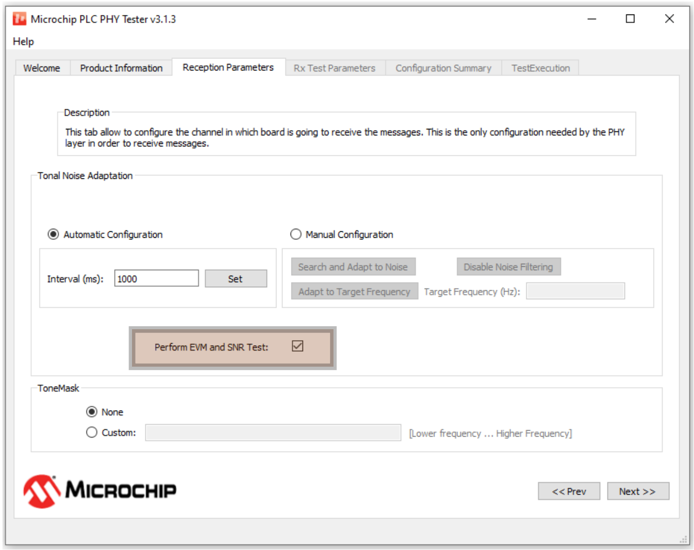
Figure 4-7. Reception Parameters Tab of DUT (Receiver)



Configure the DUT frames (receiver):

- If the EVM and SNR tests were selected in the previous tab, the configuration of the frames is already done with the following values:
  - Time Interval (ms): 100.
  - Number of frames: 100.
  - Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Configure the Reference Board as the transmitter:

- Select “Transmission” in the reference instance of the PHY Tester Tool, then click the **Next** button to continue.
- In the *Transmission Parameters* tab:
  - Select the modulation scheme and type.
  - Enable “Perform EVM and SNR Test” in the configuration setup.
  - As the reference is connected to the 2Ω impedance, select the branch configuration as “Very Low Impedance”.
- Click the **Next** button to continue.

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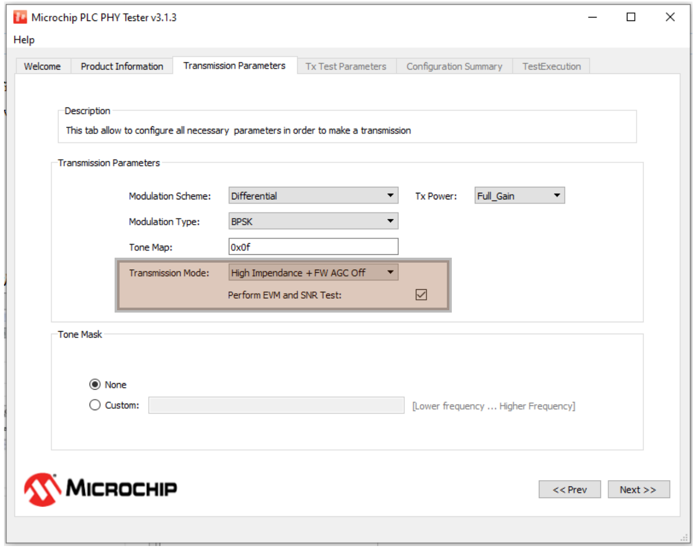
Figure 4-8. Transmission Parameters Tab of Reference (Transmitter) in G3-PLC



Configure the reference frames (transmitter):

- If the EVM and SNR tests were checked in the previous tab, the configuration of the frames is already done with the following values:
  - Time Interval (ms): 100.
  - Number of frames: 100.
  - Message: *[G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY, [G3|PRIME] IS A GREAT INTEROPERABLE WORLDWIDE TECHNOLOGY*.
- Click the **Next** button to continue.
- In the last tab, *Configuration Summary*, check that all values correspond to the desired configuration and wait.

Run the test:

1. Set an attenuation level of 0 dB.
2. Execute the transmission.

- Go to the receiver PHY Tester Tool instance (DUT in this case), then click the **Start Test** button.
- Go to the transmitter PHY Tester Tool instance (Reference in this case), then click the **Start Test** button.
- After that, the test with 0 dB of attenuation starts. Now, the transmission and reception processes are visible in both *Test Executions* windows. If the messages are different, the receiver will not recognize them as valid. If the configured interval and number of frames are different, the statistics computed at the end of the test may be inaccurate. In both boards' displays, the transmitted/received messages show.

Store the EVM and SNR results in a spreadsheet:

Tip: Remember to mark the following information:
DUT operation (TX or RX) + DUT Position (HIGH or LOW) + AttenuationdB

- Copy the table with the EVM and SNR results that appears in the receiver PHY Tester Tool instance (reference board in this case) by clicking the **Copy Table** button.

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- Paste the table in the corresponding spreadsheet created. Marking information can be `RxHIGH0dB` where:
  - RX: DUT is operating as the receiver.
  - HIGH: DUT is connected in the High impedance side (50R).
  - 0 dB: The attenuation between the DUT and the reference is 0 dB.
- The user must repeat the above steps, varying the attenuation in each process of measurement (0 dB, 10 dB, 20 dB, 30 dB, 40 dB, 50 dB) and updating the spreadsheet with the obtained values. The user will find some attenuation (normally 50 dB or 60 dB) where the transmission will not be successful.

Remember: More attenuation points provide more accurate results.

4.3 Results

Results obtained testing the DUT with Python Scripts or the PLC PHY Tester Tool can be compared with the results obtained with Microchip Evaluation Boards.

PHY Performance Validation Python script outputs three files:

- Sqlite Database: This file is the database that includes all the raw information of the test. It includes:
  - `Configurations` Table: Includes the DUT name, date, time and configuration file of the test.
  - `Frames` Table: Includes all the frames with their corresponding parameter values (tx_power, mod_scheme). It is possible to use a SQL database browser for accessing the full information stored by the tests.
- Basic Excel Report: It includes the different signal-to-noise ratios and frame error rates for each modulation in function of the `Attenuation` programmed and a summary tab with only frame error rates for all the modulations.
- Marketing Excel Report: It includes the different signal-to-noise ratios and frame error rates for each modulation in function of the `RSSI calculated` and a summary tab with only frame error rates for all the modulations.

On the PLC Phy Tester Tool, the output is a table that could be copied and pasted in an Excel file similar to the reports obtained with Python Scripts.

4.3.1 Meaning of the Result Graphs in G3-PLC

The meaning of each result graph in the spreadsheets is described in the table below. The name of each one refers to the DUT operation, position and kind of data.

Attention: The “Y axis” of the graphs represents a value measured (dB or dBµV or %) in each test and the “X axis” represents the attenuation value (dB) or RSSI (dBµV) in each test.

Table 4-1. Graph Names Description

Graph Name	Description
RSSI (dBµV)	The Received Signal Strength Indication in dBµV
Noised Symbols	Number of corrupted symbols in payload due to impulsive noise
Corrupted Carriers	Number of corrupted carriers in payload due to narrow/broad band noise
SNR BE (dB)	SNR of corrupted carriers in payload due to narrow/broad-band noise in quarters of dB
SNR Impulsive (dB)	SNR of corrupted symbols in payload due to impulsive noise in quarters of dB

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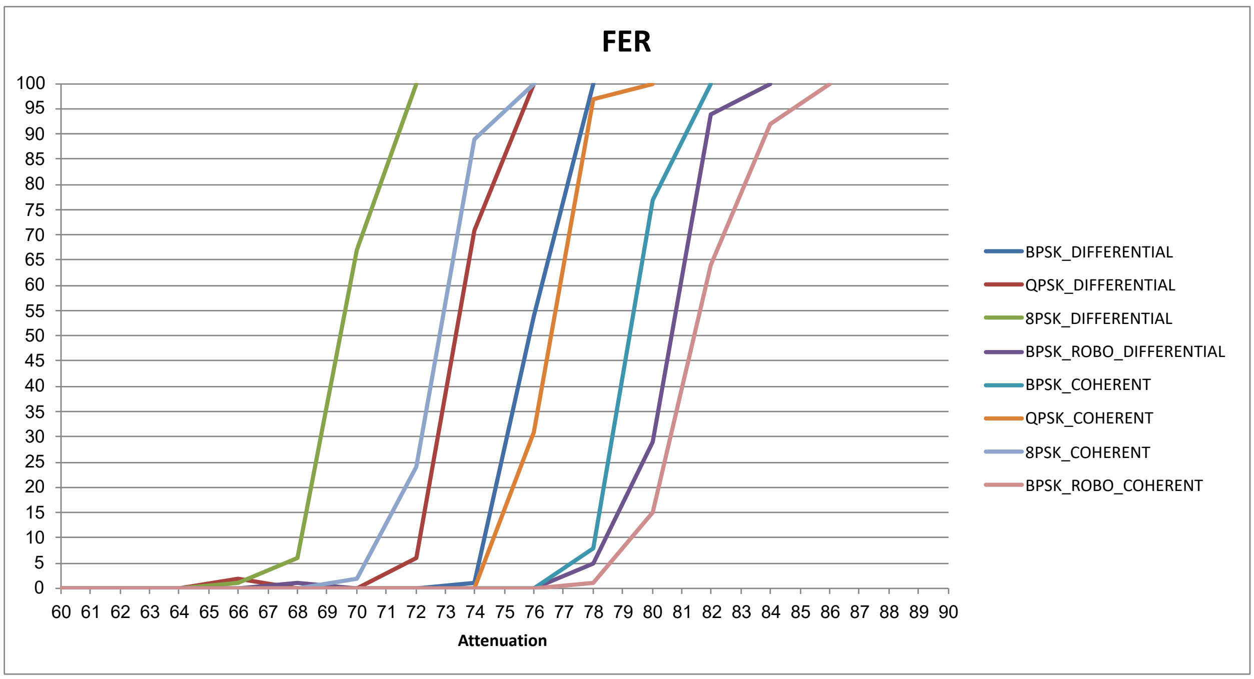
...........continued	
Graph Name	**Description**
SNR Background (dB)	Signal-to-Noise Ratio of the carriers that have not narrow band noise and from the symbols without impulsive noise
SNR Worst Carrier (dB)	Signal-to-Noise Ratio of the most noised carried in quarters of dB
SNR Worst Symbol (dB)	Signal-to-Noise Ratio of the most noised symbol in quarters of dB
SNR Header (dB)	The SNR Header is the SNR of the header in quarters of dB
SNR Payload (dB)	The SNR Payload is the SNR of the payload in quarters of dB
LQI (dB)	The *LQI* parameter indicates the mean SNR per carrier. The LQI is an integer ranging from 0x00 to 0xFF and LQI values in-between are uniformly distributed between these two limits. The LQI value is derived from the average SNR (where averaging is done over all active tones and pilot tones, if present, in the bandplan and overall OFDM symbols in the received packet) where the SNR-to-LQI mapping is: • SNR ≤ -10 dB maps to LQI 0x00 • SNR ≥ 53.75 dB maps to LQI 0xFF • -10 < SNR < 53.75 dB is linearly interpolated between 0x00 and 0xFF (the nominal step size is 0.25 dB) The value analyzed in the spreadsheet is the average of all *LQI* received.
FER (%)	Frame Error Rate, percentage of lost frames against sent frames.

The different value results obtained from the PLC Tester Tool are related to the attenuation programmed on the setup for each test, so it is very important to calibrate the setup to obtain comparable results, mainly the FER.

Figure 4-9. Typical Frame Error Rate Versus Attenuation for G3-PLC on CEN-A with Microchip Reference EKs



Additionally, Python Scripts provide results related to the RSSI calculated on the reception, the simplest way to compare the results between different devices.

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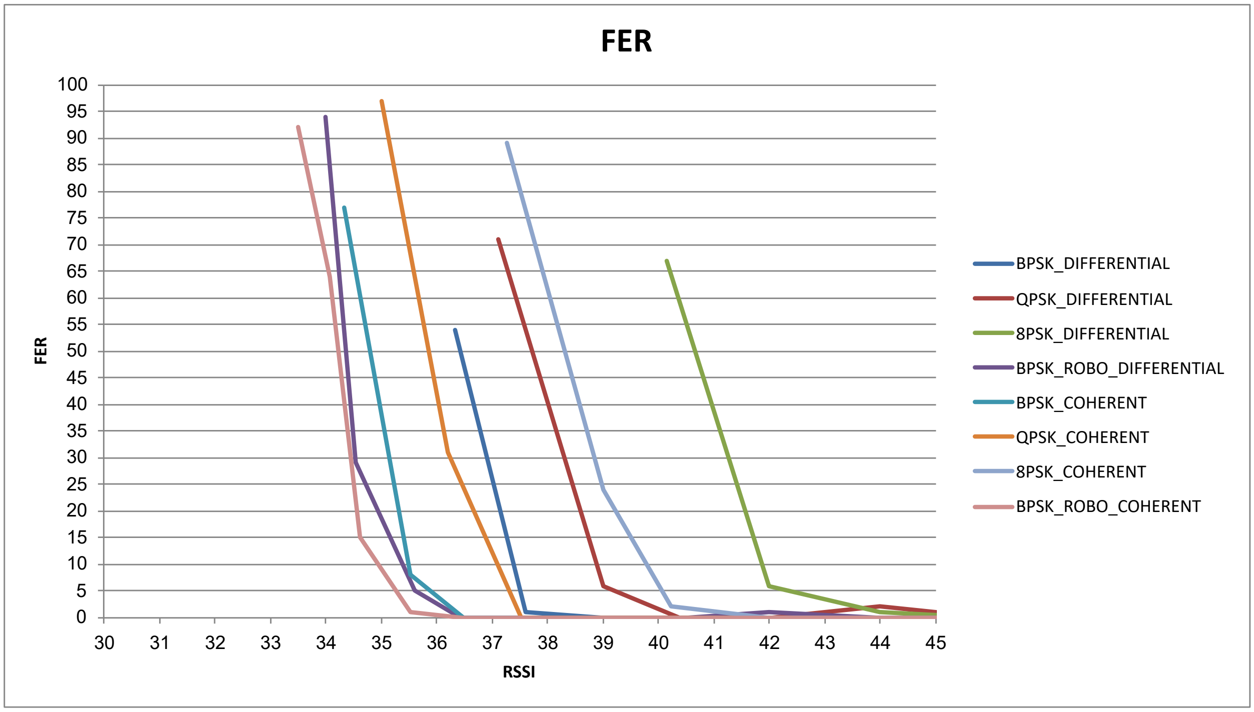
Figure 4-10. Typical Frame Error Rate Versus RSSI for G3-PLC on CEN-A with Microchip Reference EKs



From a theoretical point of view, the FER vs RSSI shows:

- A gain of 3 dB between the modulations BPSK, QPSK, 8PSK.
- Additional gain is obtained using ROBO modulation that adds more energy to each symbol.
- Sensitivity is improved with coherent modulations in exchange for greater complexity in the reception and lower baudrate.

4.3.2 Analysis of the Results in G3-PLC

Physical performance validation script results help to determine if a design is comparable with the Microchip reference designs. These tests allow detection of possible fails in the PLC reception or transmission paths associated with an incorrect PCB layout, incorrect component selection, etc.

Generally speaking, the most important result is the `Frame Error Rate` that represents the number of frames with errors received in the function of the attenuation (ATT) on the path or, more generally, depending on the received signal strength indication (RSSI).

The analysis of `TX path` results helps to determine:

- Transmission Power: Depending on the RSSI value obtained in the results, we can evaluate if the board is transmitting the expected power. If the setup attenuation configuration is the same, the RSSI of the received frames from DUT will be similar to the results for the Microchip reference platform when the power supply source of the power amplifier is the same (12V by default).

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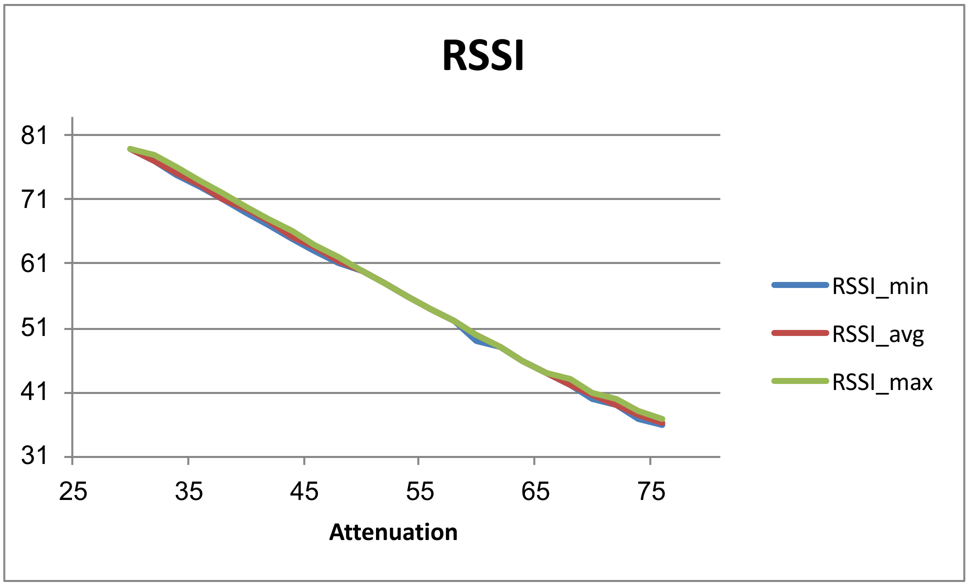
Figure 4-11. Typical RSSI Versus Attenuation on CEN_A with Microchip Reference EKs



- On a clean environment setup, the TX path helps to analyze the transmission linearity of the DUT comparing the SNR_Payload, SNR Background or the LQI average for the same RSSI signal. Differences can be found mainly because of the transformer response on an isolated device but also there are no linear or ideal components, like coils, protection diodes or varistors, if no Microchip reference design BOM is selected.
- On a similar calibration and transmission path, the TX_RMSCALC values must be similar as on Microchip reference boards. Otherwise it is highly recommended to calibrate transmission parameters using 3. Physical TX Calibration.

The analysis of the `RX path` results helps to determine:

- Sensitivity: Depending on the FER vs RSSI value obtained on the results, it can be determined if the background noise of the DUT is lower to the limit to pass G3-PLC certification.

Important: The G3-PLC certification Sensitivity Performance Test defines a maximum of 5% FER at 60 dBuV of RSSI when running the ROBO Differential modulation.

According to the Microchip experience, on a typical meter device connected to AC mains:

Sensitivity (dBuV)	RESULT
<= 45	VERY GOOD
45 < TotalNoise <= 52	GOOD
52 < TotalNoise <= 58	POOR
>58	POTENTIAL ISSUES

- Impulsive Noise: Regarding Noised Symbols, it can be determined if there is impulsive noise on the reception. Additionally, comparing SNR Worst Symbol or SNR Impulsive with the SNR Payload, its influence can be determined. It causes errors in symbols so, a frame can be discarded depending on the impulsive intensity and the length of the frame increasing the frame error rate.

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Figure 4-12. Typical SNR Worst Symbol Versus RSSI on CEN_A Using DBPSK with Microchip Reference EKs

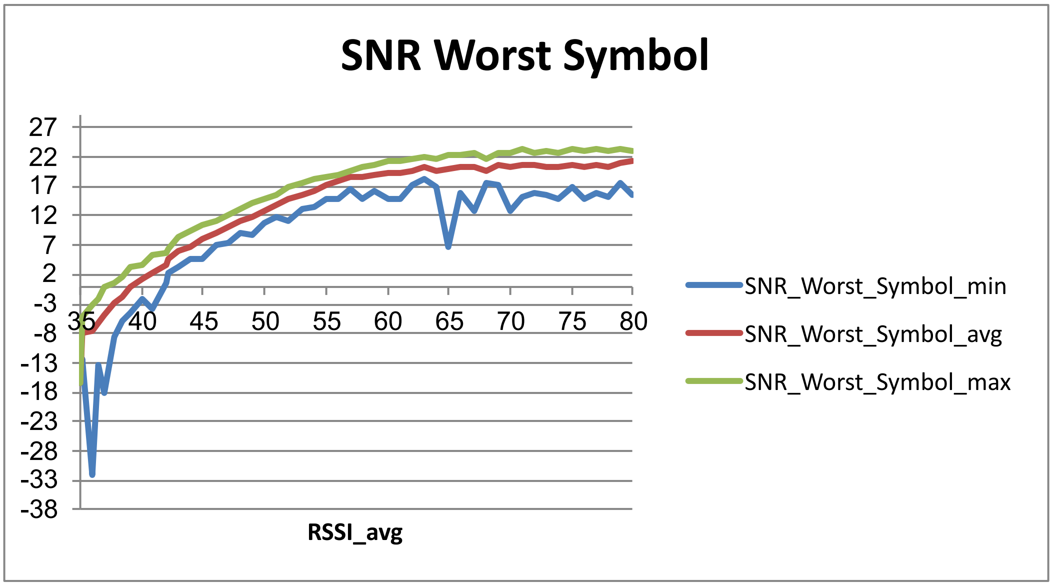

Figure 4-13. Typical SNR Impulsive Versus RSSI on CEN_A Using DBPSK with Microchip Reference EKs

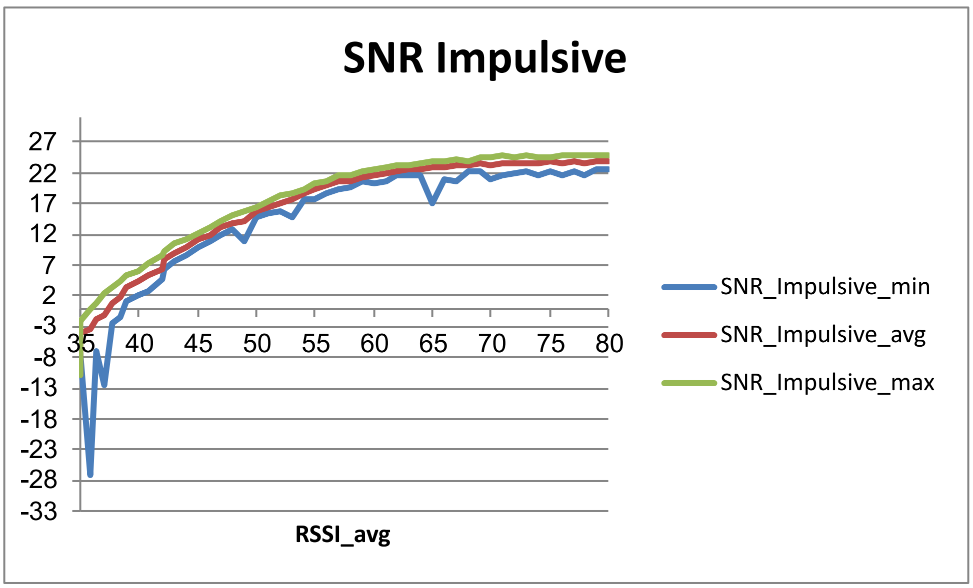

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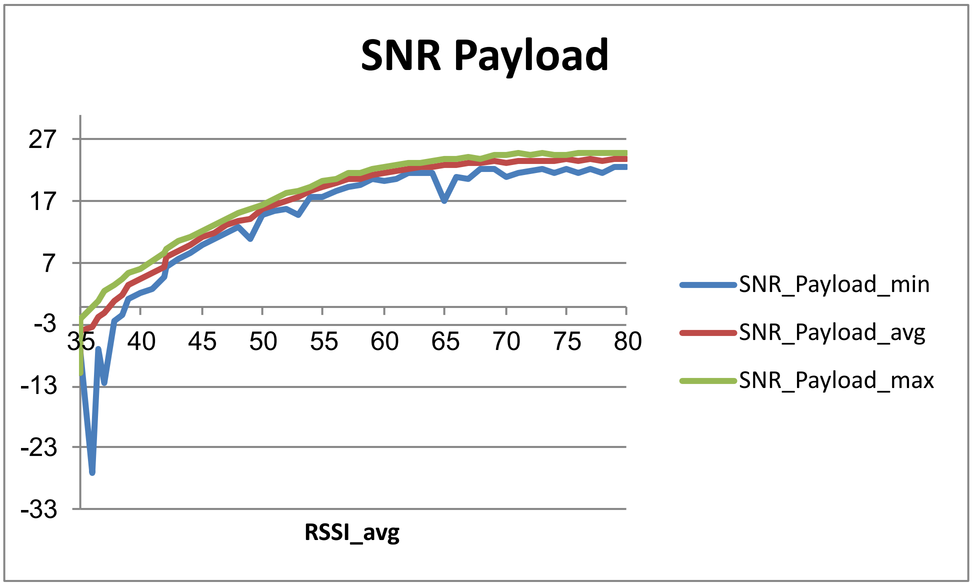
Figure 4-14. Typical SNR Payload Versus RSSI on CEN_A Using DBPSK with Microchip Reference EKs



- Narrowband Noise: Regarding Corrupted Carriers, it can be determined if there is narrowband noise on the reception. Additionally, comparing SNR Worst Carrier or SNR BE with the SNR Payload, its influence can be determined. This kind of noise is continuous and could be identified by accessing the SQLite database and analyzing the RX_SNR_CARRIER result values for each frame sent. It could be identified too on a clean environment when the G3-PLC Tone Map parameter does not correspond with the expected. It can be analyzed with tools like 5. Noise Test.

Figure 4-15. Typical SNR Worst Carrier Versus RSSI on CEN_A Using DBPSK with Microchip Reference EKs

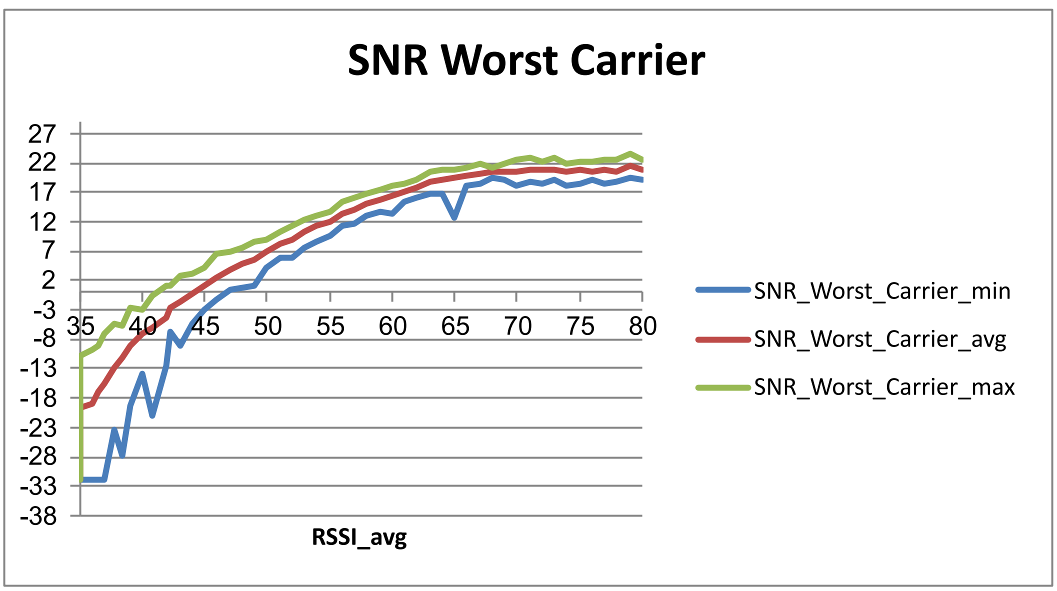


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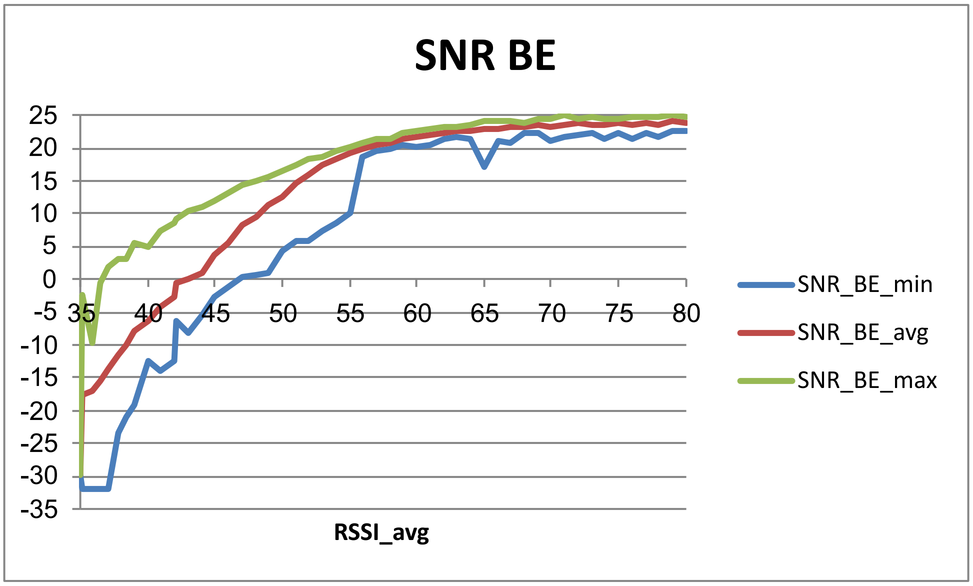
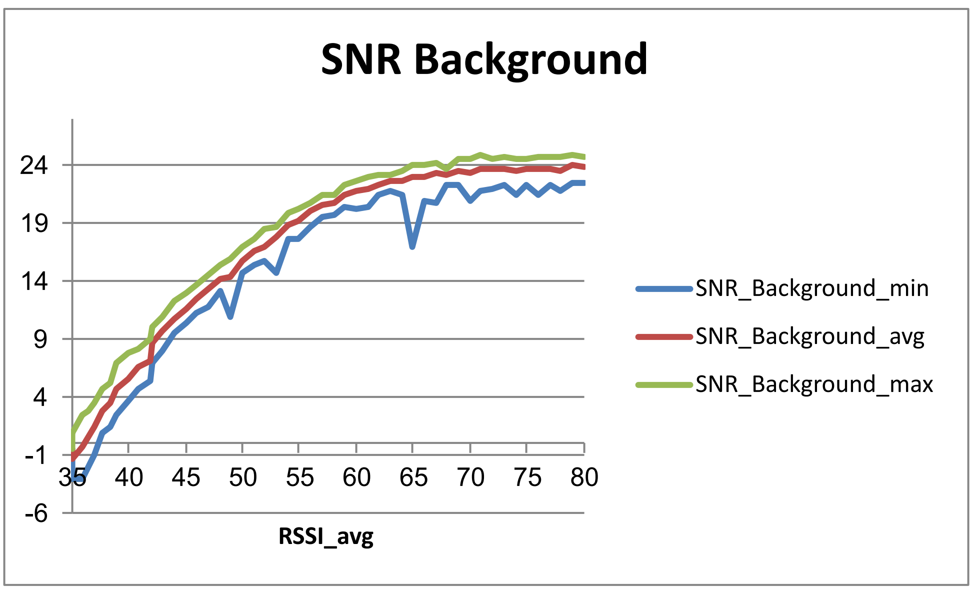
Figure 4-16. Typical SNR BE Versus RSSI on CEN_A Using DBPSK with Microchip Reference EKs



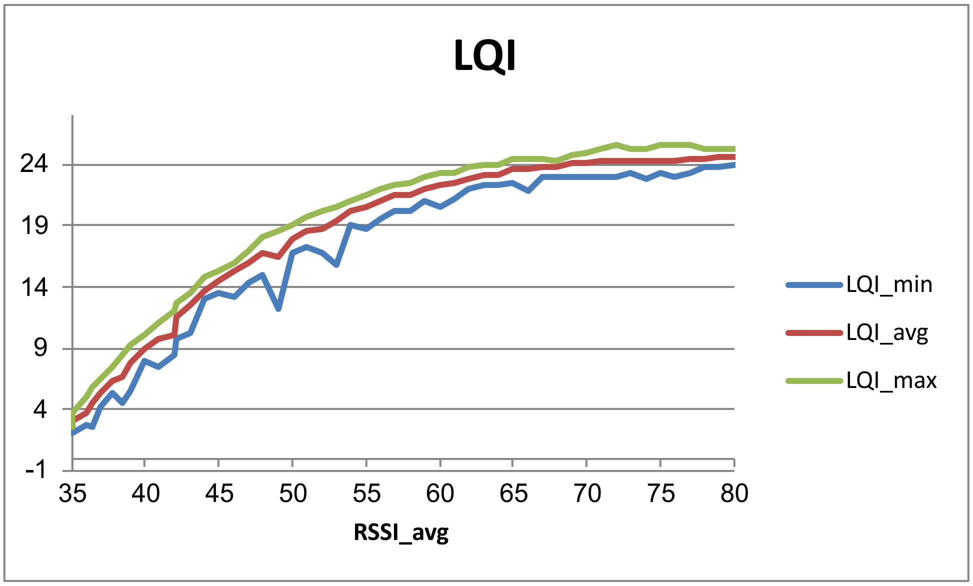
- White Noise: If there is only white Gaussian noise during the test, the `SNR payload`, the `SNR impulsive`, the `SNR be` and the `SNR background` are similar. It is not critical in terms of the reception (because it applies to the complete bandwidth) when the sensitivity limits are not reached and is usually due to thermal noise, wrong PC or component selection.

Figure 4-17. Typical SNR Background Versus RSSI on CEN_A Using DBPSK with Microchip Reference EKs



On a clean environment setup, the RX path helps to analyze the reception linearity of the DUT (mainly transformer response on an isolated device) comparing the LQI average for the same RSSI signal.

Figure 4-18. Typical LQI Versus RSSI on CEN_A Using DBPSK with Microchip Reference EKs



Detected errors on symbols or carriers is due to some impulsive or continuous carrier noise. The common sources for these noises are:

- Continuous Narrow Band Noise: Usually associated with switching frequencies (or harmonics – mainly odd) of AC/DC and DC/DC converters. Follow Microchip PLC HW guidelines.
- Impulsive Noise: Usually associated with other asynchronous transfers like SPI, I^2C, radiated coupling,commonly related to a poor PCB Layout or BOM. Follow Microchip PLC HW guidelines.
- Noise coming from mains.

According to the G3-PLC certification process, there are some limits that need to be accomplished, depending on the modulation and white background noise, regarding Frame Error Reception results with a maximum of 5% of errors:

Table 4-2. G3-PLC Performance SNR Limits Statements for White Noise

Modulation	Unit	CENELEC_A	CENELEC_B	ARIB	FCC
ROBO_D	dB	1	1	2	1
DBPSK	dB	5	5	5	5
DQPSK	dB	8	8	8	8
D8PSK	dB	12	12	12	12
ROBO_C	dB	0	0	0	0
BPSK_C	dB	3	3	3	3
QPSK_C	dB	6	6	6	6
8PSK_C	dB	10	10	10	10

4.3.3 Meaning of the Result Graphs in PRIME

The meaning of each result graph in the spreadsheets is described in the table below. The name of each one refers to the DUT operation, position and kind of data.

Important: The “Y axis” of the graphs represents a value measured (dB or dBμV or %) in each test and the “X axis” represents the attenuation value (dB) or RSSI (dBuV) in each test.

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Table 4-3. Graph Names Description

Graph Name	Description
RSSI (dBμV)	The *rssi* parameter is the Received Signal Strength Indication in dBuV
CINR (dB)	The *cinr* parameter is the Carrier to Interference plus Noise Ratio in dB. It is a measure of the signal quality. It has a correspondency with the EVM defined on the PRIME specification (CINR(dB) = - EVM(dB)).
SNR (dB)	The *snr* parameter is the Signal to Noise Ratio in dB. It is a measure of the signal quality (SNR (dB) ≃ CINR(dB) + 3).
EVM (%)	The *evm* parameter on the graphs is the Error Vector Magnitud in % defined like the porcentage of phase gap (from 0 to 90º) between the received samples and the expected samples. It is a measure of the difference between the ideal (reference) and the measured received samples on the modulation mapping. Depending on the modulation, this error can reach the: • 100% (corresponding with a gap of 90º) for DBPSK (Figure 4-19) • 50% (corresponding with a gap of 45º) for DQPSK (Figure 4-20 • 25% (corresponding with a gap of 22.5º) for D8PSK (Figure 4-21)
EVM Header Avg (%)	This is the average of all the EVM Header received. The EVM Header to average is the carrier's phase error that has more distortion (maximum EVM) in the two header symbols (four symbols if we use the robust mode) for each received frame. As the PRIME header is always in BPSK with convolutional encoder, the maximum error that it is allowed will be 100%, but it is recommended to have a small error without noise and low attenuation in order to support high noise environments.
EVM Payload Avg (%)	This is the average of all the EVM Payloads received (in BPSK, QPSK or 8-PSK). The EVM Payload to average is the carrier's phase error that has more distortion (maximum EVM) in all the payload symbols for each received frame. This average is a global measure that indicates how far (in average) we are of transmitting in one or other modulation. Example: If we have an EVM Payload Average of 20%, we could transmit in 8PSK (without convolutional encoder) without problems, but if we are around 24% or more, we will have to think on more robust modulations. This is done automatically by the MAC layer on a real scenario.
EVM Payload Max (%)	It is the maximum of all the EVM payloads received. It is the carrier with more distortion in all the payloads received. This value can imply that it could not possible to receive some messages in some modulations (without convolutional encoder)..
EVM Payload Acum Avg (%)	It is the average of all the EVM Payload Accumulated received. The EVM Payload Accumulated received is the error average of all the carriers in all the payload symbols. This value is normally small because generally, the carriers that have more distortion are only a few.
BER soft	On the soft-decision decoding process, it correspond with the accumulated distance between the received symbols and the theoretical ones. The result must be as close as possible to 0 to guarantee the correct decoding.
Narrow Band Noise (%)	Percentage of carriers with detected narrow band noise
Impulsive Noise (%)	Percentage of symbols with detected impulsive noise
FER (%)	Frame Error Rate, percentage of lost frames against sent frames.

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Figure 4-19. EVM (%) for DBPSK modulation

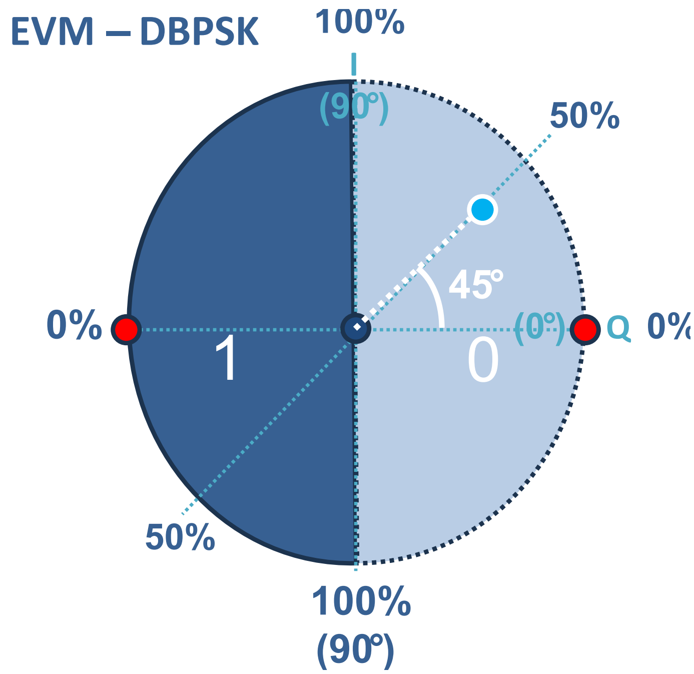


Figure 4-20. EVM (%) for DQPSK modulation

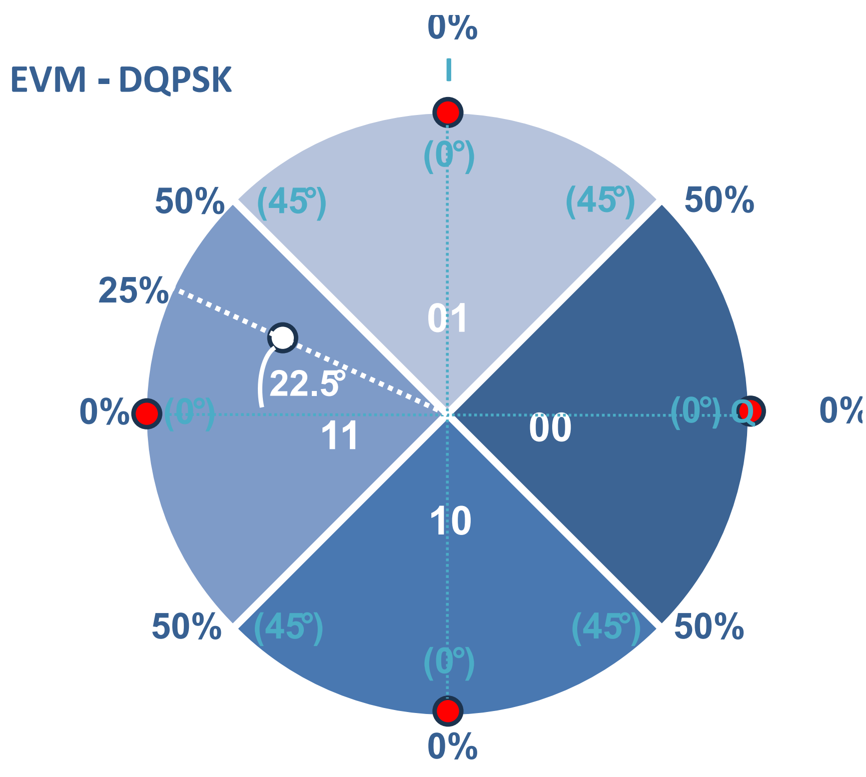
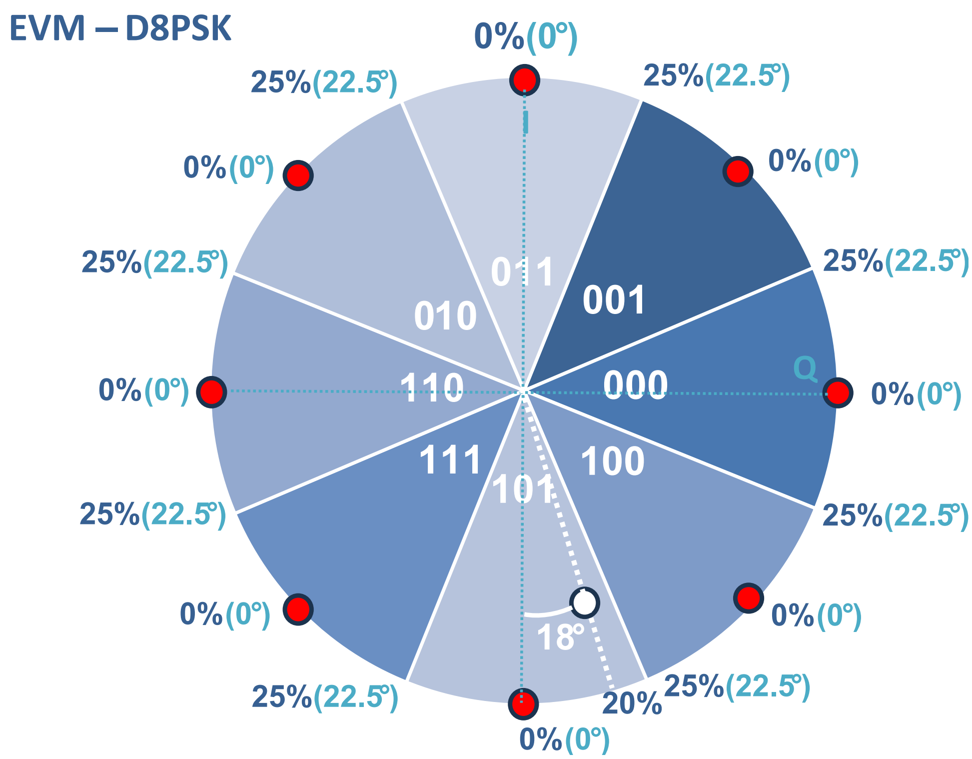
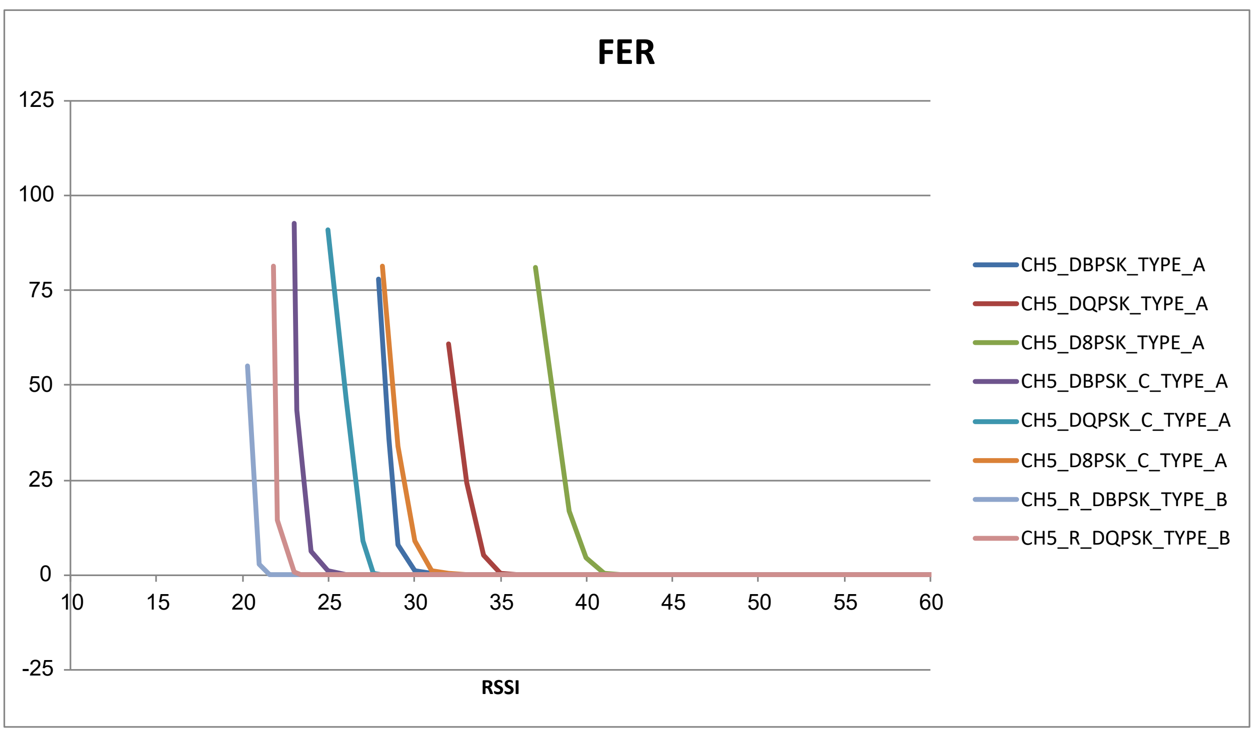


Figure 4-21. EVM (%) for 8PSK modulation



The different value results obtained from the PLC Tester Tool are related to the attenuation programmed on the setup for each test and the corresponding RSSI calculated on the reception, this is the simplest way to compare the results between different devices.

Figure 4-22. Typical Frame Error Rate Versus RSSI for PRIME with Microchip Reference EKs



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From a theoretical point of view, the FER vs RSSI shows:

- A gain of 3 dB between the modulations BPSK, QPSK, 8PSK.
- A gain of about 6 dB when using convolutional coding.
- Additional gain is obtained using robust modulation that adds more energy to each symbol.

4.3.4 Analysis of the Results in PRIME

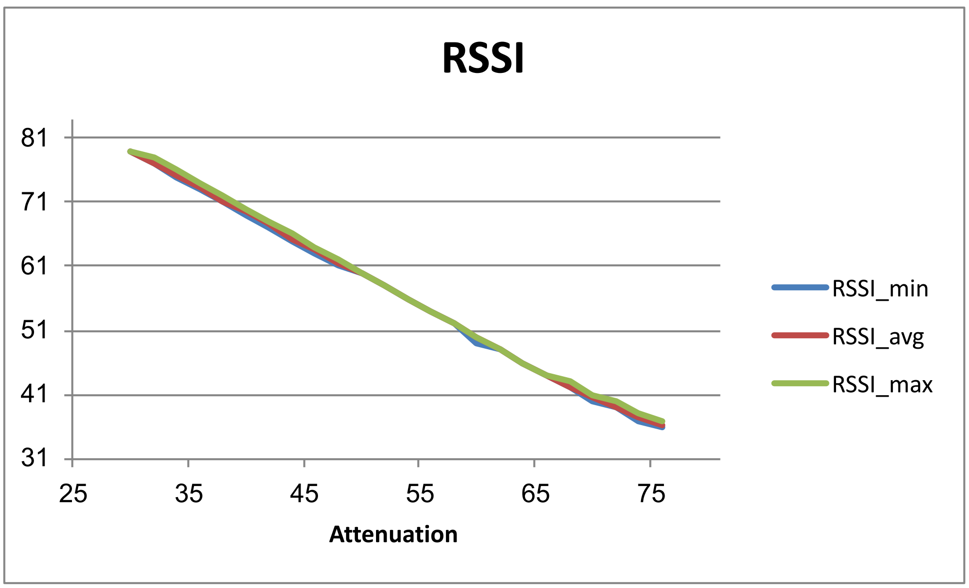
Physical performance validation script results help to determine if a design is comparable with the Microchip reference designs. These tests allow detection of possible fails in the PLC reception or transmission paths associated with an incorrect PCB layout, incorrect component selection, etc.

Generally speaking, the most important result is the `Frame Error Rate` that represents the number of frames with errors received in the function of the attenuation (ATT) on the path or, more generally, depending on the received signal strength indication (RSSI).

The analysis of `TX path` results helps to determine:

- Transmission Power: Depending on the RSSI value obtained in the results, we can evaluate if the board is transmitting the expected power. If the setup attenuation configuration is the same, the RSSI of the received frames from DUT will be similar to the results for the Microchip reference platform when the power supply source of the power amplifier is the same (12V by default).

Figure 4-23. Typical RSSI Versus Attenuation on CHANNEL 5 with Microchip Reference EKs



- On a clean environment setup, the TX path helps to analyze the transmission linearity of the DUT comparing the CINR and EVM for the same RSSI signal. Differences can be found mainly because of the transformer response on an isolated device but also there are no linear or ideal components, like coils, protection diodes or varistors, if no Microchip reference design BOM is selected.
- On a similar calibration and transmission path, the RMSCALC values must be similar as on Microchip reference boards.

The analysis of the `RX path` results helps to determine:

- Sensitivity: Depending on the FER vs RSSI value obtained on the results, it can be determined if the background noise of the DUT is lower to the limit to pass PRIME certification.

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Important: The PRIME certification Sensitivity Performance Test defines a maximum of 0.2% FER on an asymmetric Side-by-Side setup scenario (CENELEC CISPR16-1 LISN in one side and PRIME Adaptation LISN on the other side) without attenuation for interchanges of 2000 frames with a specific format.

According to the Microchip experience, on a typical meter device connected to AC mains and using R_DBPSK modulation:

Sensitivity (dBuV)	RESULT
<= 45	VERY GOOD
45 < TotalNoise <= 52	GOOD
52 < TotalNoise <= 58	POOR
>58	POTENTIAL ISSUES

- Impulsive Noise: It causes errors in symbols so, a frame can be discarded depending on the impulsive intensity and the length of the frame increasing the frame error rate. Not robust modulations can not help to decode properly frames with impulsive noise because interleaver only works in the frequency domain (carriers), not in the time domain (symbols). The impulsive noise on the reception can be determined:
  - Regarding the percentage of impulsive noised symbols.
  - On robust modulations, detecting a BER Soft Maximum far of the BER Soft Average. In not robust modulations BER Soft Max is equal to BER Soft.
  - Detecting an EVM Payload maximum far of the EVM Payload average.
  - It can be analyzed with tests like 5. Noise Test.
- Narrowband Noise: Regarding the percentage of corrupted carriers, it can be determined if there is narrowband noise on the reception. It is detected internally comparing the SNR for each carrier and symbol. This kind of noise is continuous and can be analyzed with tests like 5. Noise Test.

Detected errors on symbols or carriers is due to some impulsive or continuous carrier noise and at the end because of background noise. The common sources of the noise are:

- Continuous Narrow Band Noise: Usually associated with switching frequencies (or harmonics – mainly odd) of AC/DC and DC/DC converters.
- Impulsive Noise: Usually associated with other asynchronous transfers like SPI, I^2C, radiated coupling,commonly related to a poor PCB Layout or BOM.
- Noise coming from mains.
- Thermal noise.

Attention: For more information about how to prevent or solve issues related to noise in the reception, refer to PLC Hardware Design Guidelines application note.

On a clean environment setup, the RX path helps to analyze the reception linearity of the DUT (on an isolated device, the distorsion comes mainly by the transformer response or saturation) comparing the CINR average for the same RSSI signal respecting the Microchip reference. It should be higher than 17dBs for 8PSK according to the PRIME Test Book.

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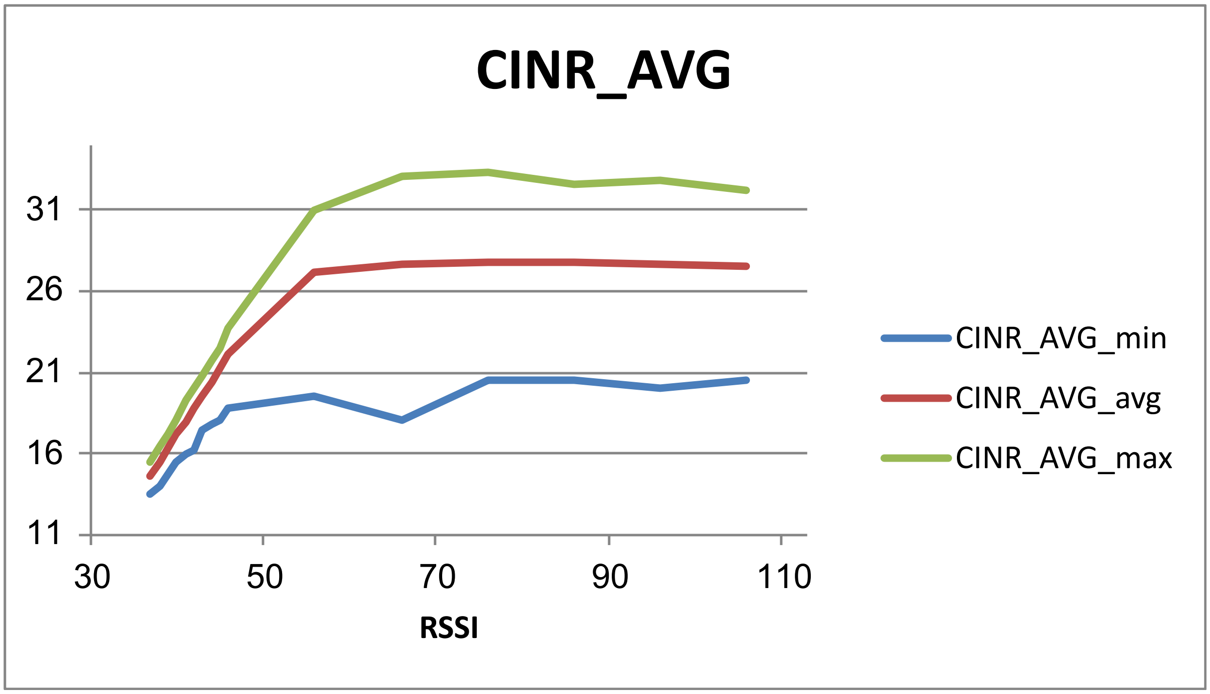
Figure 4-24. Typical PRIME CINR Average vs RSSI results using 8-PSK



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5. Noise Test

Microchip provides a Python script for noise power analysis in the frequency band in use.

The Microchip PLC Noise test is a Python script for the analysis of the noise power per carrier in the working frequency band for the PLC communications. This PC tool requires that the PLC device runs the PHY Tester tool embedded project included in the Microchip PLC firmware package.

Figure 5-1. Microchip PLC Noise Per Carrier Tool

Typical noise sources present on PLC devices are:

- Thermal noise inherent to the components.
- Noise coming from AC-DC or DC-DC power supply switching frequency.
- Noise coming from serial protocols like UART/SPI/I^{2}C because of incorrect PCB Layout.
- Noise coming from coupled radiated signals due to a bad isolation to interferences, signal loops.

Attention: The Total Noise value provides an idea about the performance of the design in terms of sensitivity (signal level of a frame that can be received correctly by the device under test) required. In case of the G3-PLC certification, it is established a maximum limit of 60 dBuV when communicating at ROBO BPSK modulation.

The Noise Test tool use the following PIBs to recover the information:

- REG_VERSION_NUM, for the PLC protocol and working frequency band.
- REG_NOISE_PER_CARRIER, for the estimation of the noise power (in dBμV) in each carrier belonging to the corresponding band for a spectrum analysis on the full frequency bands defined on the PLC standards.

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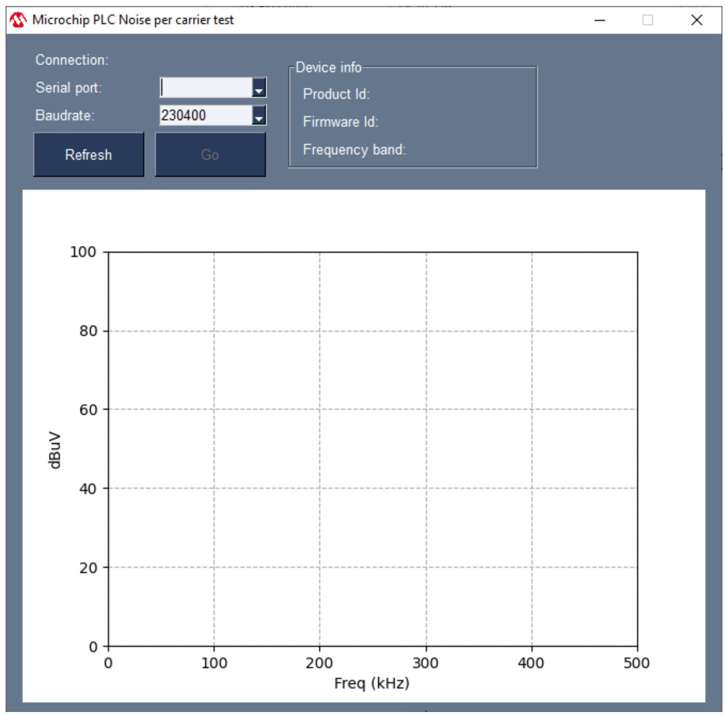
Important: For more information about those PIBs, refer to the Microchip PL360 Host Controller User Guide

The process to perform the noise test is the following:
1. Connect the board programmed with the PHY Tester Tool firmware.
2. Runs the Python script PLCNoiseTest.py (or PLCNoiseTest.exe).
3. Press the **Refresh** button to update the serial ports available.

Figure 5-2. PLC Noise Per Carrier Tool Refresh Serial Ports



4. Select the corresponding serial port and speed (230400 bps by default), then press the **Connect** button.

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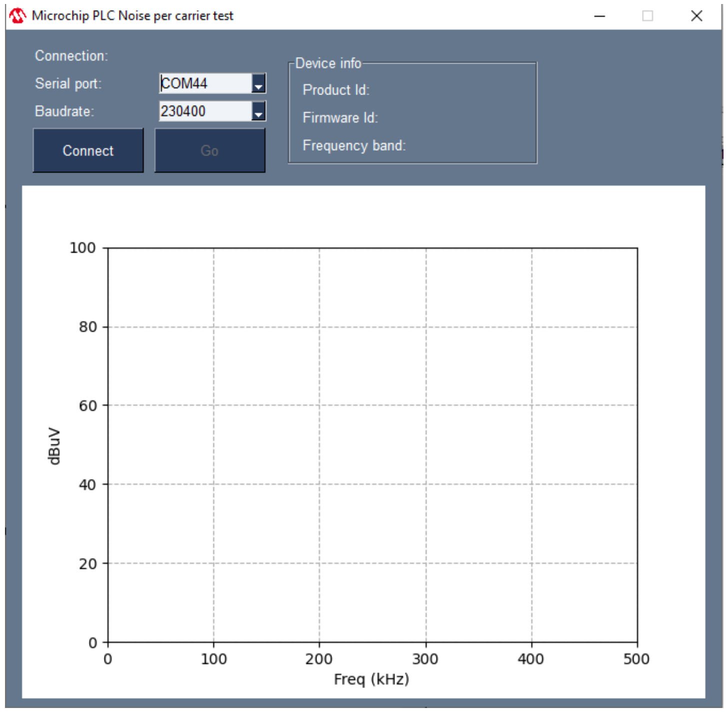
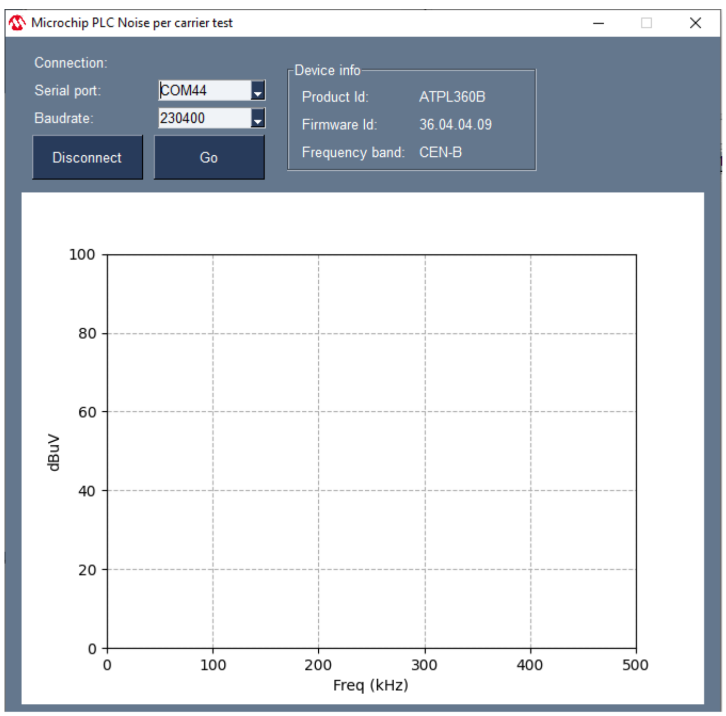
Figure 5-3. PLC Noise Per Carrier Tool Connection



5. If everything is ok, the Device Info information will be filled.

Figure 5-4. PLC Noise Per Carrier Tool Device Info



6. Press the **Go** button, then wait for results on the screen.

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Figure 5-5. PLC Noise Per Carrier Tool Screen Results

7. Analyze the frequency of the highest peaks looking for unexpected noises at different frequencies to determine which could be the source of them. Whether the spectrum is more or less flat in the step band, the noise could be associated to thermal noise, PCB layout (RX path, ground, power supply distribution), and only the Total Noise value is important because it provides an idea about what the RX Sensitivity of the device is in terms of PLC communications. The next table shows recommended values:

Table 5-1. PLC Noise Measurement Results

Total Noise RANGE (dBuV)	RESULT
<= 40	VERY GOOD
40 < TotalNoise <= 47	GOOD
47< TotalNoise <= 55	POOR
>55	POTENTIAL ISSUES

8. Press the **Stop** button when finished. A report with the results are stored in the “report folder” on an Excel file named MCHP_**BAND**_TestNoise_**DATE-TIME**.xlsx.

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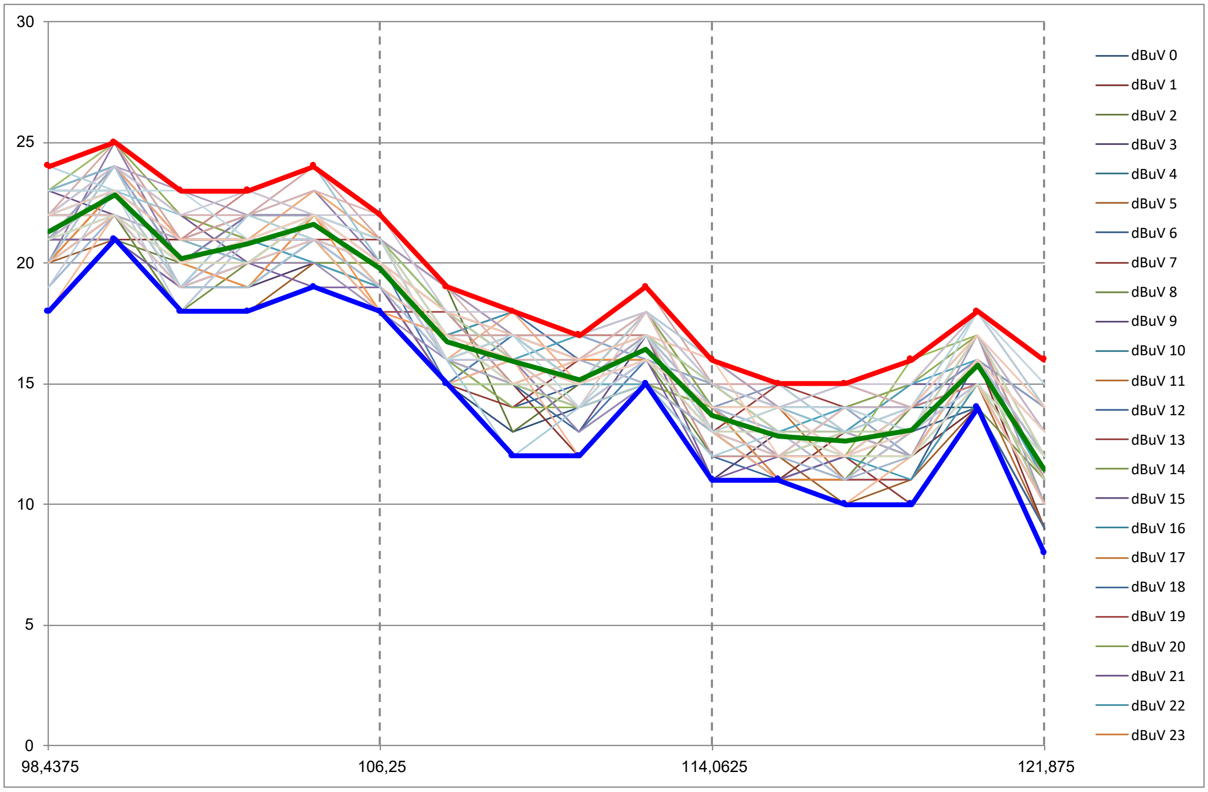
Figure 5-6. PLC Noise Per Carrier Tool Excel Results

FREQ (Hz)	dBuV 74	dBuV 75	dBuV 76	dBuV 77	dBuV 78	dBuV 79	dBuV 80	dBuV 81	dBuV 82	dBuV 83	Min dBuV	Max dBuV	Avg dBuV
98,4375	21	21	24	23	19	22	21	22	23	22	18	24	21,28571429
100	22	22	23	23	23	22	22	24	23	23	21	25	22,8452381
101,5625	20	19	19	21	18	19	20	22	23	20	18	23	20,20238095
103,125	21	21	22	21	21	20	20	23	21	21	18	23	20,77380952
104,6875	22	21	21	22	21	21	22	22	22	22	19	24	21,5952381
106,25	21	20	20	20	20	20	20	22	21	20	18	22	19,79761905
107,8125	17	16	18	18	16	17	17	18	16	17	15	19	16,76190476
109,375	16	16	17	17	16	16	15	18	17	16	12	18	15,94047619
110,9375	14	15	15	16	14	14	15	17	14	15	12	17	15,14285714
112,5	17	16	18	17	16	18	16	18	17	16	15	19	16,45238095
114,0625	13	13	16	16	13	13	13	15	13	14	11	16	13,69047619
115,625	12	12	15	12	13	12	13	14	14	14	11	15	12,82142857
117,1875	13	14	13	12	12	14	12	15	14	12	10	15	12,64285714
118,75	13	14	14	14	13	13	12	15	13	13	10	16	13,05952381
120,3125	17	17	18	17	15	16	15	18	18	16	14	18	15,78571429
121,875	12	13	14	14	12	13	12	16	15	13	8	16	11,44047619

Figure 5-7. PLC Noise Per Carrier Tool Excel Figures



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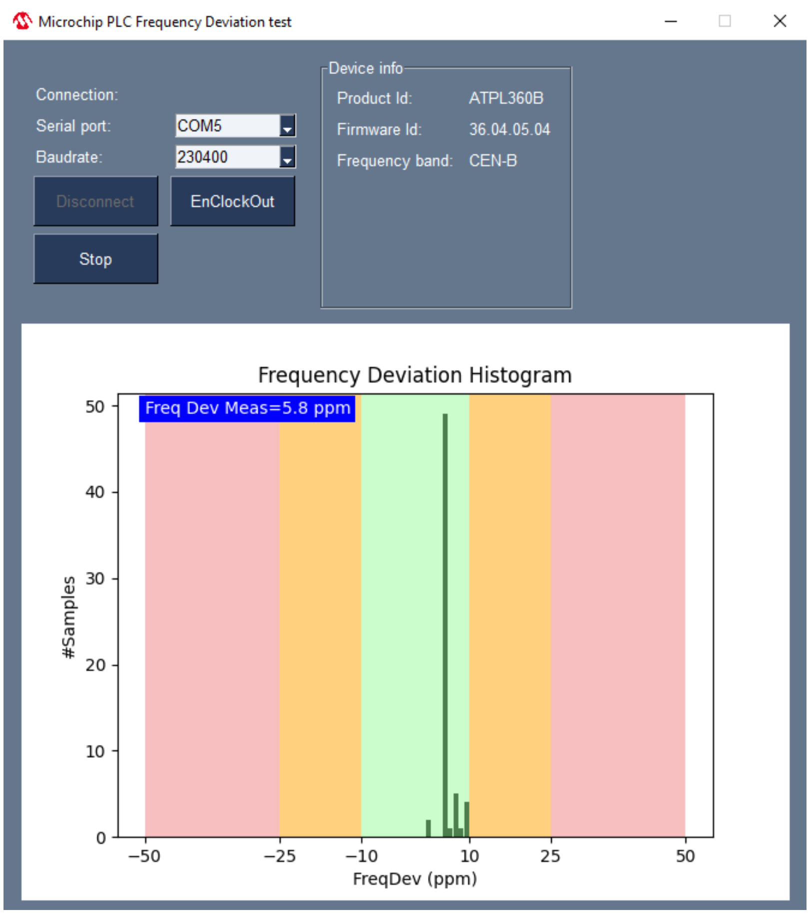
6. Frequency Deviation

PLC communications, based on OFDM, requires a clock synchronization on devices to fulfill with physical requirements implicit to the technology. This topic addresses the process of analysis of this requirement.

The Microchip PLC Frequency Deviation Python script tool requirements are as follows:

- The PLC device in reception runs the PHY Tester tool embedded project included in the Microchip PLC firmware package.
- Primed to process a received frame every second, which will subsequently update a histogram (see Figure 6-1) that illustrates the discrepancy in frequency deviation between devices.

Figure 6-1. Microchip PLC Frequency Deviation Test – Measurement



The scenario of testing is shown in Figure 6-2.

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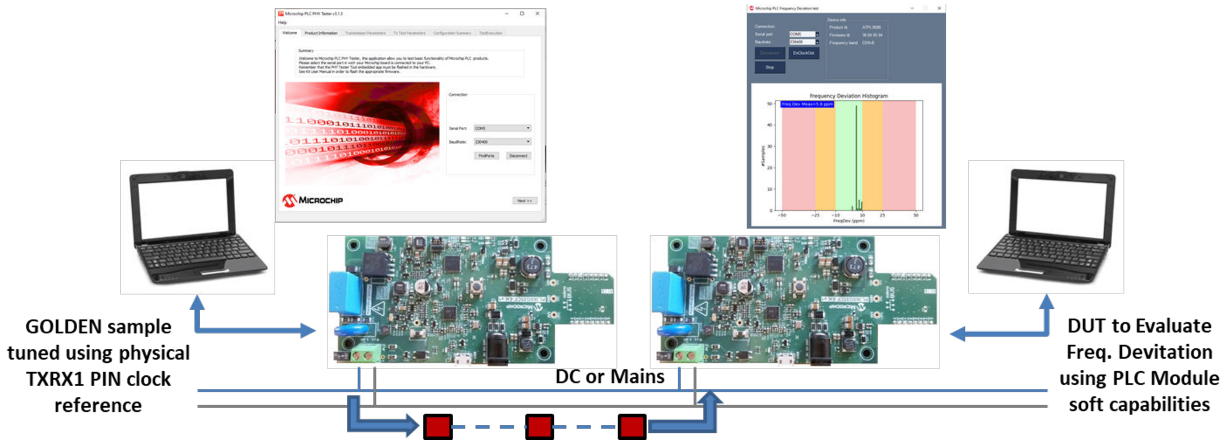
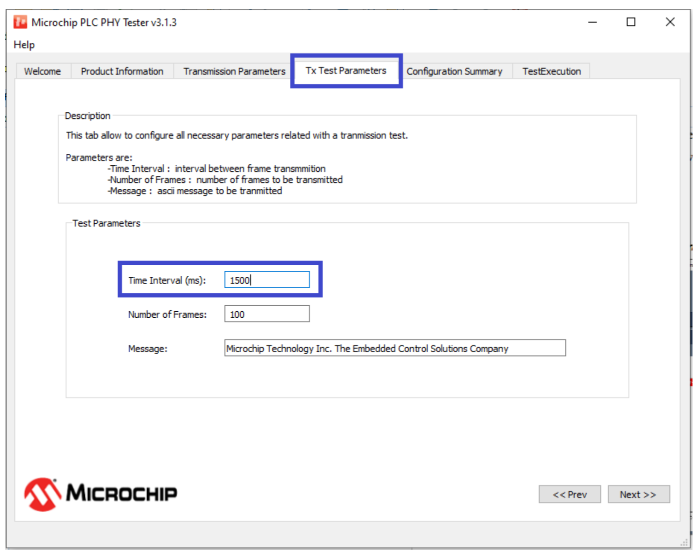
Figure 6-2. Microchip PLC Frequency Deviation Test – Measurement Setup



It requires a tester device calibrated in frequency acting like transmitter controlled with the PHY Tester Tool with a configuration where the time between frames is higher than 1 second (Figure 6-3) and the receiver DUT about which the PLC Frequency Deviation tool acts.

Figure 6-3. Microchip PLC Frequency Deviation Test – PLC PHY Tester Tool TX Configuration



According to the G3-PLC specification, the imperfection of the sampling clock frequency variation can cause inter-carrier interference (ICI). In practice, the ICI caused by a typical sampling frequency variation of about 2% of the frequency spacing is negligible. In other words, considering a ±25 ppm sampling frequency in the transmitter and receiver clocks, the drift of the subcarriers is approximately equal to 8 Hz, that is approximately 0.5% of the selected frequency spacing. Considering these selections, the number of usable subcarriers is set to 36 for the CENELEC-A band, 16 for the CENELEC-B band and 72 for the FCC band.

The system clock frequency tolerance is +/-25 ppm maximum and the transmit frequency and symbol timing is derived from the same system clock oscillator. As this tolerance must be accomplished on the full temperature range of use for the device, a good criteria in testing is to measure the frequency deviation in both extremes of the temperature range.

The worst case analyzing the frequency deviation in reception is with Coherent ROBO frames with the maximum length on the frequency band with the full tone masking/mapping including CRC (2

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bytes). An indirect way to find this kind of problems in frequency deviation appear when running certification performance tests that use coherent modulations evaluating the device in reception.

Important: According to the PRIME specification, the system clock shall have a maximum tolerance of +/-50 ppm, including ageing.

Tip: Follow the process of crystal selection and hardware configuration by reading the Microchip Application Note AN2716 – Crystal Selection Guidelines for PLC Devices.

The main purpose of Frequency Deviation tool are:

- To tune the capacitors selected for the crystal configuring a PIN of the PLC device as clock output of the internal 24Mhz signal to be analyzed with an oscilloscope or spectrum analyzer.
- To identify the frequency deviation between devices analyzing the received frames.

The Frequency Deviation tool use the following PIBs to recover the information:

- REG_PPM_CALIB_ON: Enable the oscillator clock signal to go out through the TXRX1 pad.
- REG_SFO_ESTIMATION_LAST_RX: Estimation of the clock frequency deviation on the last received PDU.

Important: For more information about those PIBs, refer to the Microchip PL360 Host Controller User Guide.

To use the tool just follow these steps:

1. Mount the 24 MHz clock crystal capacitors according to the Microchip reference design and guidelines followed on the crystal selection application note.
2. Configure the device with the firmware project `phy_tester_tool`.
3. Run the PLCFreqDev tool or Python script.
4. Configure the `Serial Port` and the `Baudrate` for connecting to the board (push the `Refresh` button, if necessary, for updating the serial ports available).

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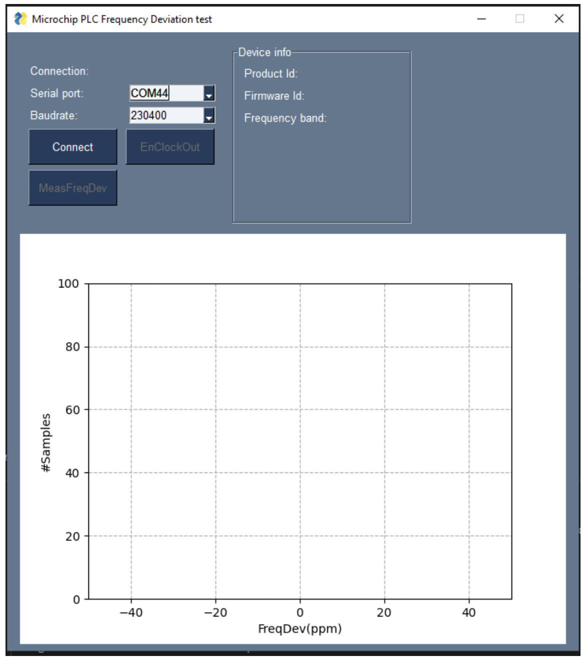
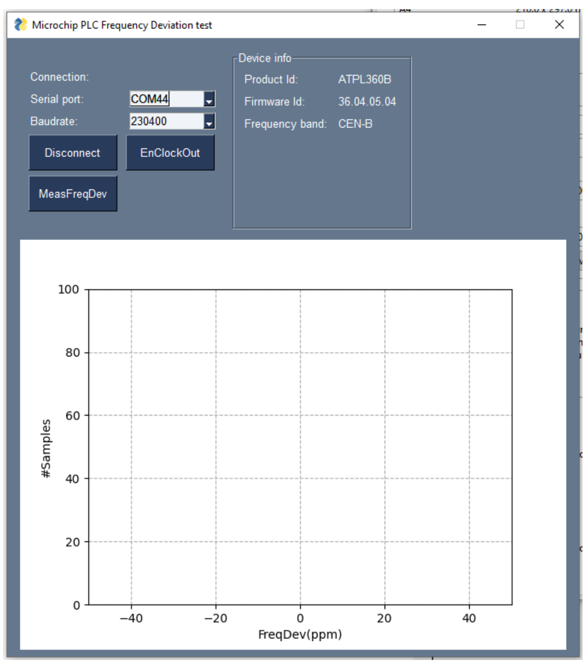
Figure 6-4. Microchip PLC Frequency Deviation Test – Connection



5. Push the **Connect** button for accessing the board. The Device Info layout is updated with information from the firmware.

Figure 6-5. Microchip PLC Frequency Deviation Test – Device Info



6. Now depending of the purpose to use the tool:
   – To calibrate the frequency clock source: press the **EnClockOut** button that enables the availability of the PLC module reference clock signal on the TXRX1 pad (24 MHz). The clock frequency can be adjusted by modifying the values of the associated capacitors as explained in the application note Crystal Selection Guidelines. It is recommended to tune the tester board to be as close as possible to 24MHz because the frequency deviation is a differential measurement between receiver and transmitter.

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- To analyze the frequency deviation: press the **MeasFreqDev** button that starts the application obtaining the frequency deviation from received frames inside the PLC module and showing the histogram with a maximum refresh of 1 second.

The results can be analyzed according the table Table 6-1.

Table 6-1. PLC Frequency Deviation Measurement Results

Absolute Frequency Deviation Meas RANGE (ppm)	RESULT
<= 10	VERY GOOD
10 < FreqDevMeas <= 20	GOOD
20 < FreqDevMeas <= 25	POOR
>25	POTENTIAL ISSUES

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7. RF Tests

7.1 Introduction

The PLC communication standards evolved to hybrid solutions where radio frequency is used to create alternative routes between devices in the same network.

The RF tests help to evaluate the transmission and reception capabilities of the RF subsystem of devices running PLC Hybrid protocols. These tests cannot be considered as a full validation of the RF subsystem or any design guideline of the RF subsystem.

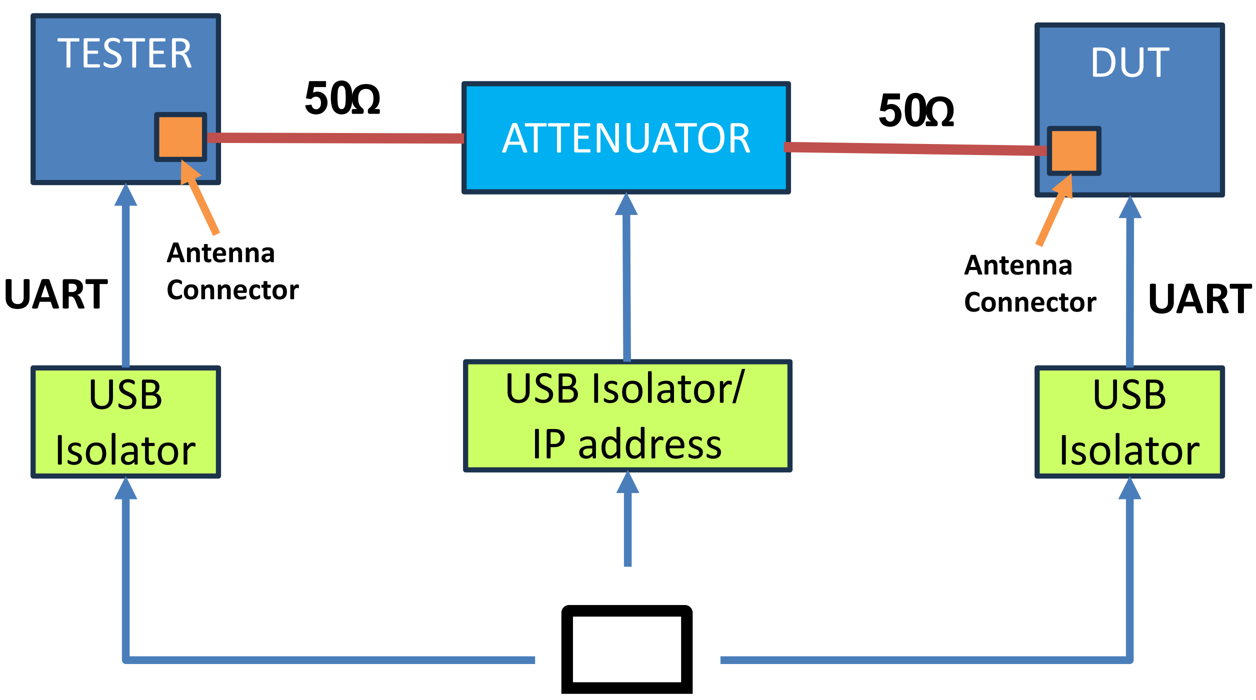
Microchip provides the necessary firmware/software to perform the different measurements in a similar way than for PLC evaluation:

- Microchip PLC PHY Tester Hybrid Firmware – The apps_phy_tester_hybrid_tool embedded project configures PLC and RF PHY layers and its serial interface to communicate with any application that implements the corresponding Universal Serial Interface (USI). This firmware is loaded into the DUT and the Reference Device. For the DUT, the user has to adapt the original PHY Tester Hybrid Tool embedded project to the hardware specifications of the design.
- The Python® Library Package, *mchp_plc_tools* – It includes a specific package for RF evaluation: mchp_rf_tools_phy_tester_public.
- The Python PLC PHY Performance Validation Package – Includes on the SNR and EVM Analysis section a simple example for RF analysis.

7.2 Setup

To use the RF test setup, as shown in the figure below, it is required that the device under test has the option to use a wired connection with an impedance of 50 Ohm to connect to a variable attenuator. The effects of the antenna, such as near/far field, gain, radiation diagram in the system are not evaluated.

Figure 7-1. RF Test Setup



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Tip: These RF tests provide an idea of the design performance compared to Microchip AT86RF215-EK reference design.

The RF Tests are as follows:

- Verify the reception and transmission levels of any PLC Hybrid prototype. This prototype is also named as "*Device Under Test*" (DUT).
- Consist of transmitting and receiving predefined or random RF messages between the DUT and a *Reference Device* or *Tester*. Both devices are connected to a side-by-side setup. The shipping message process between devices is repeated in both ways, increasing the attenuation level step-by-step.
- Refer to the RSSI (in dBm) measurement (the only information received from the RF transceiver) and the corresponding frame error rate obtained iterating along different attenuation in the channel.

The measurement requires a configuration point-to-point that simulates a transmission path between a tester and the DUT. To reduce the radio propagation effects out of the cable connection, the transmitted power is configured to be minimum. The setup is ready to connect a digital attenuator (controlled through Virtual Instrument Software Architecture VISA or handled by hand) in the middle to simulate a transmission path with different attenuation to measure transmission power and sensibility.

7.3 RF Measurement Process with Python

Important: Install Microchip Python Libraries and dependencies for the corresponding Python version needed by the PHY Performance script TestATT_rf.py for RF validation.

Once boards are supplied and programmed with the PLC PHY Tester Hybrid Firmware, connect both DUT and reference boards to the PC by means of a USB/Serial Port cable (better if it includes any kind of ferrite chocke filter).

1. Open and edit the **TestATT_rf.config** file.
2. Configure the property **name** to form the name of the output files, and identify the results.
3. Configure the **paths** setting:

- **rx**: Data from Reference Tester to DUT. Helps to analyze DUT reception path.
- **tx**: Data from DUT to Reference Tester. Helps to analyze DUT transmission path.
- **tx_rx**: First evaluates TX path, then RX path.
- **rx_tx**: First evaluates RX path, then TX path.

4. Configure the **port_dut** and **port_reference** that defines the connection to the DUT and the Reference Tester.

- **COMX:SPEED**– Local Serial COM Port connection and speed baud rate (bps).
- **IP:PORT**– TCP/IP connection. Physical connection to DUT and Reference Tester is always a Serial Port connection, but it can be accessed remotely through additional software like socat, COMbyTCP, SerialToI.

Configure the **band_op_mode** setting corresponding to the operating frequency band an mode:

- SUN_[FSK|OFDM]_BAND_[863|866|870|915|915A|915B|915C|919|920|920B]_OP[M|T][1-12]

Configure the **fec** to test with or without convolution coding (by default off as specified on G3).

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Configure the platform **device** under test. By default RF215.

Configure the attenuation plan for the test:

- Configure the Attenuator Instrument **attenuator_device_id** using the **Virtual instrument software architecture** (VISA) address. If the setup does not include a digital attenuator instrument, just comment the line and the script will ask for manual attenuation setting during the test.
- Configure the **att_start**, **att_step** and **att_stop** values.
- Configure the **att_int_fixed** reducing the transmitted power in TX (0 to 31). Default 30 to reduce the air coupling.
- Configure the **att_ext_fixed** present on the setup. Typically:
  - att_ext_fixed = 80 dB = 2 * 40 dB (Fixed Att on antenna connectors in both sides).

If needed, configure the message length, **msg_len** between:

- **max**: Configures the maximum physical size for the frame.
- **fixed**: Configures the value defined by **msg_len_value**.
- **random**: Configures a random value between the minimum and maximum allowed.

If needed, configure the message content: **msg_content**:

- **random**
- **fixed**

Additionally, there are some configurations for file report sending and storing:

- **email_server**: Email server for SMTP request.
- **email_notification**: Email address for sending the reports (no SQL databases included).
- **repo_server**: Windows shared folder where store reports and databases.

Run the **TestATT_rf.py** script according to customer-specific configuration.

```
C:\PHYperformance\python.exe TestATT_rf.py -c TestATT_rf.config
C:\Python37\lib\site-packages\visa.py
Physical RF DUT Testing Tool
AGILENT TECHNOLOGIES, J7211A, MY52201152, A.00.04
Physical RF Testing Tool
Completed: 0.000000 %
ATTENUATION: 0
Sent 010 of 010 (362) - Received 010 (-102 dBm)
FER = 0.000000 %
Completed: 4.761905 %
ATTENUATION: 1
Sent 010 of 010 (056) - Received 010 (-103 dBm)
FER = 0.000000 %
Completed: 9.523810 %
...
ATTENUATION: 19
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue0 (311) - Received 001 (-121 dBm)
FER = 90.000000 %
Completed: 95.238095 %
ATTENUATION: 20
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
```


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```
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
FER = 100.000000 %
END of -> ATTENUATION: 20
FINISHED with completed: 100.000000 %
Completed: 0.000000 %
ATTENUATION: 0
Sent 010 of 010 (386) - Received 010 (-101 dBm)
FER = 0.000000 %
Completed: 4.761905 %
ATTENUATION: 1
Sent 010 of 010 (030) - Received 010 (-102 dBm)
FER = 0.000000 %
Completed: 9.523810 %
ATTENUATION: 2
Sent 010 of 010 (256) - Received 010 (-104 dBm)
FER = 0.000000 %
Completed: 14.285714 %
...
ATTENUATION: 18
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue0 (166) - Received 001 (-118 dBm)
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue

FER = 90.000000 %
Completed: 90.476190 %
ATTENUATION: 19
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue0 (205) - Received 001 (-120 dBm)
Empty Rx Queue
Empty Rx Queue0 (097) - Received 002 (-119 dBm)
Empty Rx Queue
Empty Rx Queue

FER = 80.000000 %
Completed: 95.238095 %
ATTENUATION: 20
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue
Empty Rx Queue

FER = 100.000000 %
END of -> ATTENUATION: 20
FINISHED with completed: 100.000000 %
Test finished, Duration:0:03:29
Sending e-mail report to username@domain.com
E-mail sent.
```

The results obtained can be compared with the results obtained with Microchip Evaluation Boards and checked with the transmission and reception characteristics of RF215 transceiver.

PHY Performance Validation Python script for RF outputs two files:

- Sqlite Database: This file is the database that includes all the raw information of the test. It includes:
  - `Configurations` Table: Includes the DUT name, date, time and configuration file of the test.
  - `Frames` Table: Includes all the frames with their corresponding parameter values. It is possible to use a SQL database browser for accessing the full information stored by the tests.

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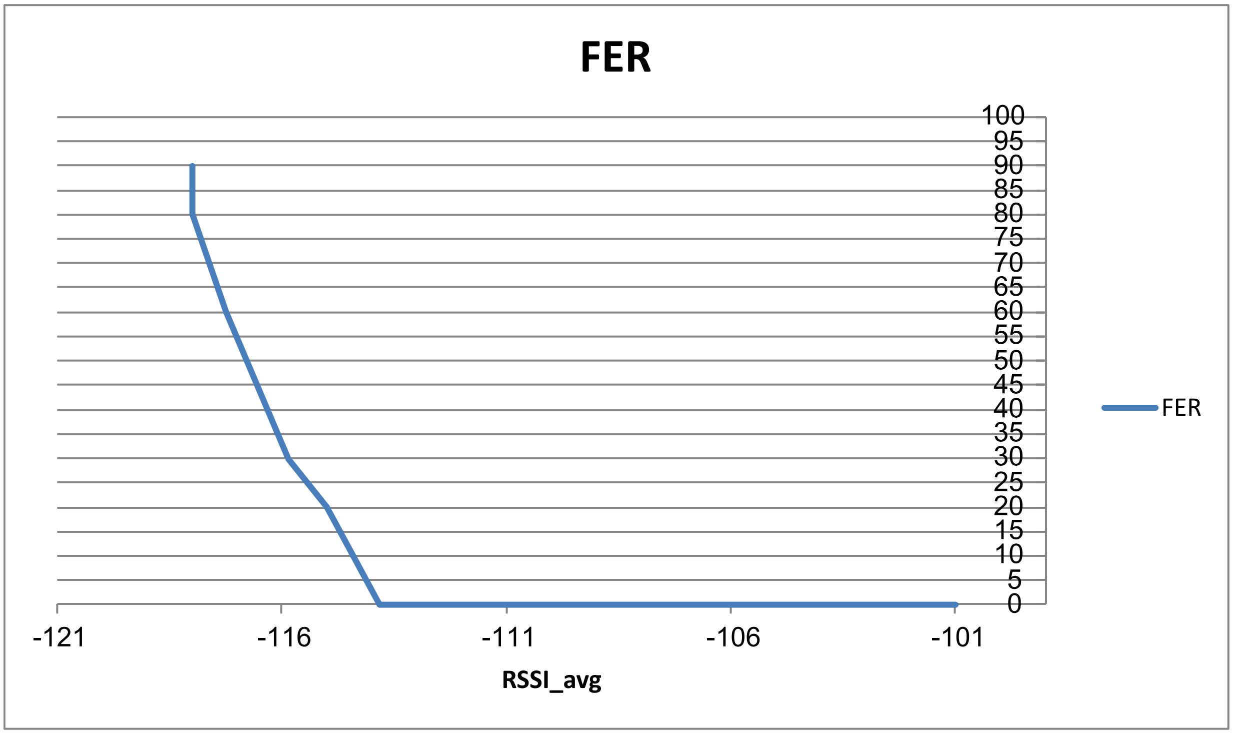
- Basic Excel Report: It includes the frame error rates in function of the `Attenuation` programmed and the `RSSI` received.

Figure 7-2. Typical FER vs RSSI on a RF setup



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4. *Performance Test Suite for G3-PLC Device Certification*, 2023
5. *Narrowband OFDM PLC Specifications for PRIME Networks*, 2023
6. *Performance Test Suite for PRIME Device Certification*, 2023
7. *PL360* Data Sheet, reference DS70005364, on the Microchip website
8. *PL460* Data Sheet, reference DS60001666, on the Microchip website
9. *AT86RF215* Data Sheet, on the Microchip website
10. *G3-PLC Firmware Stack* User Guide, reference DS50003232, on the Microchip website
11. *PRIME Firmware Stack* User Guide, reference DS50002759, on the Microchip website
12. *PLC Host Controller User's Guide*, reference DS50002738, on the Microchip website
13. *PLC Hardware Design Guidelines*, reference DS00004700, on the Microchip website
14. *PLC Tools Python Package* User Guide, 2022
15. *PHY Performance Tool Package*, 2023

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9. Abbreviations

Acronyms and Abbreviations	Description
AKA	Also Known As
BPSK	Binary Phase Shift Keying
CENELEC	European Committee for Electrotechnical Standardization
DBPSK	Differential Binary Phase Shift Keying
DUT	Device Under Test
FW	Firmware
IEC	International Electrotechnical Committee
EVM	Error Vector Magnitude
LISN	Line Impedance Stabilization Network
LQI	Link Quality Indicator
MCU	Microcontroller Unit
MTP	Manufacturing Test Procedure
OFDM	Orthogonal Frequency Division Multiplexing
PCB	Printed Circuit Board
PHY	Physical Layer
PLC	Power-Line Communications
PPDU	PHY Protocol Data Unit
QPSK	Quadrature Phase Shift Keying
RMS	Root Mean Square
RSSI	Received Signal Strength Indicator
SNR	Signal-to-Noise Ratio
USI	Universal Serial Interface

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10. Revision History

10.1 Revision B - 01/2024

Introduction	Updated to consider Hybrid profile.
2. Setup	Updated to consider PL460 and Hybrid profile in section 2.1. Hardware Requirements. Updated to consider Hybrid profile in section 2.2. Software and Tools Requirements.
4. SNR and EVM Tests	Updated to consider generic PLC transceiver references and PRIME (mainly the meaning and analysis of the results).
6. Frequency Deviation	Updated to consider PRIME.
7. RF Tests	Added this section common for hybrid profiles.

10.2 Revision A - 02/2023

Document	Initial document

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