APPLICATION NOTE

Atmel AT01777: SAM4L Schematic Checklist

Atmel 32-bit Microcontrollers

Features

- Power circuits
- Reset circuit
- ADC connection
- Clock and crystal oscillators
- JTAG and SWD debug ports
- Capacitive Touch (CATB) Module
- USB connection
- Segment LCD connection
- Miscellaneous topics
- Suggested reading
- Patents and Trademarks
  - Atmel® QTouch® (patented charge-transfer method)

Introduction

A good hardware design comes from a proper schematic. Since SAM4L devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a SAM4L design.

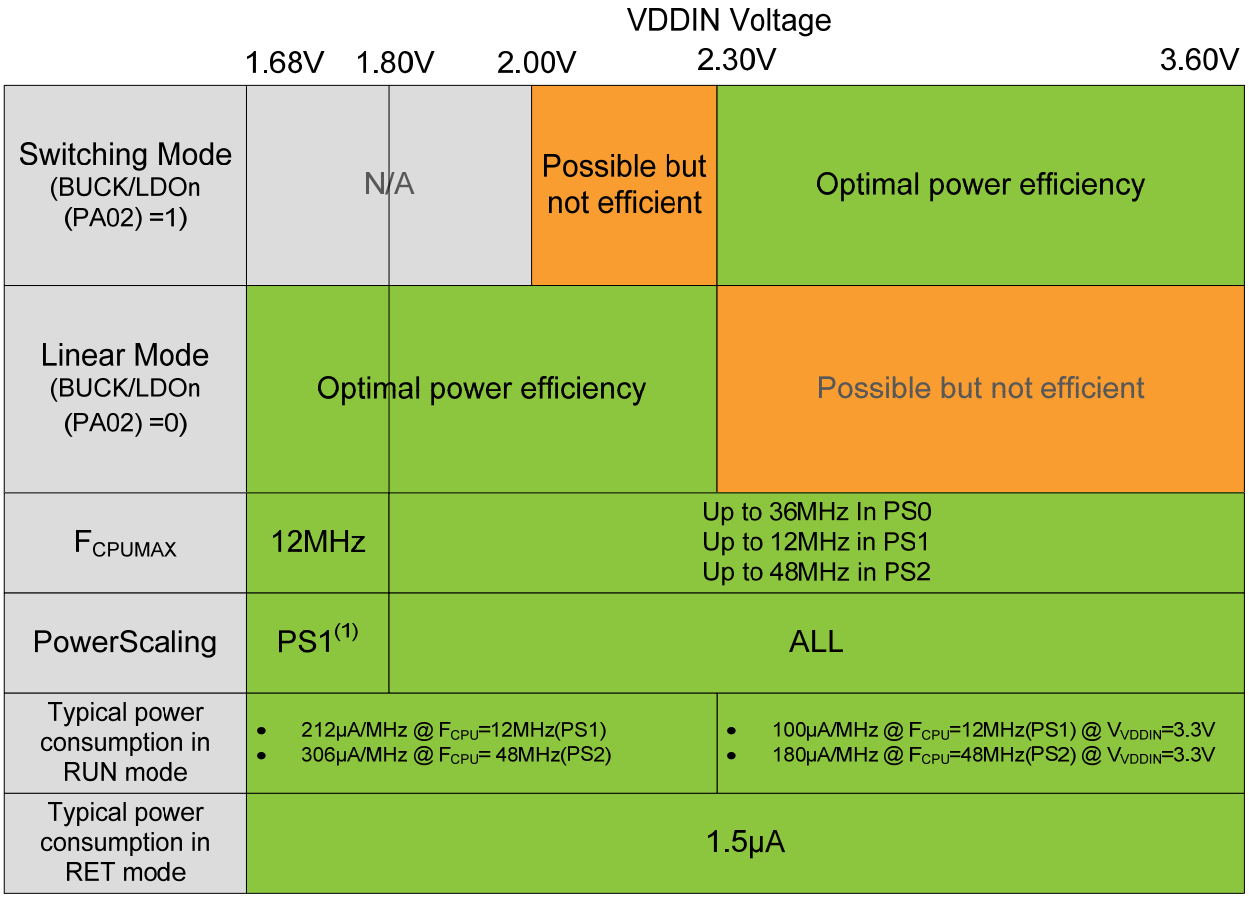
1. Power Circuit

1.1 Choosing the Right Regulator Mode for the Application

ATSAM4L internal voltage regulator has two modes: switching or linear mode. This configuration has to be set once for all when designing the schematic by using a pull up or a pull down on the BUCK/LDOn pin depending on the chosen mode. The BUCK/LDOn is sampled on power on reset and remains available for the application after reset.

Figure 1-1 shows the mandatory requirements for the power supply in the two modes:

Figure 1-1. Regulator Choice vs. VDDIN Voltage.



Note 1. The SAM4L boots in PS0 on RCSYS(115kHz), then the application must switch to PS1 before running on higher frequency (<12MHz)

Table 1-1 details the pros and cons of the two modes:

Table 1-1. Regulator Mode Choice.

Criteria	Switching mode	Linear mode
BOM Cost	Requires an external 22µH inductor. Requires a good quality ceramic capacitor on VDDCORE. (see minimum requirements in the datasheet)	Minimal cost.
Component size	Requires an external 22µH inductor.	Minimal size.
Emitted noise	Proper filtering and decoupling is needed in noise sensitive applications due to switching regulator. Note: The SAM4L has a “Stop/Restart switching” feature that can be use to stop the switching noise for the time to make an ADC measurement and then restart the regulation loop after measurement is done. Refer to the Peripheral Event Controller section of the datasheet.	Minimal emitted noise.

1.2 Switching Mode

Figure 1-2. Switching Mode Example Schematic.

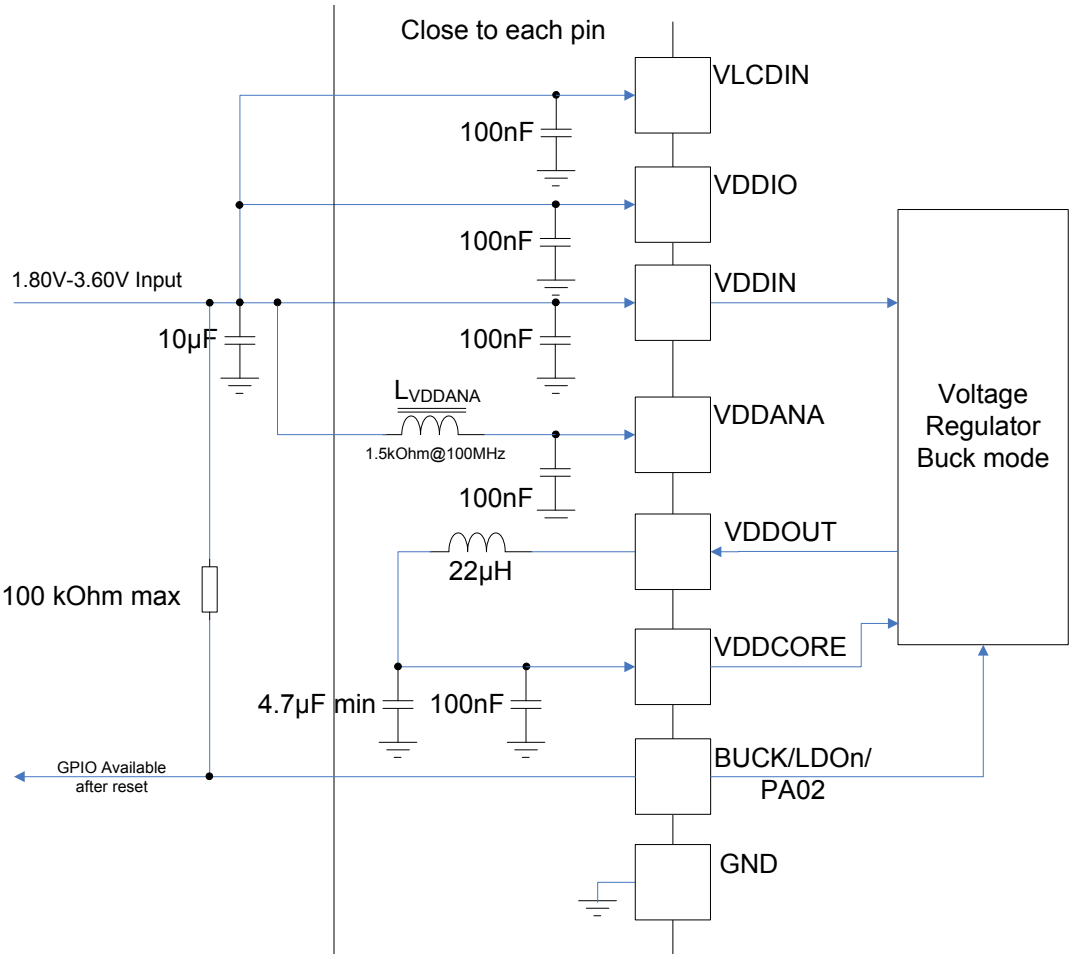


Table 1-2. Switching Mode Power Supply Checklist.

☑	Signal name	Recommended pin connection	Description
	Supply input	VDDIN = VDDIO = VDDANA = VLCDIN [3]	The supply pins must be at the same potential.
	VLCDIN[3]	1.80V to 3.60V 100nF X7R [1][2] Decoupling/filtering capacitor	Powers the LCD voltage pump. Decoupling/filtering capacitors must be added to minimize voltage ripple.
	VDDIO	1.80V to 3.60V 100nF X7R [1][2] Decoupling/filtering capacitor	Powers I/O lines, the general purpose oscillator (OSC), the 80MHz integrated RC oscillator (RC80M). Decoupling/filtering capacitors must be added to minimize voltage ripple.
	VDDANA	1.80V to 3.60V 100nF X7R [1][2] Decoupling/filtering capacitor	Powers the ADC, the DAC, the Analog Comparators, the 32kHz oscillator (OSC32K), the 32kHz integrated RC oscillator (RC32K) and the Brown-out detectors (BOD18 and BOD33). Decoupling/filtering capacitors must be added to minimize voltage ripple.
	VDDIN	1.80V to 3.60V Decoupling/filtering capacitors 100nF X7R [1][2] and 10µF [1]	Powers I/O lines and internal voltage regulator. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Connect a 22µH inductor from VDDOUT to VDDCORE	Output of the on-chip voltage regulator. Switching frequency: 1MHz. Inductor recommended reference: Wire Wound type with DC resistance <0.7Ω and saturation current >300mA (Ex: Murata LQH3NPN220MJ0 or Taiyo Yuden NR4018T220M).
	VDDCORE	Decoupling/filtering capacitors 100nF X7R [1][2] and 4.7µF X7R [1]	Powers the core, memories, peripherals, the PLL, the DFLL, and the 4 MHz integrated RC oscillator (RCFAST) and the 115kHz integrated RC oscillator (RCSYS). Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	BUCK/LDOn	100kΩ (maximum) pull up resistor to VDDIN.	Selects the regulator mode on power on reset. The pin is available for the application after reset.

Notes:
1. These values are given only as a typical example.
2. Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Only on LCD capable devices (ATSAM4LCx).

1.3 Linear Mode

Figure 1-3. Linear Mode Example Schematic.

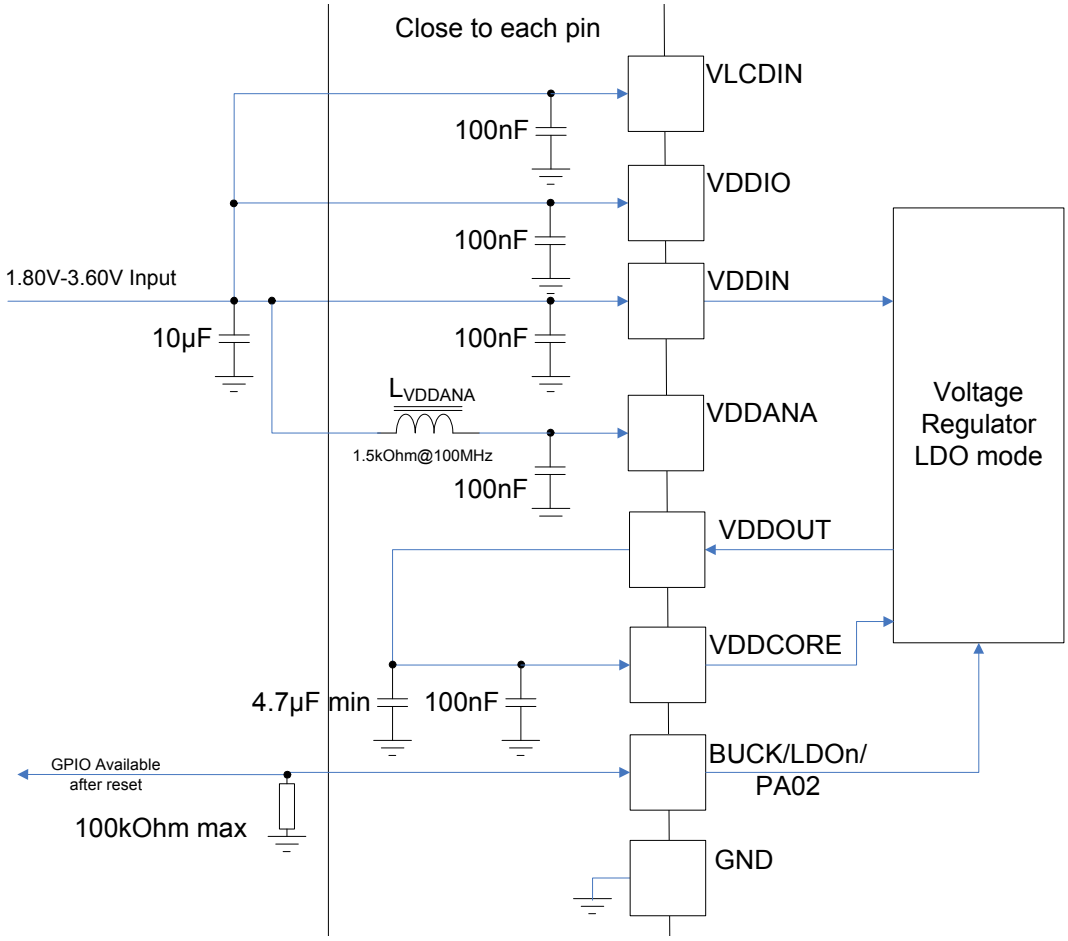


Table 1-3. Linear Mode Power Supply Checklist.

☑	Signal name	Recommended pin connection	Description
	Supply input	VDDIN = VDDIO = VDDANA = VLCDIN (3)	The supply pins must be at the same potential.
	VLCDIN (3)	1.80V to 3.60V 100nF X7R (1)(2) Decoupling/filtering capacitor	Powers the LCD voltage pump. Decoupling/filtering capacitors must be added to minimize voltage ripple.
	VDDIO	1.80V to 3.60V 100nF X7R (1)(2) Decoupling/filtering capacitor	Powers I/O lines, the general purpose oscillator (OSC), the 80MHz integrated RC oscillator (RC80M). Decoupling/filtering capacitors must be added to minimize voltage ripple.
	VDDANA	1.80V to 3.60V 100nF X7R (1)(2) Decoupling/filtering capacitor	Powers the ADC, the DAC, the Analog Comparators, the 32kHz oscillator (OSC32K), the 32kHz integrated RC oscillator (RC32K) and the Brown-out detectors (BOD18 and BOD33). Decoupling/filtering capacitors must be added to minimize voltage ripple.
	VDDIN	1.80V to 3.60V Decoupling/filtering capacitors 100nF X7R (1)(2) and 10µF(1)	Powers I/O lines and internal voltage regulator. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOUT	Connect VDDOUT to VDDCORE	Output of the on-chip voltage regulator.
	VDDCORE	Decoupling/filtering capacitors 100nF X7R (1)(2) and 4.7µF X7R (1)	Powers the core, memories, peripherals, the PLL, the DFLL, and the 4 MHz integrated RC oscillator (RCFAST) and the 115kHz integrated RC oscillator (RCSYS). Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	BUCK/LDOn	100kΩ (maximum) pull down resistor to GND.	Selects the regulator mode on power on reset. The pin is available for the application after reset.

Notes:
1. These values are given only as a typical example.
2. Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Only on LCD capable devices (ATSAM4LCx).

1.4 GPIO Cluster Supply on LCD Capable Devices

If, for some reason, the LCD controller of an LCD capable device is not used at all, refer to 7.2 When not using the LCD.

2. Analog Schematics

The ATSAM4L features a differential ADC, a DAC and an analog comparator.

2.1 ADC Reference Voltage Schematic

Figure 2-1. ADC Reference Voltage Example Schematic.

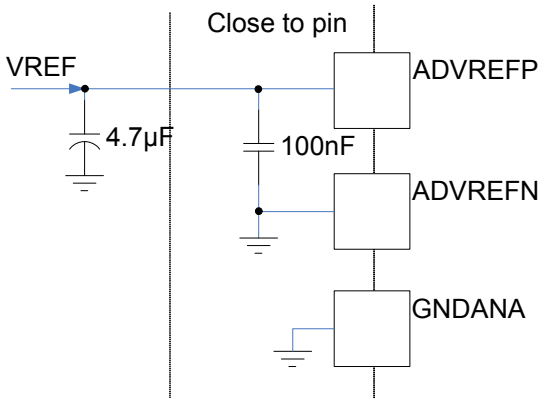


Table 2-1. Linear Mode Power Supply Checklist.

☑	Signal name	Recommended pin connection	Description
	ADVREFP	1.0V to VDDANA 100 nF X7R (1)(2) Decoupling/filtering capacitor	ADVREFP is a pure analog input. The 100nF capacitor. The 4.7µF capacitor is recommended in applications where low frequency noise is expected.
	ADVREFN	Connect to GNDANA	
	GNDANA	Connect to same voltage level as GND	This pin is not internally connected to other GND pins.

Notes: 1. These values are given only as a typical example.
2. Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

2.2 ADC Analog Inputs

Table 2-2. ADC Analog Input Connection Checklist.

☑	Signal name	Recommended pin connection	Description
	ADx	Source impedance is low enough to avoid drops of voltage when the ADC samples the input.	Refer to “Inputs and Sample and Hold Acquisition Times” in Electrical characteristics section of the datasheet.
	ADx	Measured voltage is between 10% and 90% of reference voltage.	Operation outside this range leads to lower accuracy. Refer to Electrical characteristics section of the datasheet for details.
	ADx	Selection of the ADC inputs when using differential mode.	Differential mode: - In the MUXNEG table, the input signal is selected among the AD[7..0] inputs. - In the MUXPOS table, the input signal is selected among the AD[14..0] inputs.

3. Reset Circuit

Figure 3-1. Reset Circuit Example Schematic.

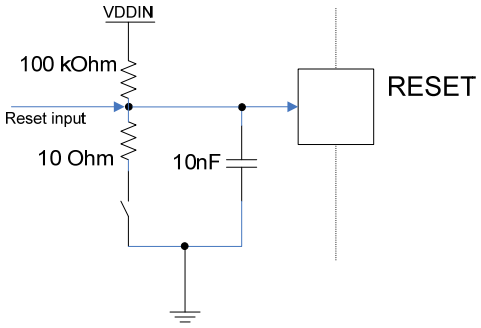


Table 3-1. Reset Circuit Checklist.

☑	Signal name	Recommended pin connection	Description
	RESET		The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIN. As the product integrates a power-on reset detector, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

4. Clocks and Crystal Oscillators

4.1 External Clock Source

Figure 4-1. External Clock Source Schematic.

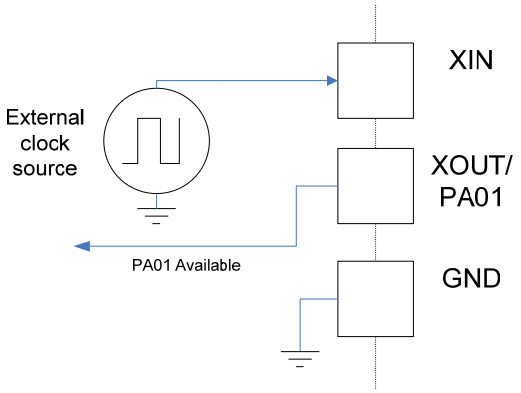


Table 4-1. External Clock Source Checklist.

☑	Signal name	Recommended pin connection	Description
	XIN	Connected to clock output from external clock source.	Up to VDDIO volt square wave signal. Input frequency up to 50MHz. Refer to the datasheet for duty cycle requirements.
	XOUT	Can be left unconnected or used as a standard pin.	

4.2 Crystal Oscillator

Figure 4-2. Crystal Oscillator Example Schematic.

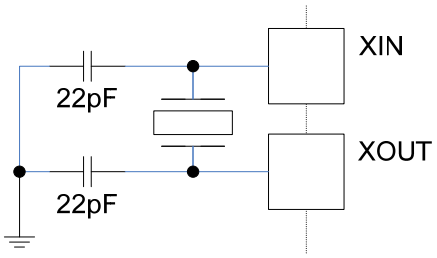


Table 4-2. Crystal Oscillator Checklist.

☑	Signal name	Recommended pin connection	Description
	XIN	Biasing capacitor 22pF (1)	External crystal between 0.6MHz and 30MHz, powered by VDDIO. The crystal and capacitors should be located close to the device to minimize noise emission and improve immunity.
	XOUT	Biasing capacitor 22pF (1)	Powered by VDDIO.

Notes: 1. These values are given only as a typical example and depend on the crystal parameters, PCB tracks capacitance and MCU package. To determine the suitable value for the application, refer to the “Electrical characteristics” section of the datasheet.

4.3 Low Frequency External Clock Source

Figure 4-3. Low Frequency External Clock Source Schematic.

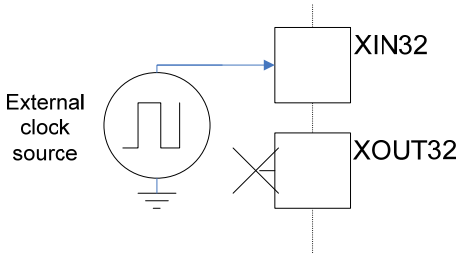


Table 4-3. Low Frequency External Clock Source Checklist.

☑	Signal name	Recommended pin connection	Description
	XIN32	Connected to clock output from external clock source	Up to VDDANA volt square wave signal. Input frequency up to 6MHz.
	XOUT32	Must be left unconnected	

4.4 32kHz Crystal Oscillator

Figure 4-4. 32kHz Crystal Oscillator Example Schematic.

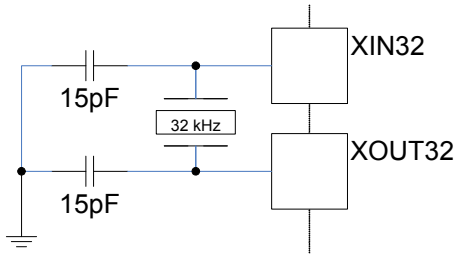


Table 4-4. 32kHz Crystal Oscillator Checklist.

☑	Signal name	Recommended pin connection	Description
	XIN32	Biasing capacitor 15pF (1)	32.768kHz external crystal powered by VDDANA. The crystal and capacitors should be located close to the device to minimize noise emission and improve immunity.
	XOUT32	Biasing capacitor 15pF (1)	Powered by VDDANA.

Notes: 1. These values are given only as a typical example and depend on the crystal parameters, PCB tracks capacitance and MCU package. To determine the suitable value for the application, refer to the “Electrical characteristics” section of the datasheet.

5. Capacitive Touch (CATB) Module

The CATB can operate in single-ended or differential mode.

Figure 5-1. QTouch Single Ended Schematic.

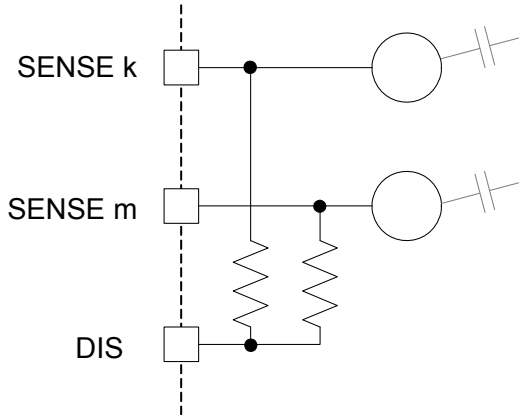


Table 5-1. QTouch Single Ended Checklist.

☑	Signal name	Recommended pin connection	Description
	SENSEx	Low capacitance track to sensor Connect a discharge resistor to DIS pin of the device	Capacitive touch sensor connection.
	DIS	Resistor connected to each sensor line	Common discharge pin.

Figure 5-2. QTouch Differential Schematic.

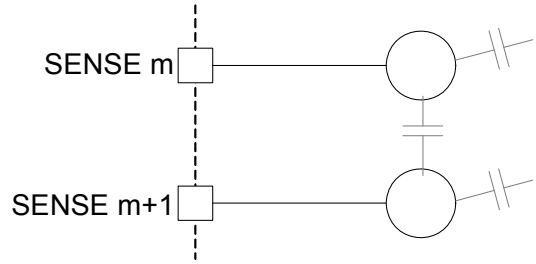


Table 5-2. QTouch Differential Mode Checklist.

☑	Signal name	Recommended pin connection	Description
	SENSE m	Connect directly to the first part of the differential capacitive touch sensor	Capacitive touch sensor connection.
	SENSE m+1	Connect directly to the second part of the differential capacitive touch sensor	Capacitive touch sensor connection.

6. USB Connection

To be able to use the USB I/O, the VDDIN power supply must be 3.3V nominal.

6.1 Not Used

If the USB interface is not used, D+ and D- are available for application and behave as standard GPIOs but their electrical characteristics are different than the standard I/Os. Refer to the electrical characteristics section of the datasheet.

6.2 Device Mode, Powered from Bus Connection

Figure 6-1. USB in Device Mode, Bus Powered Connection Example Schematic.

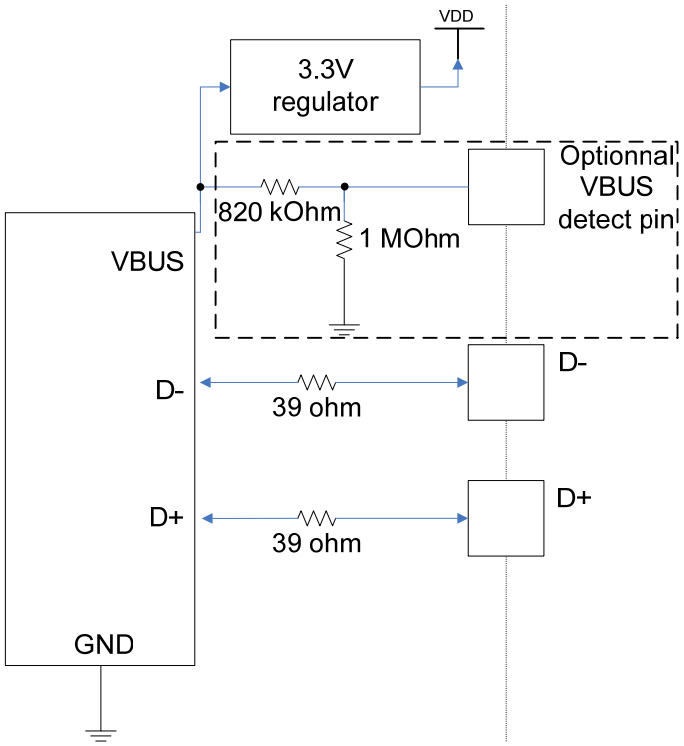


Figure 6-2. USB in Device Mode, Self Powered Connection Example Schematic.

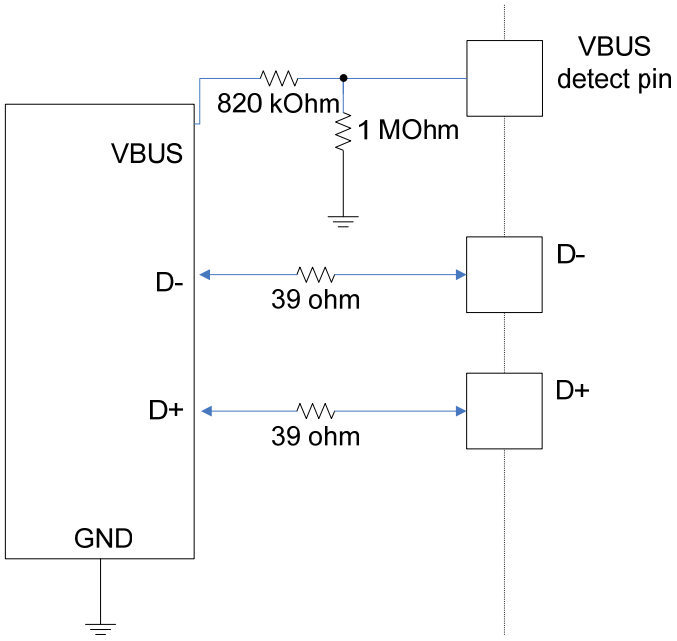


Table 6-1. USB Connection Checklist.

☑	Item	Recommended pin connection	Description
	VBUS	Voltage divider to convert 5V VBUS to 3.3V input compatible level	Depending on the application, detecting VBUS level may be required to perform specific actions.
	D+ and D-	USB signals impedance	PCB traces for USB signals must have specific impedance: - 45Ω single ended - 90Ω differential Refer to the USB specification for more details
	D+ and D-	39Ω (1) series resistor placed as close as possible to the device pin.	USB signal lines.
	Crystal	XTAL or external digital clock input: Typical frequencies (1): 6MHz ±2500ppm 7.3728MHz ±900ppm 8MHz ±2500ppm 12MHz ±2500ppm 14.7456MHz ±900ppm 16MHz ±2500ppm 24MHz ±2500ppm	USB module requires a specific clock input. Refer to the device datasheet for details.

Notes: 1. These values are given only as a typical example.

7. Segment LCD Schematics

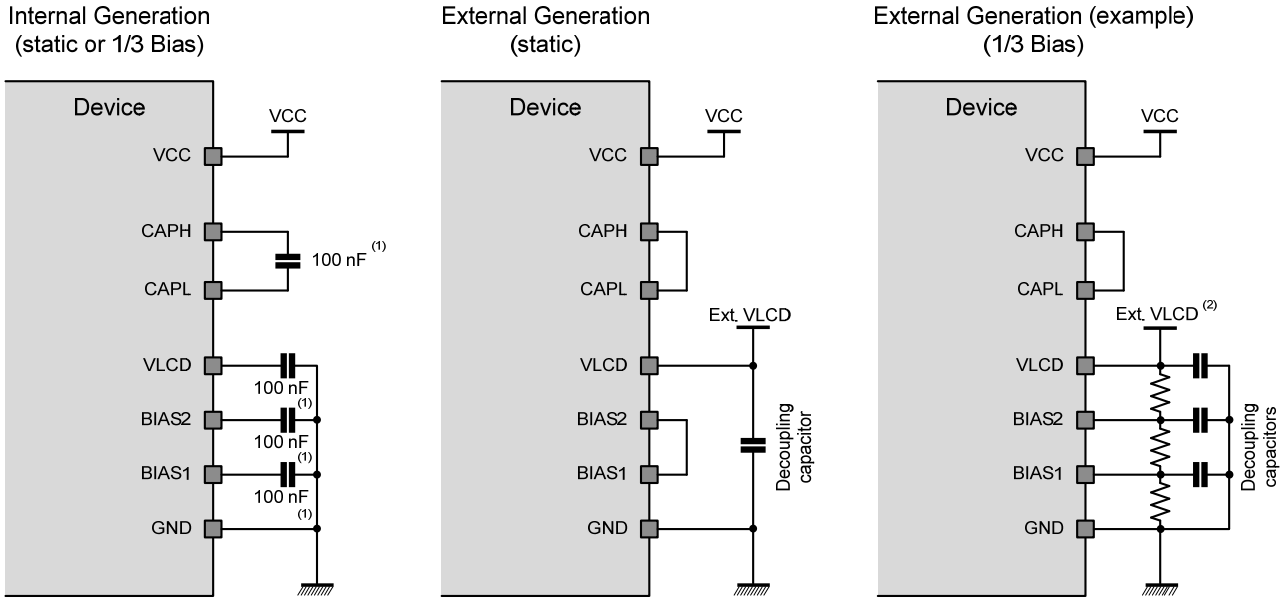
ATSAM4L features a 4x40 segment LCD controller with character mapping.

LCD controller requires some external components for operation.

Character mapping and autonomous animation requires specific allocation of the LCD screen segment and common terminals. Refer to the LCD controller section of the datasheet.

7.1 LCD Voltage Pump Schematic

Figure 7-1. LCD Bias Voltage Generation Schematic.



(1) Values are given for design guidance only.
(2) Bias generation can be provided by other voltage source than a division resistor

Table 7-1. Internal Bias Voltage Generation Checklist.

☑	Signal name	Recommended pin connection	Description
	CAPH and CAPL	Connect a 100nF (1)(2) capacitor from CAPH to CAPL	Charge pump capacitor.
	VLCD	Connect a 100nF (1)(2) capacitor from VLCD to GND	LCD controller decoupling.
	BIAS2	Connect a 100nF (1)(2) capacitor from BIAS2 to GND	LCD bias voltage filtering.
	BIAS1	Connect a 100nF (1)(2) capacitor from BIAS1 to GND	LCD bias voltage filtering.

Notes: 1. These values are given only as a typical example.
2. Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

7.2 When not Using the LCD

If, for some reason, the LCD controller is not used at all, the LCD power pins should be connected this way:

Table 7-2. Checklist When Not Using the LCD Controller.

☑	Signal name	Recommended pin connection	Description
	CAPH and CAPL	Connect CAPH & CAPL together but not to GND	Avoids current consumption of undriven input
	VLCD	Connect to VDDIO	LCDA Cluster GPIO pins power supply (1)
	BIAS1 and BIAS2	Connect BIAS1 & BIAS2 together but not to GND	Avoids current consumption of undriven input

Notes: 1. Refer to the “LCD power modes” section of the device datasheet.

8. Debug and Programming

There are two standard debug interfaces connectors for ARM® devices:

- 20-pin legacy connector:
  - Supported by most available ARM debug interfaces
  - Robust
- 10-pin Cortex™ debug connector
  - New standard
  - Reduced board area

8.1 JTAG Port Interface

Figure 8-1. JTAG 20-pins Debug Port Schematic.

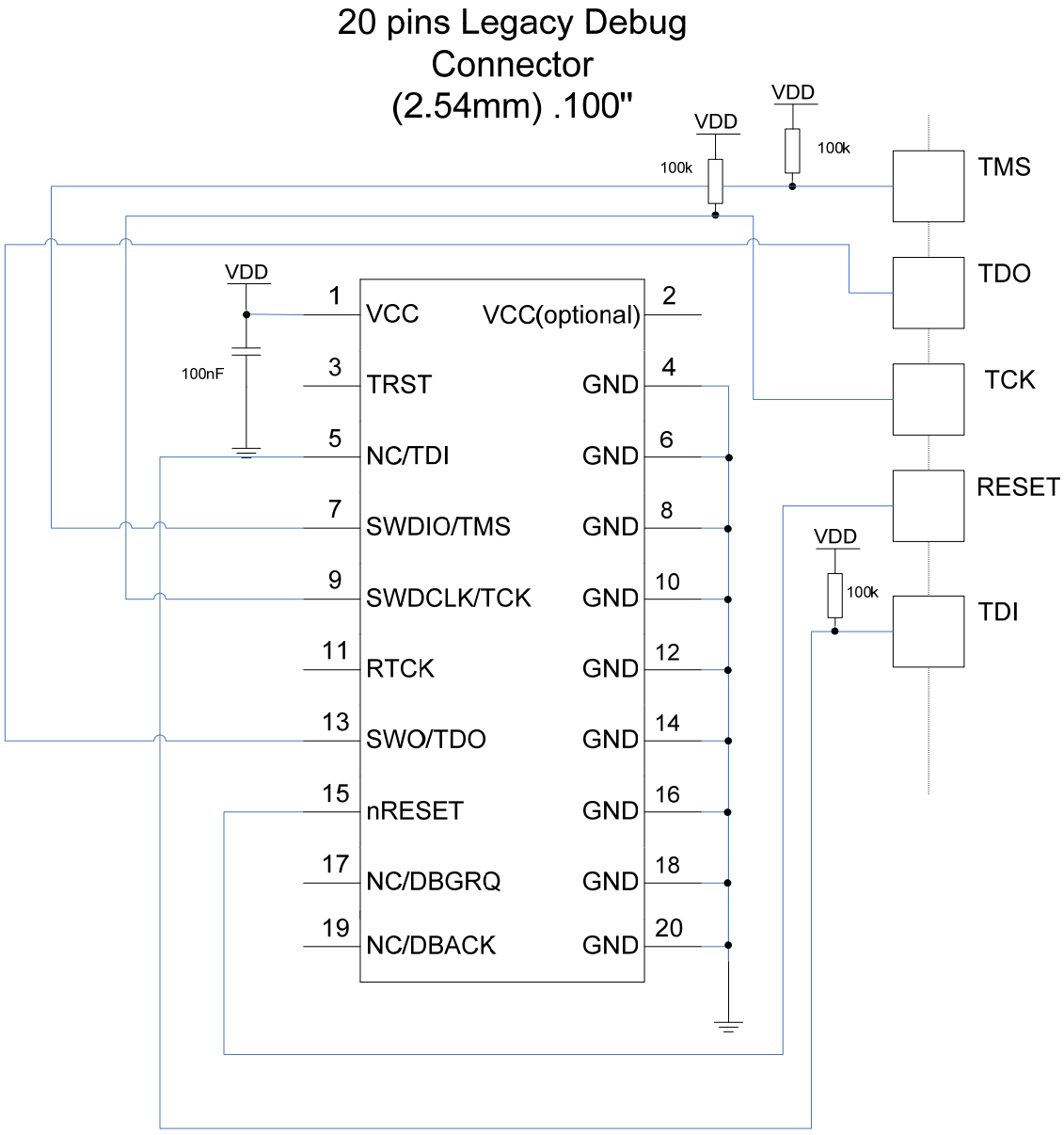


Figure 8-2. JTAG 10-pins Debug Port Schematic.

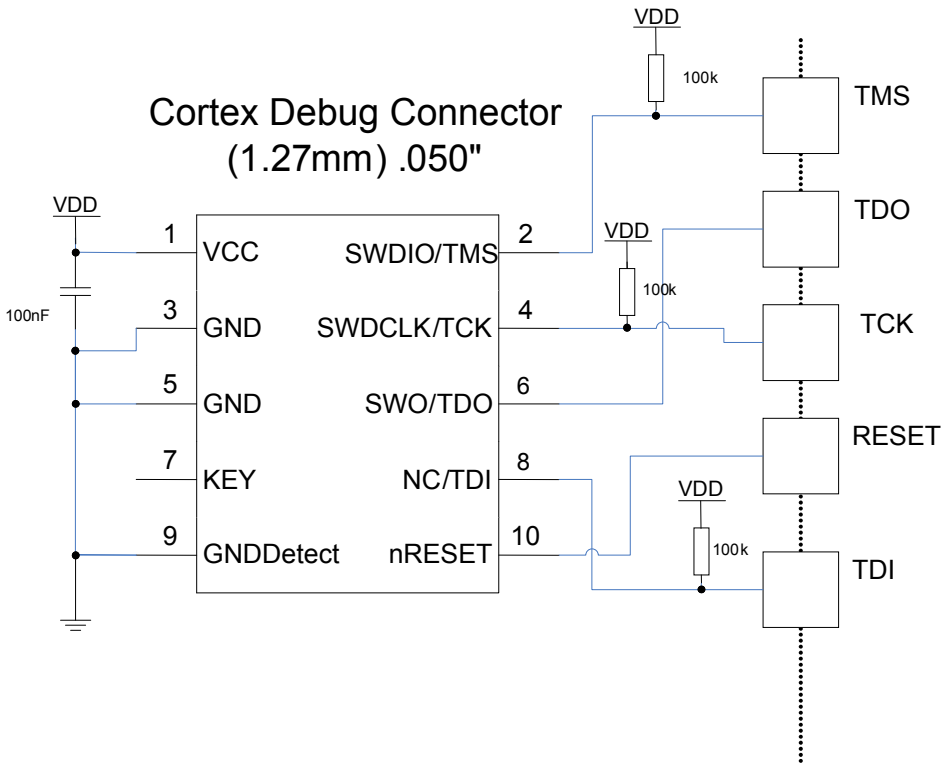


Table 8-1. JTAG Debug Port Checklist.

☑	Signal name	Recommended pin connection	Description
	TMS/PA03 (1)	Connect to debugger connector 100k Pull-up to VDDIN	
	TDO/PA23 (1)	Connect to debugger connector	
	TDI/PA24 (1)	Connect to debugger connector 100k Pull-up to VDDIN	
	TCK	Connect to debugger connector 100k Pull-up to VDDIN	
	RESET	Connect to debugger connector	

Notes: 1. These pins may be used by the application but will be unavailable when debugging: If the JTAG is enabled, the JTAG will take control over a number of pins, irrespectively of the I/O Controller configuration.

8.2 SWD Port Interface

Serial wire debug use less pins than JTAG debug interface.

Figure 8-3. SWD 20-pins Legacy Debug Port Schematic.

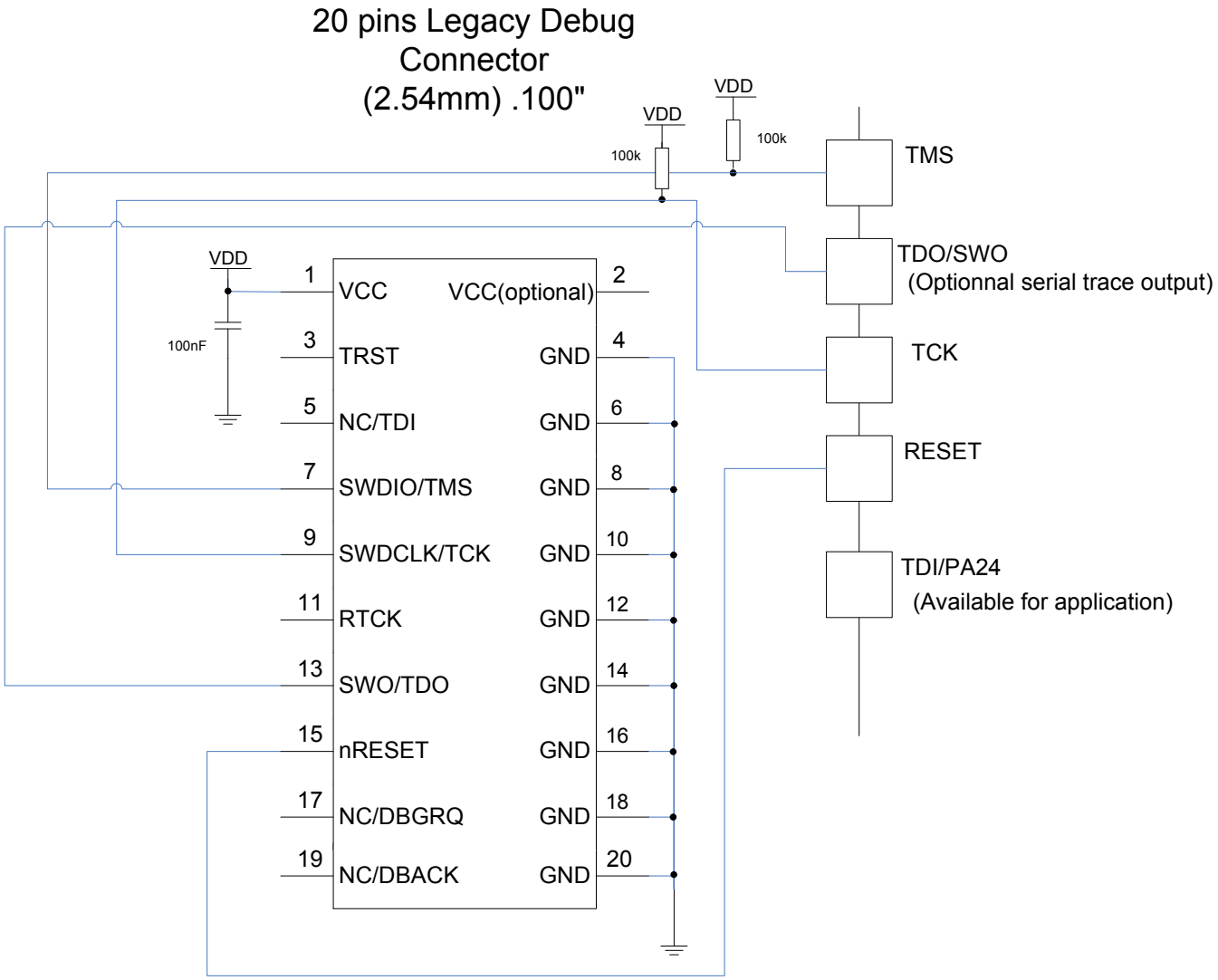


Figure 8-4. SWD 10-pins Debug Port Schematic.

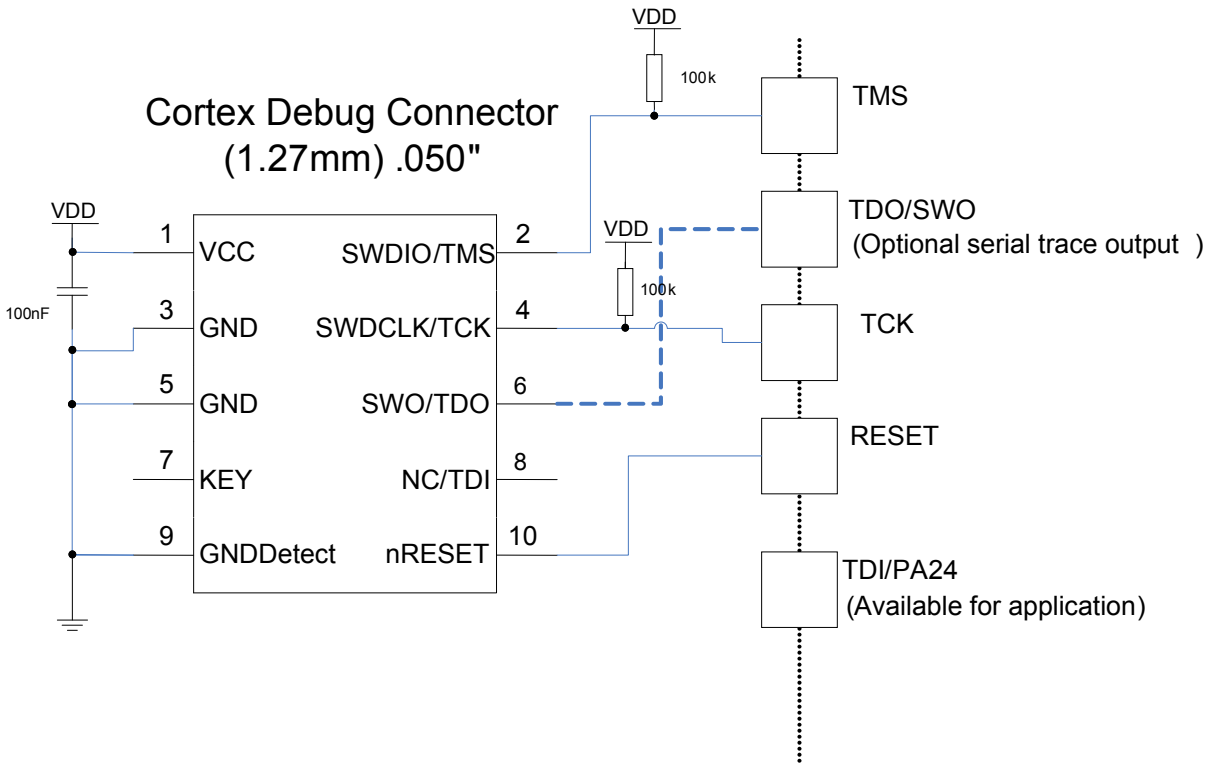


Table 8-2. SWD Debug Port Checklist.

☑	Signal name	Recommended pin connection	Description
	TMS/PA03 (1)	Connect to debugger connector 100k Pull-up to VDDIN	SWDIO
	TDO/PA23 (1)	Optionally connect to debugger connector if serial trace is needed	SWO If serial trace is enabled, trace will take control of this pin irrespectively of the I/O Controller configuration.
	TDI/PA24 (1)	No connection needed Available for application	
	TCK	Connect to debugger connector 100k Pull-up to VDDIN	SWDCLK
	RESET	Connect to debugger connector	

Notes: 1. These pins may be used by the application but will be unavailable when debugging: If the SWD is enabled, the SWD will take control over a number of pins, irrespectively of the I/O Controller configuration.

9. Miscellaneous Topics

9.1 SAM-BA Bootloader Hardware Requirements

The SAM-BA® Boot Assistant supports serial communication via the UART or USB device port:

Table 9-1. UART Mode Requirements Checklist.

☑	Signal name	Recommended pin connection	Description
	PA05	Connect to host	USART0 RXD pin.
	PA07	Connect to host	USART0 TXD pin.
	Hardware Bootloader Entry (Any GPIO)	Connect to host	Optional pin to force bootloader entry on reset. If enabled, the bootloader will check the GPIO on reset to determine if the bootloader monitor shall start. This feature allows the end user to reprogram the device even if the application is corrupted or unable to start the SAM-BA monitor. This GPIO number and its active level are defined in the flash user page. The SAM-BA application can be used to program it. Note: The bootloader won't pull up or pull down the pin, the level has to set externally.

Notes: 1. These values are given only as a typical example.

Table 9-2. USB Mode Requirements Checklist.

☑	Signal name	Recommended pin connection	Description
	D+	Connect to host	USB D+ pin
	D-	Connect to host	USB D- pin
	Hardware Bootloader Entry (Any GPIO)	Connect to host	Optional pin to force bootloader entry on reset. If enabled, the bootloader will check the GPIO on reset to determine if the bootloader monitor shall start. This feature allows the end user to reprogram the device even if the application is corrupted or unable to start the SAM-BA monitor. This GPIO number and its active level are defined in the flash user page. The SAM-BA application can be used to program it. Note: The bootloader won't pull up or pull down the pin, the level has to set externally.
	XIN / XOUT	XTAL or external digital clock input : Supported frequencies: 6MHz ±2500ppm 7.3728MHz ±900ppm 8MHz ±2500ppm 12MHz ±2500ppm 14.7456 MHz ±900ppm 16MHz ±2500ppm 24MHz ±2500ppm	Clock input for PLL used for USB clock source.

9.2 Low Power Design

In order to minimize power consumption the following checklist should be followed:

Table 9-3. Low Power Design Checklist.

☑	Item	Recommendations
	Any I/O	Avoid mid-level voltages on digital inputs (analog inputs excluded). The voltage placed on the input shall be as close as possible to VDD or GND. Beware of any external component connected to MCU but powered by another supply domain (ex: 5V sensor connected to SAM4L using 3.3V VDDIN).
	Unconnected pins	To reduce power consumption, unused I/O pins should be made stable by either: - Setting I/O as input with internal pull-up enabled. - Setting I/O as output and driven at '0' with internal pull-up disabled.
	Oscillators	Avoid driving high capacitance lines at high frequencies by ensuring minimum track length.
	Regulator Mode	The regulator has an impact on power consumption. Refer to 1.1 Choosing the right regulator mode for the application to choose the suitable regulator mode.
	Communications	Avoid software emulation for communications, hardware driven use less CPU and complete communications quicker allowing the CPU to go back to sleep sooner. Some hardware peripherals also allow the use of SleepWalking to perform actions without CPU intervention.

10. Suggested Reading

10.1 Device Datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. It also contains the electrical specifications and expected characteristics of the device.

The datasheet is available on http://www.atmel.com/ in the Datasheets section of the product page.

10.2 Evaluation Kit User Guide

The SAM4L-EK user guide contains schematics that can be used as a starting point when designing with the SAM4L devices. This user guide is available on http://www.atmel.com/ in the documents section of the SAM4L-EK page.

The SAM4L Xplained Pro user guide contains the details about pin assignment of the extension interfaces on the board and other hardware information. This user guide is available on http://www.atmel.com/ in the documents section of the SAM4L Xplained Pro page.

10.3 USB Specification

The Universal Serial Bus specification is available from http://www.usb.org.

10.4 ARM Documentation on Cortex-M4 core

- Cortex-M4 Devices Generic User Guide for revision r0p1
- Cortex-M4 Technical Reference Manual for revision r0p1

These documents are available at http://www.arm.com/ in the info center section.

11. Revision history

Doc. Rev.	Date	Comments
42025D	11/2013	• Table 7-2 updated. Checklist when not using the LCD controller • Typos fixed • Tables and headings updated according to template
42025C	06/2013	• Renamed from “AVR4035: SAM4L Schematic Checklist” to “AT01777: SAM4L Schematic Checklist” • Changed section 1 and section 7, on LCD clusters supply • Added SAM4L Xplained Pro information
42025B	10/2012	• Changed USART2 to USART0 in SAM-BA Bootloader hardware requirements
42025A	09/2012	• Initial document release

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