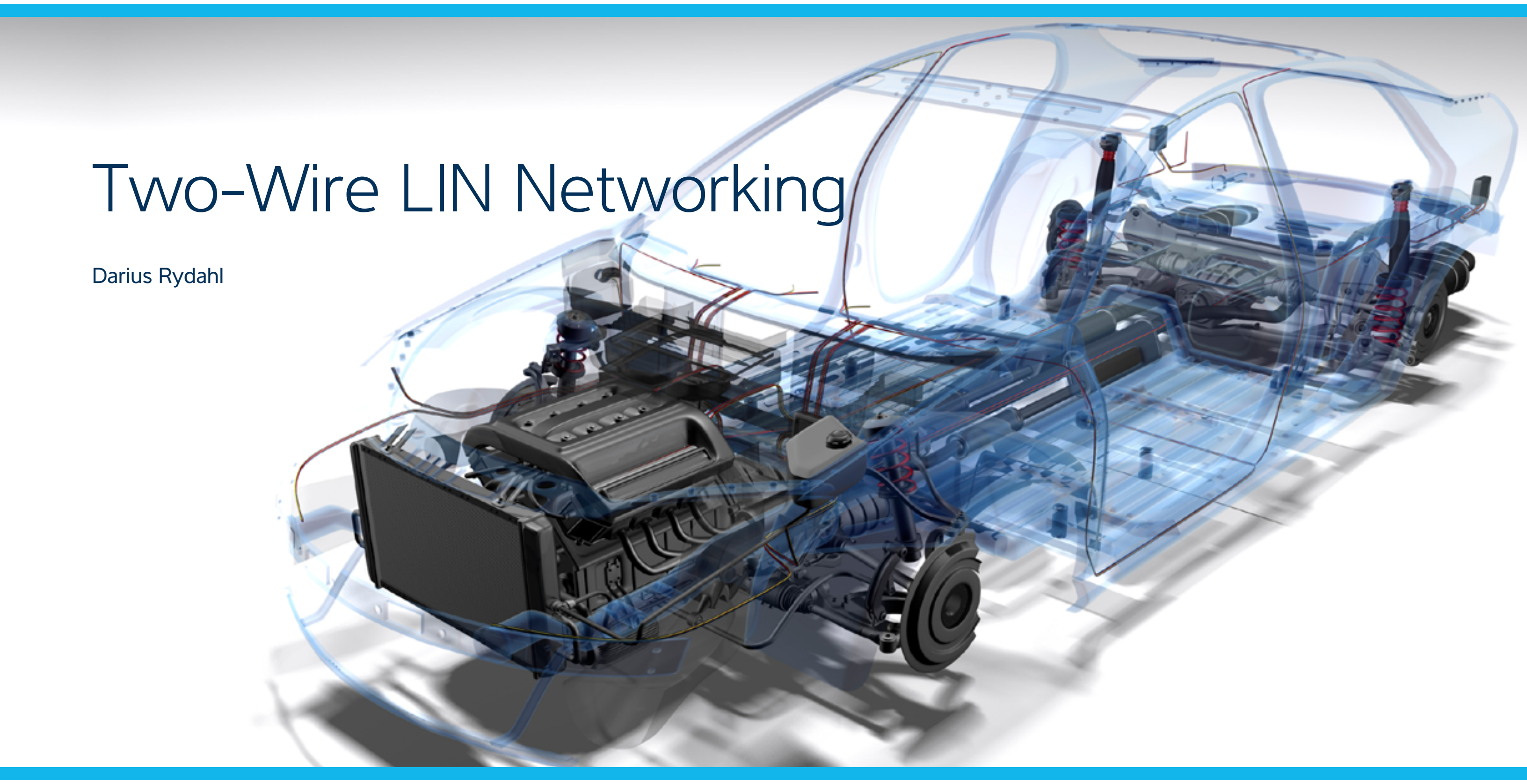
Two-Wire LIN Networking

Darius Rydahl



LIN Bus—Introduction

Today's modern automobiles contain hundreds of sensors used to measure and report on parameters such as temperature and pressure. In most instances, these sensors are remotely located within a vehicle far away from the host microcontroller responsible for monitoring and processing the sensor data. These sensors typically do not directly connect to a network (such as CAN or LIN) due to the vehicle wiring overhead associated with connecting to the network. One such method for overcoming this wiring limitation is to convert the standard three-wire LIN network to a two-wire implementation where the LIN slave nodes harvest power directly from the LIN bus master communication wire, thereby eliminating the need for an individual battery supply wire to each slave node.

A standard LIN bus consists of a master node and up to 15 slave nodes connected to a single network. The physical LIN network is a three-wire configuration consisting of power (vehicle battery), ground and the LIN bus communication line. A pull-up resistor, R_{LIN}, typically 1kΩ, is required on the master's LIN bus line. Under normal LIN bus operation, this pull-up resistor provides a voltage bias on the LIN bus line to the slave nodes on the LIN network. It does not power the LIN slave nodes. Slave node power is derived from the battery input to the device, as shown in Figure 1.

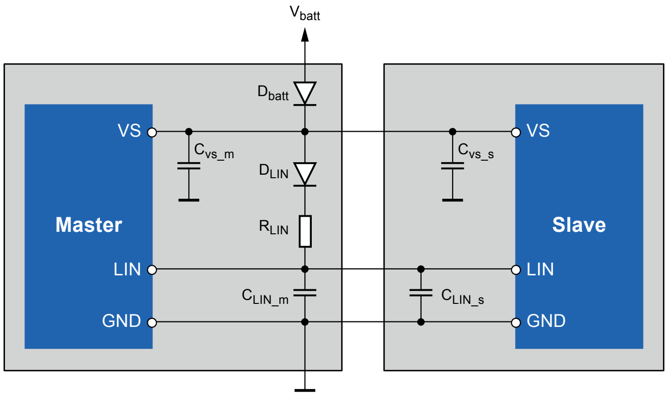


Figure 1. Standard Three-wire LIN Configuration

It is possible to use a non-standard LIN network architecture that simplifies to two wires. This approach relies on the harvesting of power by a connected slave node directly from the LIN bus line, thus eliminating the need for an independent slave node battery supply line. This concept is shown in Figure 2.

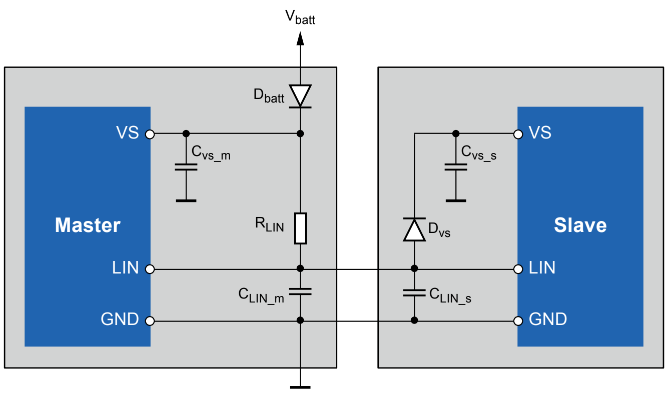


Figure 2. Proposed Two-wire LIN Configuration

With the battery supply line removed, all that is required to power the slave node is a blocking diode, V_{DS} and buffer capacitor, C_{VS_S}, large enough to sustain the slave node supply voltage during the transmission of LIN data packets, which periodically pulls the LIN signal to ground. This article outlines the implementation of this two-wire approach and identifies the inherent system-level tradeoffs that must be considered to fully realize a functional two-wire LIN network.

Key Parameters

The key to successfully implementing a two-wire LIN network centers around the power requirements of the connected slave node. The slave node must be supplied with sufficient power to maintain communication at the minimum system operating voltage: typically 9V. If this condition cannot be met, it is unlikely that the two-wire LIN implementation will be a viable solution.

Key parameters that affect the slave node's performance in the two-wire implementation are:

1. LIN bus power supply
2. Slave node current consumption
3. Slave node buffer capacitance
4. LIN bus data protocol

LIN Bus Power Supply

The two-wire LIN network is limited by the power supplied from the master to the slave node over the LIN bus line. The supply to the LIN slave in this configuration will be dictated by the LIN bus master pull-up resistor, R_{LIN} (Figure 2). The slave node has a fixed minimum input voltage operating requirement of 5.5V (reference: the Atmel® ATA6624 LIN transceiver). In order to meet this minimum operating voltage requirement, the load current drawn by the slave node must not cause the voltage drop across the LIN master pull-up resistor to increase to the point at which the input voltage to the slave node drops below 5.5V. This is the minimum operating voltage threshold for slave node voltage regulator operation. Figure 3 shows the maximum load current available to the slave node at the minimum supply voltage of 5.5V at different LIN master pull-up resistances.

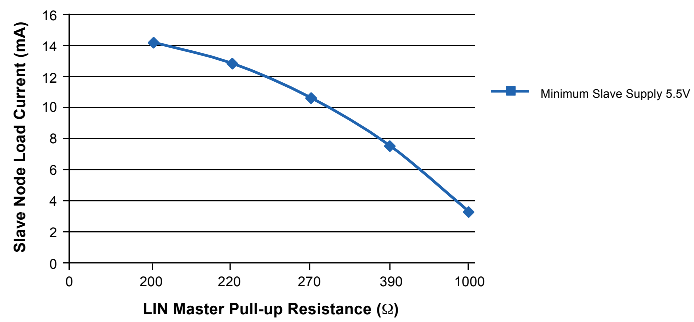


Figure 3. LIN Master Pull-up Resistance versus Maximum Slave Node Load Current at 5.5V Supply

The 1kΩ master pull-up resistor specified in the LIN standard specification cannot be used in the two-wire configuration. The resistor is too large and, as a result, is unable to properly source the slave node load (slave node current will be discussed in further detail in the following chapter). The pull-up resistor must be reduced in size to the smallest value possible without exceeding the current limitation specification of the LIN driver. In the case of the typical Atmel LIN transceiver, the ATA6624, the recommended minimum pull-up resistor value is 220Ω. Resistances lower than this could result in excessive current flow through the LIN transceiver when the LIN bus is asserted low.

Slave Node Current Consumption

There are several factors which contribute to the overall current consumption of the LIN slave node. They include:

1. System clock frequency
2. Power management
    a. Sleep mode
    b. LIN scheduling

System Clock Frequency

The system clock frequency of the microcontroller has the most significant effect on the slave node current consumption. The slave node current consumption is directly proportional to the clock frequency. This effect is shown in Figure 4.

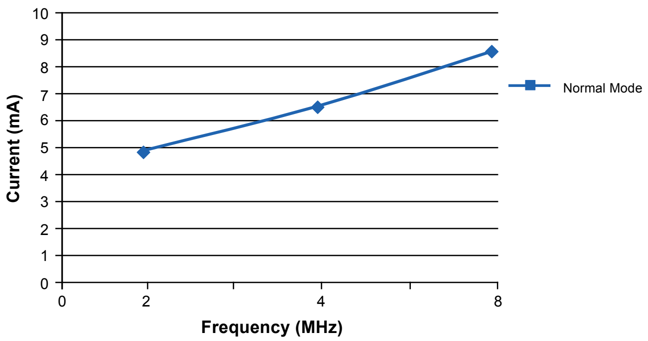


Figure 4. Typical Normal Mode ATtiny167 Current vs. System Clock Frequency

Clearly, one should attempt to use the lowest clock frequency that enables the application to meet functional design requirements.

Power Management—Sleep Mode

The overall current consumption of the two-wire LIN slave node can be further reduced by duty-cycling between low and high current operating modes, e.g. power-down/normal mode for the microcontroller and silent/normal mode for the LIN transceiver in between LIN data frames. Figure 5 demonstrates this point.

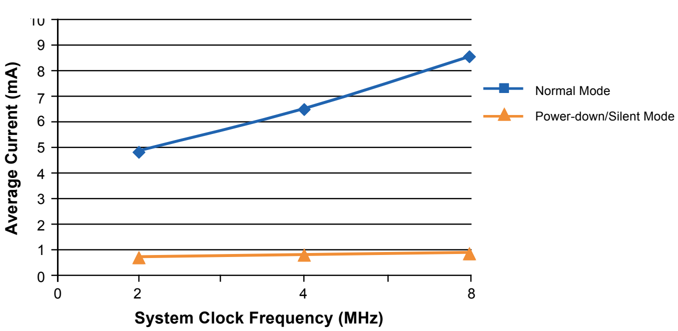


Figure 5. Typical Current vs. System Clock Frequency
(Note: 2MHz System Clock, 8-bit Response, No Load, 1s LIN Schedule Table Period for the Power-down/Silent Mode Measurement Case)

Atmel AVR® microcontrollers provide various sleep modes, allowing the user to tailor power consumption to the application's requirements. In the case of the two-wire LIN application, the power-down mode provides the greatest current reduction when used in conjunction with the silent mode of the LIN transceiver. In this mode, all generated clocks are shut down, allowing operation of asynchronous modules only (external interrupts, USI and watchdog). To wake up the microcontroller from power-down, the LIN master must first generate a LIN wake-up request followed by a LIN frame header. This process is shown in Figure 6.

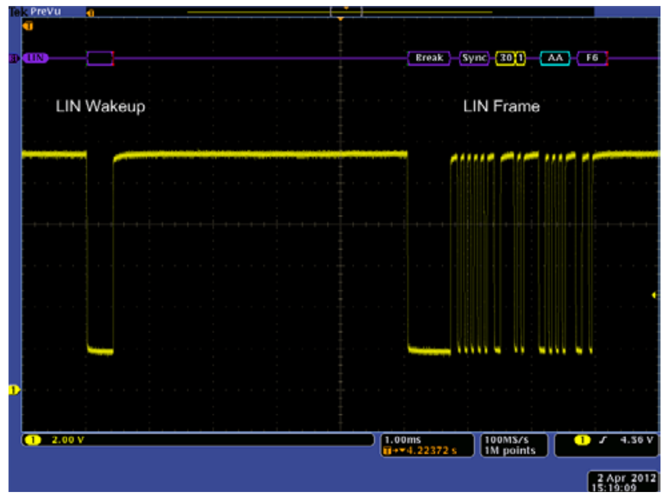


Figure 6. LIN Wake-up and LIN Frame

Upon wake-up, the microcontroller enters the normal mode and switches the EN pin (LIN transceiver enable) to HIGH at the start of each newly received LIN wake-up/frame packet. During LIN data frames, the slave node microcontroller remains in normal mode and is able to provide an immediate data response upon receipt of the sync-break and message ID. At the end of the LIN data frame, the slave node returns to the power-down mode.

Operating the device in this manner will significantly reduce the average current consumption of the slave node.

Power Management—LIN Scheduling

The time between LIN frames, also known as the schedule table period, and the duration of the LIN frame define the power duty cycle of the slave node. This duty cycle affects the average current consumption of the two-wire LIN slave node. A typical LIN network operating at 19.2kbaud with a single frame, 8-bit message response has an average frame length of 2.95ms each. Figure 7 shows the effect of varying the schedule table period while connected to a slave node that is power duty cycling between power-down/silent and normal modes under these conditions.

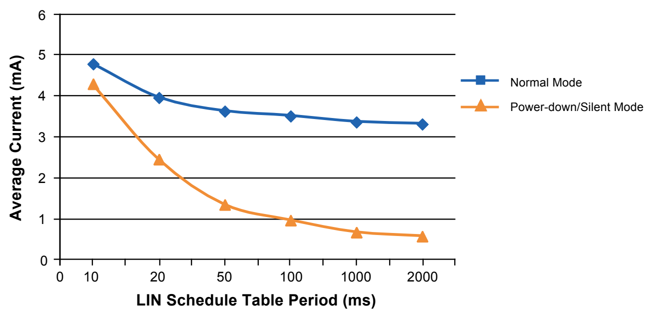


Figure 7. Effect of LIN Schedule Periods vs. Current Consumption (2MHz System Clock)

Clearly, lengthening the schedule table period reduces the slave node's average current consumption. However, this benefit is bounded by the power-down/silent mode current and offers minimal benefit for schedule periods greater than one second.

Slave Node Buffer Capacitance

While an important piece of the two-wire LIN equation, sizing of the slave node buffer capacitor, C_{VS_S}, is not a dominant factor. The capacitor must provide sufficient charge reserve to power the slave node during a LIN frame data packet (LIN signal is periodically asserted low) and also receive a full charge between LIN frame data transmissions (the LIN signal is pulled up to system supply voltage). In practice, bench tests indicate that a buffer capacitor of 47µF to 100µF is sufficient to maintain power to the slave node for a network operating at a data rate of 19.2kbaud with a 100ms delay (or greater) between LIN data frames and a 9V minimum operating battery voltage.

LIN Bus Data Protocol

The format of the LIN bus data protocol will affect the charge/discharge rate of the slave node supply line buffer capacitor. Three factors affect the data format:

1. Rate of data transfer
2. Quantity of data transferred
3. LIN data schedule table period

The LIN bus data rate should be kept high, i.e., a maximum baud rate of 19.2kHz or higher to maximize the speed at which the data can be transferred. The quantity of data (number of bits) should be kept as low as possible in order to minimize the duration of the dominant state (logic level low) on the LIN bus line. And finally, the LIN schedule table period should be long enough in duration to allow the LIN bus powered slave node time to fully recharge the buffer capacitor, C_{VS_S}, between LIN message frames.

Note: Most Atmel LIN transceivers are capable of baud rates in excess of the LIN specification (please refer to the specific device data sheet for more information).

Multi-slave Evaluation Network

The multi-slave two-wire LIN network used for test and characterization purposes is shown in Figure 8. The two-wire LIN network total node count is limited only by the LIN master pull-up resistor's ability to source the required current to the attached slave nodes to maintain normal operation (slave node VS greater than 5.5V).

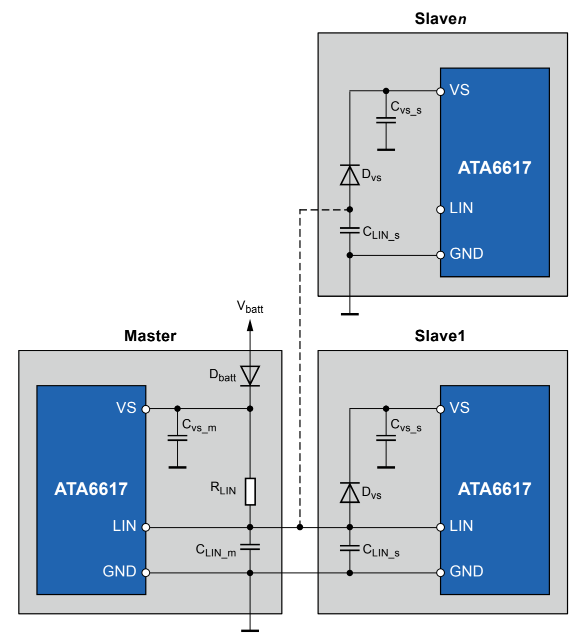


Figure 8. Two-wire LIN Multi-slave Network

Each node has been realized using the Atmel ATA6617-EK* evaluation board and configured using the settings shown in Table 1. This configuration provides one possible operating scenario and, as such, will most likely need to be modified to accommodate the end user's application.

**Note: the ATA6617-EK is an Atmel LIN system in package (SiP) evaluation board which consists of an Atmel AVR microcontroller, the ATtiny167, and the Atmel LIN system basis chip (SBC), the ATA6624. For more detailed information, please refer to the product data sheets for the respective devices.*

The network utilizes the standard LIN protocol and does not deviate from the LIN2.x standard in any manner. The schedule table has been optimized for the two-wire LIN application where a LIN wake-up frame is followed by a single slave node frame, Figure 9.

Atmel

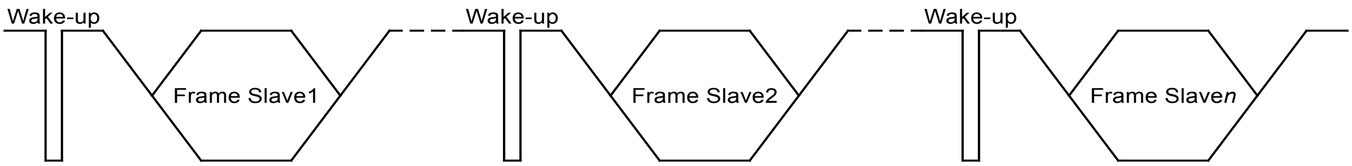


Figure 9. Multi-slave LIN Frame Schedule

Standard LIN protocol dictates that each node must process every incoming frame ID message on the bus. This forces each slave node to wake-up on every incoming message, regardless of ownership. Sending a wake-up frame followed by a single slave node frame minimizes the time that each slave node is powered "ON". The alternate approach of sending a wake-up frame followed by a sequential burst of all the slave frames will cause slave nodes to remain awake longer than necessary. The end result is an overall increase in system load current—a scenario that should be avoided.

Network Start-up and the Voltage Regulator

A multi-slave, two-wire LIN network can be implemented so long as the supply voltage to the slave node does not drop below the 5.5V minimum input voltage requirement of the ATA6617 voltage regulator. In this regard, extensive testing has shown that the network as currently configured cannot support more than three slave nodes at any one time. The effective load placed upon the LIN master pull-up resistor simply cannot source enough current to meet the minimum input voltage requirement under all operating conditions.

Ultimately, the network is limited by the voltage drop across the LIN master pull-up resistor and the cumulative load induced by the multiple slave nodes. Adding slave nodes to the network will increase the effective load placed upon LIN master pull-up resistor. The load placed upon V_{batt} results in an increased voltage drop across the master pull-up resistor, R_{LIN}, thus decreasing the input supply voltage to the slave nodes. If the input voltage falls below 5.5V, the minimum input voltage required for ATA6617 voltage regulator operation, the output will become unregulated and the slave node(s) will be rendered inoperable. In this mode of operation, the voltage regulator pass transistor behaves as a switch and the input voltage flows directly through to the regulator output. Voltage regulator current in this region is unstable and can be upwards of 3mA in excess of the normally regulated current. Operation in this unstable region will lead to non-linear increases in the voltage drop across the LIN master pull-up resistor, R_{LIN}.

Increasing the number of slave nodes on the network greatly raises the risk that an "unregulated" voltage regulator condition will occur. This is due to the brief, but instantaneous spike in the load current of each slave node when power is initially supplied to the network at start-up. Extra current is required to kick-start the voltage regulator of each slave node. Even though the average current consumption in the multi-slave network is approximately 0.8mA per slave node, an extra 2mA to 3mA of current must be factored into the overall current consumption of each node at start-up.

Four-node Network (1 Master, 3 Slaves)

Figure 10 shows the effect that the load has upon the LIN bus line at network power-on when three slave nodes are connected to the network. The plot clearly shows that slave node start-up briefly places an extra load on the network not seen during normal operation. At start-up, the LIN bus supply voltage hovers around 5.5V. Eventually, the slave node voltage regulators stabilize and the supply voltage settles to 8.2V. Network communication begins at this point.

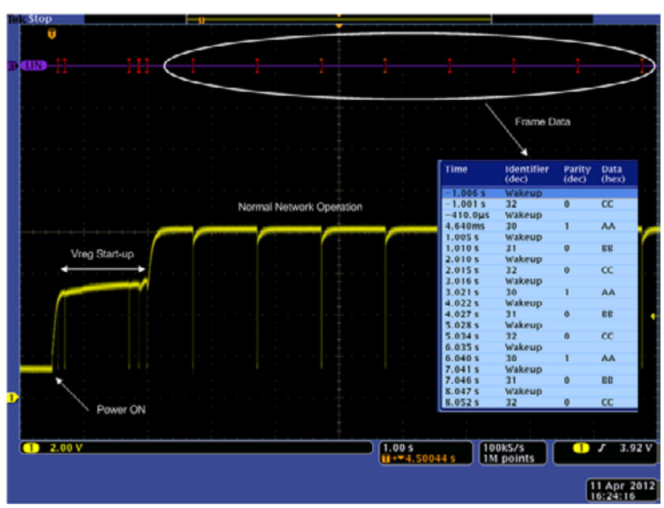


Figure 10. Three-slave Network Start-up

Five-node Network (1 Master, 4 Slaves)

Figure 11 shows the start-up behavior when a fourth slave node is added to the network. In this case, the LIN bus supply voltage is never able to recover from the start-up load condition and hovers at 5V (0.5V below the minimum operating voltage of the voltage regulator). The measured voltage drop across the LIN master pull-up resistor in this case is 3.3V.

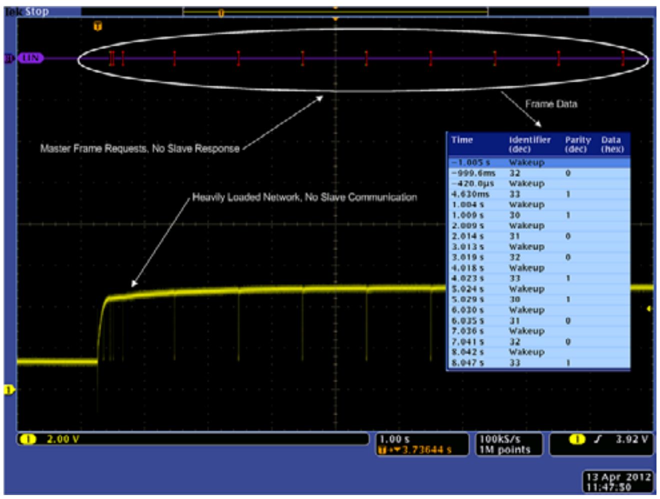


Figure 11. Four-slave Network Sequential, Start-up

The load current through the 220Ω LIN master pull-up resistor under these conditions is calculated by:

$$I_{RLIN} = V_{RLIN} / R_{LIN} = 3.3 / 220 = \underline{15mA}$$

Referencing the plot from Figure 3, one can see that the maximum load current supported by the 220Ω LIN master pull-up resistor is approximately 13mA at 5.5V. The 15mA load caused by the addition of the fourth slave node is 2mA greater than the two-wire LIN network can handle. As a result, the slave nodes fail to respond to the master frame requests.

To mitigate this effect, consider the scenario where the slave nodes are started sequentially (one node after the other, not all at once). In this case, network communication will occur as shown in Figure 12. Staggering the start-up of the individual slave nodes greatly reduces the current load on the network at reset, in effect increasing the node handling capabilities of the two-wire network.

A network using this implementation could potentially run up to 12 slave nodes under the same network conditions; a) current per slave node is 0.8mA and b) 3mA voltage regulator start-up transient is limited to one slave node at a time. Then,

$$I_{Slave\_total} = \text{number of slaves} \times I_{Slave} = 12 \times 0.8 = \underline{9.6mA}$$

and,

$$I_{Network} = I_{Slave\_total} + I_{Vreg\_start} = 9.6 + 3 = \underline{12.6mA}$$

The calculated current of 12.6mA is slightly below the 13mA maximum supply current that the LIN master is capable of supporting with a pull-up resistance of 220 ohms. In theory, this network should be possible.

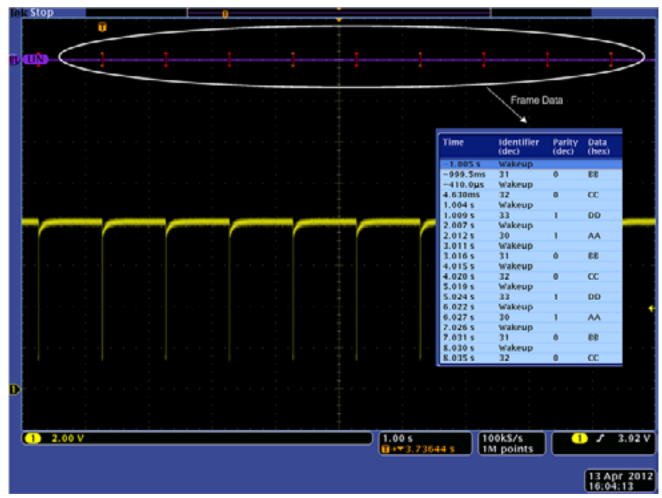


Figure 12. Four-slave Network, Serial Start-up

Conclusion

The analysis and measurements here have shown that the existing LIN networking topology (three wires, battery, ground and LIN) can be easily transformed to a two-wire implementation (LIN and ground) with very little effort. All that is required is a thorough understanding of the system supply/load requirements and several hardware modifications to enable the slave node to harvest power from the master LIN bus line in between LIN data frame transmissions. The two-wire LIN network is best suited for low-node count networks where the system is limited to one master and no more than three slaves where all nodes are powered on simultaneously. The number of slave nodes could potentially be increased if the system designer is able to implement a power-on scheme where the slave nodes are activated serially to limit the surge current at network start-up.

Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441-0311 **F:** (+1)(408) 487-2600 | **www.atmel.com**