PolarFire SLVS-EC Video Demo

AN5188

Introduction (Ask a Question)

Scalable Low-Voltage Signaling with Embedded Clock (SLVS-EC) is an advanced interface standard pioneered by Sony Semiconductor Solutions Corporation (SSS) specifically designed for rapid and high-definition image sensor transmission. It streamlines the process of constructing camera setups. Equipped with an integrated clock signal, it proves beneficial for scenarios demanding expanded capacity, enhanced speed, or extended transmission ranges.

SLVS-EC expands our extensive range of Smart Embedded Vision IPs, empowering high-speed video applications tailored for intelligent-edge devices. For more detailed information, see Smart Embedded Vision page.

The technical demonstration of the PolarFire SLVS-EC Video Demo operates seamlessly with the PolarFire video kit, SLVS-EC FMC device and an HDMI monitor. This document serves as a comprehensive guide to facilitate the execution of the demo. The design of the demo represents a fully integrated solution crafted using Microchip's Libero® SoC Design Suite.

This document describes the PolarFire SLVS-EC Video Demo, demonstrating integration with the PolarFire video kit and providing detailed instructions. The demo showcases the following functions:

1. Supports 4K video capture over SLVS-EC FMC camera and cropped to 1080p60 video output over HDMI 2.0.
2. Implements Image Signal Processing (ISP) pipeline on a raw video data.
3. Provides GUI-based image parameter controls.
4. Supports the Auto Exposure Control.

The SLVS-EC Receiver IP core offers an SLVS-EC interface for PolarFire® FPGA, is a compact receiver IP that adheres to the SLVS-EC V2.0 standards. By combining this IP with FPGA's high-speed transceiver, this IP facilitates the extraction of pixel clock and data through the high-speed serial embedded clock/data from the image sensor. This IP core supports configurations of two, four, and eight lanes, with speeds up to 4.752 Gbps per lane, and data types of Raw 8, Raw 10, and Raw 12 formats. Additionally, the SLVS-EC Rx IP core supports three Baud Rates, as listed in the following table.

Table 1. Supported SLVS-EC Baud Rate

Baud Grade	Baud Rate in Mbps
1	1188
2	2376
3	4752

Table of Contents

1. Demo Requirements (Ask a Question)

The following table lists the hardware and software required for running the demo.

Table 1-1. Demo Requirements

Requirement	Description
Hardware and Accessories	
PolarFire® video kit	MPF300-VIDEO-KIT-NS Kit Contents: • PolarFire Video and Imaging board with MPF300T-1FCG1152E Device • Dual Camera Sensor board – VIDEO-DC-DUALCAM • HDMI cable • 12V power pack/AC adapter • USB 2.0 A male to mini-B
SLVS-EC FMC	VIDEO-DC-SLVS
HDMI Monitor	1920 x 1080, 60 Hz resolution monitor for the HDMI 2.0 transmitter (Tx) port
Software	
`Program_Debug_v24.1_win.exe`	This executable file installs FlashPro Express, used to program FPGA

2. Demo Prerequisites (Ask a Question)

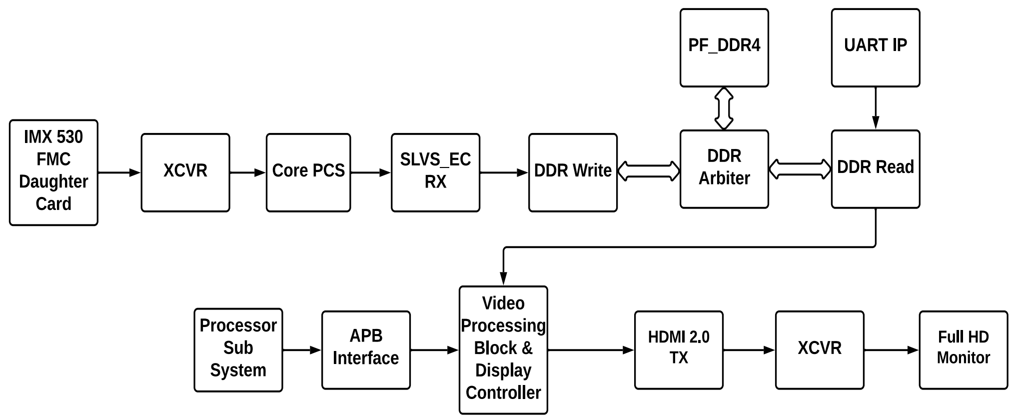
Before you begin, perform the following steps:

- Download the design files from the following link: AN5188: PolarFire SLVS-EC Video Demo
- Download and install the Libero® SoC Design Suite from Libero SoC Software Downloads

3. Design Description (Ask a Question)

The following figure shows a high-level block diagram of the design.

Figure 3-1. Block Diagram



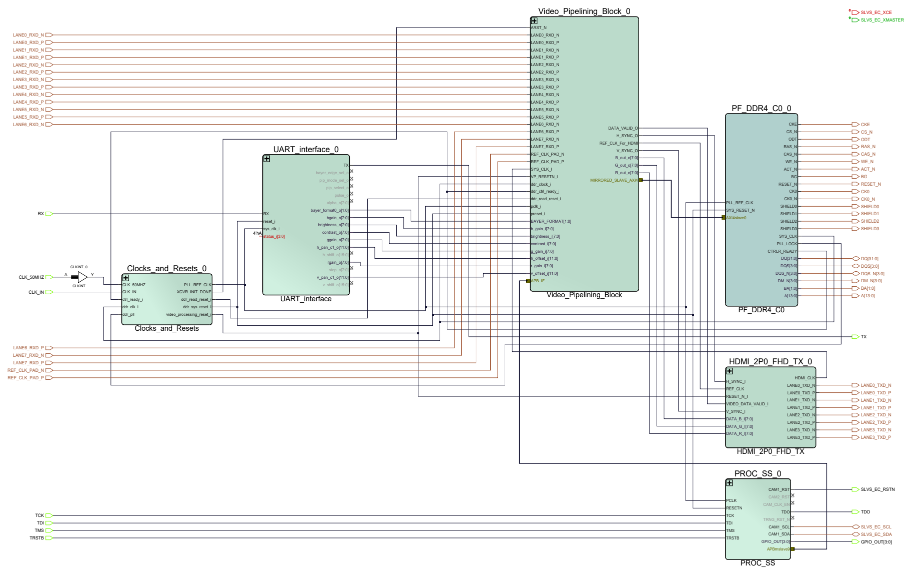
The following steps outline the preceding block diagram:

1. The IMX-530 SLVS FMC captures video data through the transceiver (XCVR), passes it to the Core PCS, and finally routes it to the SLVS-EC Rx IP.
2. The SLVS-EC Rx IP decodes the SLVS-EC format and generates RAW pixel output, which is stored in the DDR memory as a video frame (consisting of PolarFire® DDR4, DDR Write, DDR Read, and DDR Arbiter).
3. The Raw video frame is read back and processed through the video pipeline consisting of Bayer interpolation, Gamma correction, and Image enhancement.
4. The processed video is streamed over HDMI output by using Display Controller and HDMI 2.0 Tx IP.
5. This design also integrates a separate processing block, the PROC_SUB_SYSTEM, which is responsible for initializing the IMX-530 camera through the I2C interface.

3.1 Hardware Implementation (Ask a Question)

The following figure shows the Libero SoC implementation of the top-level SmartDesign.

Figure 3-2. High-Level SLVS-EC Design



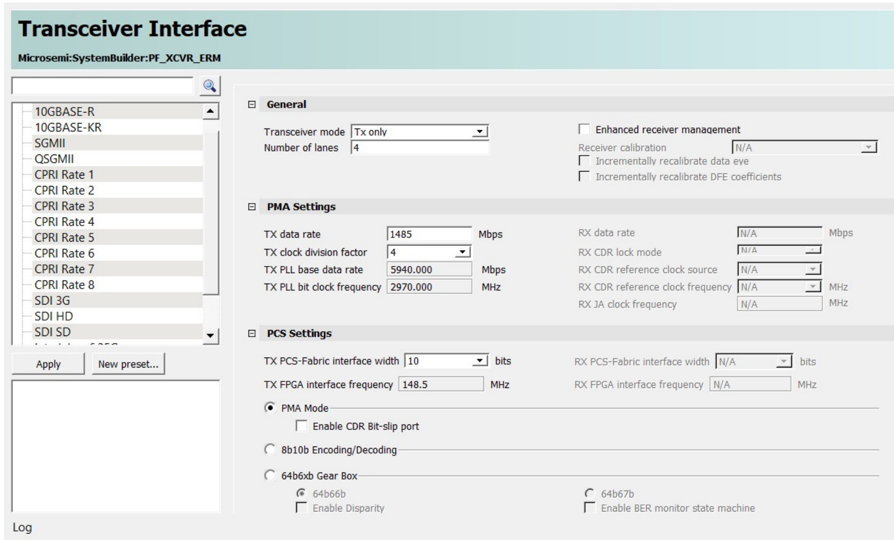
The SLVS-EC design includes the following key blocks:

- HDMI_2P0_FHD_TX (TX_PLL, HDMI 2.0 TX, and XCVR)
- Video_Pipelining_Block (DDR Write, DDR Read, DDR AXI4 Arbiter, and Display Controller)
- IMX_TOP (SLVS-EC RX, Core PCS, and XCVR)
- Video Processing Block (Bayer_Interpolation, Gamma_Correction, and Image_Enhancement)
- PF_DDR4
- PROC_SS (MIV_RV32, CoreGPIO, PF_SRAM_AHBL_AXI, and COREI2C)
- UART Interface (COREUART)

XCVR Configuration -1

The transceiver configuration for HDMI Tx implementation is shown in the following figure. The transceiver is configured in Tx only mode in 4 lane configuration. The clock signal is carried by LANE0, while lanes 1, 2, and 3 carry the blue, green, and red video signals. The transceiver is configured for Full High Definition (FHD) which is 1920 x 1080p at 60 frames per second. This configuration is labeled as XCVR Configuration -1, as shown in the following figure.

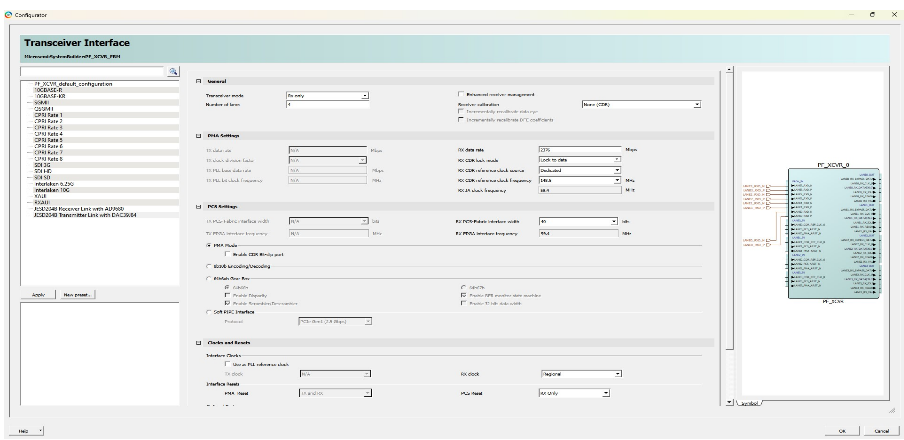
Figure 3-3. XCVR Configuration -1



XCVR Configuration -2

The SLVS-EC Rx is configured to operate in an 8-lane mode and hence, 8-transceiver Rx-lanes are required to receive the video data. The PolarFire FPGA implements transceiver lanes grouped in quads, each consisting of four lanes. Hence, two transceiver quads are used to implement 8-lane configuration. Both the quads use the same configuration as shown in the following figure.

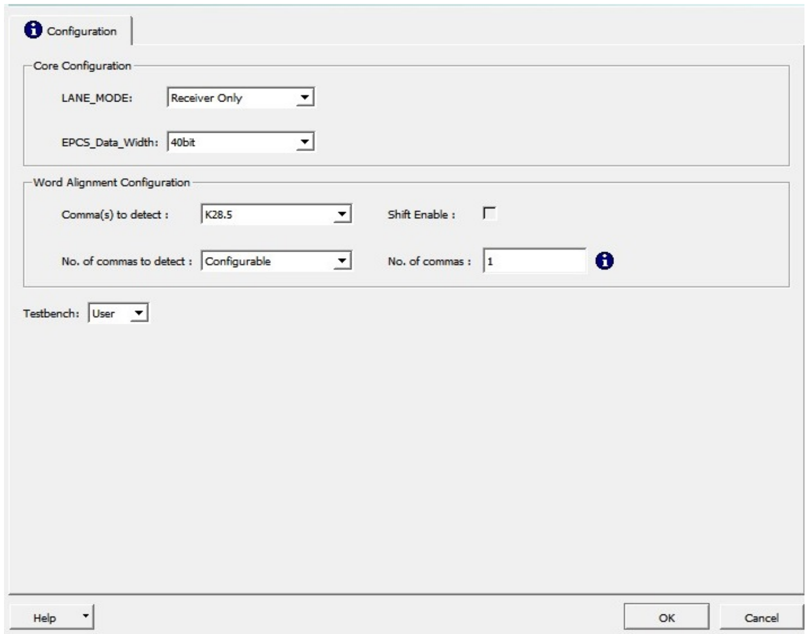
Figure 3-4. XCVR Configuration -2



CorePCS Configuration

CorePCS consists of a user interface and a transceiver interface. The user interface includes transmit and receive data functionalities, along with various control and status signals that qualify the data. The Core PCS IP in the design, the **LANE_MODE** is set to Receiver Only with **EPCS_Data_Width** as 40 bit, **Comma(s) to detect** is configured as “K28.5”, and **No. of commas** is configured to “1”, as shown in the following figure.

Figure 3-5. CorePCS Configuration



SLVS-EC Rx IP Configuration

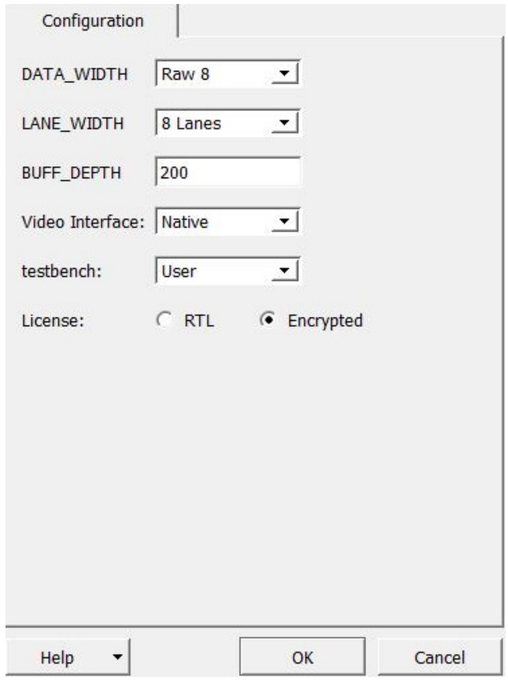
SLVS-EC Rx IP has the following configuration options:

- DATA WIDTH has configuration options as Raw 8, Raw 10, and Raw 12
- LANE WIDTH has configuration options as two lanes, four lanes, and eight lanes
- Video Interface has configuration options as Native and AXI4 Stream

For more information about SLVS-EC Rx IP, see UG0877: SLVS-EC Receiver for PolarFire FPGA user guide.

The SLVS-EC Rx IP is configured with a native interface, which uses a Raw 8 configuration and a 8-lane width.

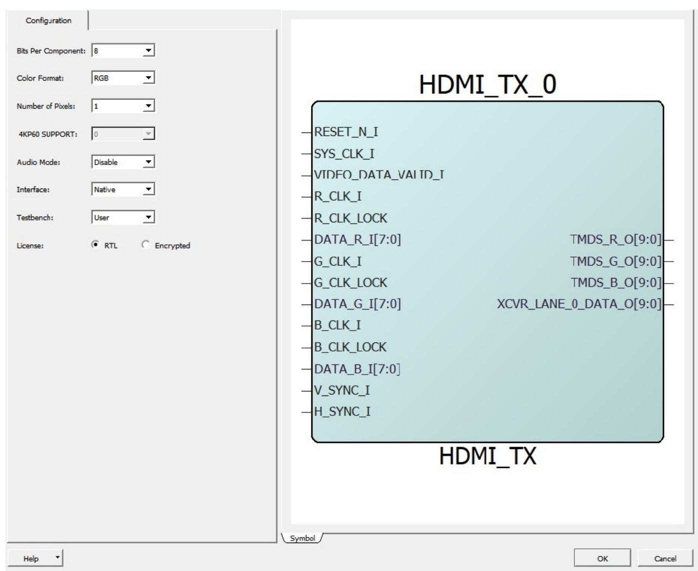
Figure 3-6. SLVS-EC Rx IP Configuration using Raw 8 and 8-Lane Width for Native Interface



HDMI TX IP Configuration

HDMI Tx IP core is configured in Single bit mode for native interface. HDMI Tx IP encodes video, auxiliary, and control data to Transition-minimized Differential Signaling (TMDS) data, which pass through transceiver.

Figure 3-7. HDMI TX 2.0 IP Configuration using Single-bit Mode for Native Interface



3.2 I/O Ports (Ask a Question)

The following table lists the important I/O ports of the design.

Table 3-1. Input and Output Ports

Port Name	Direction	Description
LANE0_RXD_N	Input	Lane0 RX channel N
LANE0_RXD_P	Input	Lane0 RX channel P
LANE1_RXD_N	Input	Lane1 RX channel N
LANE1_RXD_P	Input	Lane1 RX channel P
LANE2_RXD_N	Input	Lane2 RX channel N
LANE2_RXD_P	Input	Lane2 RX channel P
LANE3_RXD_N	Input	Lane3 RX channel N
LANE3_RXD_P	Input	Lane3 RX channel P
LANE4_RXD_N	Input	Lane4 RX channel N
LANE4_RXD_P	Input	Lane4 RX channel P
LANE5_RXD_N	Input	Lane5 RX channel N
LANE5_RXD_P	Input	Lane5 RX channel P
LANE6_RXD_N	Input	Lane6 RX channel N
LANE6_RXD_P	Input	Lane6 RX channel P
LANE7_RXD_N	Input	Lane7 RX channel N
LANE7_RXD_P	Input	Lane7 RX channel P
LANE0_TXD_N	Output	Lane0 TX channel N
LANE0_TXD_P	Output	Lane0 TX channel P
LANE1_TXD_N	Output	Lane1 TX channel N
LANE1_TXD_P	Output	Lane1 TX channel P
LANE2_TXD_N	Output	Lane2 TX channel N
LANE2_TXD_P	Output	Lane2 TX channel P
LANE3_TXD_N	Output	Lane3 TX channel N
LANE3_TXD_P	Output	Lane3 TX channel P
REF_CLK_PAD_N	Input	Reference clock N
REF_CLK_PAD_P	Input	Reference clock P
CLK_IN	Input	27 MHZ of CLK
RX	Input	RX for UART Interface
TCK	Input	TCLK for Flash Pro Debug
TDI	Input	TDI for Flash Pro Debug
TMS	Input	TMS for Flash Pro Debug
TSRTB	Input	TSRTB for Flash Pro Debug
SLVS_EC_XCE	Output	Serial Communication Interface XCE Pin for i2c (Fixed to HIGH)
SLVS_EC_XMASTER	Output	Master/Slave Select (Slave Mode: HIGH, Master Mode: LOW)
SLVS_EC_RSTN	Output	SLVS Camera Reset
CLK_50MHZ	Input	50 MHz of On Board Clock
TDO	Output	TDO for Flash Pro Debug
SLVS_SCL	Input and Output	SLVS Cam I2C SCL
SLVS_SDA	Input and Output	SLVS Cam I2C SDA
GPIO_OUT_0[3:0]	Output	GPIO_OUT_0 is connected to LED0, 1, 2, 3.
TX	Output	Tx for UART Interface

3.3 Clocking Structure (Ask a Question)

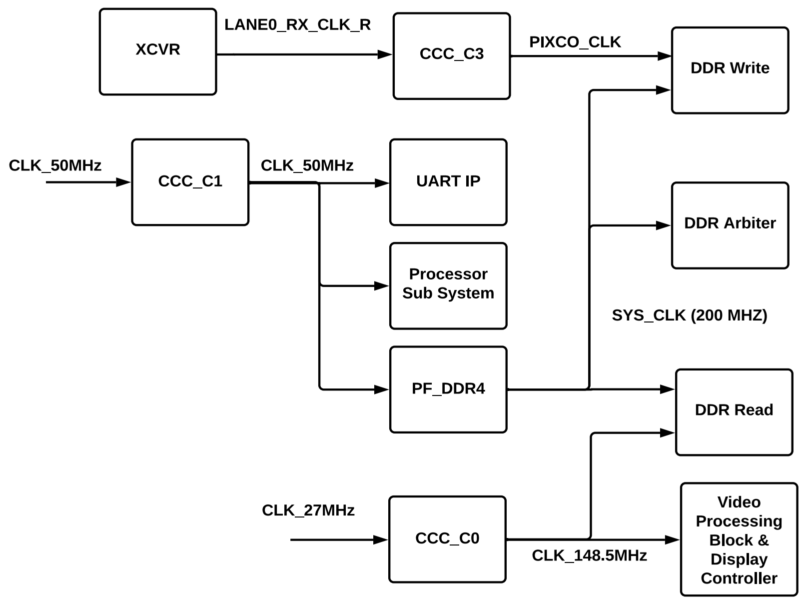
The design uses the following on-board clocks:

- The 27 MHz oscillator is used to provide a reference clock to PF_CCC_C0

- The on-board 50 MHz clock, which is driven as DDR Reference Clock, Processor Sub System, and UART Interface
- The XCVR TX PLL subsystem generates a bit clock and XCVR receives
- The LANE0_RX_CLK_R XCVR Clock provides a reference clock to PF_CCC_C3 and generates 59.4 MHz

The following figure shows the clocking structure of the design.

Figure 3-8. Clocking Structure

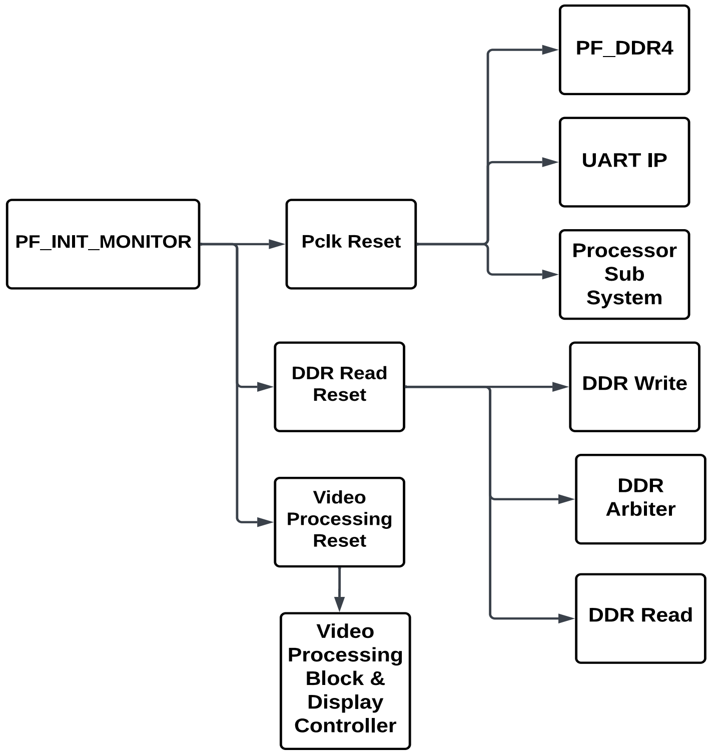


3.4 Reset Structure (Ask a Question)

The SLVS-EC design is initialized upon the de-assertion of the DEVICE_INIT_DONE signal from the PF_INIT_MONITOR block, along with the XCVR_INIT_DONE signal from the same block. In addition to this primary reset, the design incorporates three additional resets, each synchronized with a specific clock. The first reset, DDR_Write_reset, resets the DDR write operations and is synchronized with the clock from the SLVS-EC Rx IP. The second reset, Video processing reset, resets all the video processing IP and display controller IP, using the 148.5 MHz clock. The third reset, DDR_SYSTEM_reset, resets DDR read and arbiter operations, as well as other reset operations, utilizing the clock from the onboard 27 MHz source.

The following figure shows the reset structure of the design.

Figure 3-9. Reset Structure



4. Installing the Demo GUI (Ask a Question)

To install the GUI, perform the following steps:

1. Extract the contents of the `mpf_an5188_v2024p1_gui\Video_Control_GUI_V3.1.1_Installer\Volume` file and run the `setup.exe` file.
2. Click **Yes** for any message from User Account Control. The Video Control GUI installation wizard is displayed.
3. Confirm the installation directory locations for the GUI and the National Instruments products, and then click **Next**.
4. Accept the license agreement, and then click **Next**.
5. Review the summary and click **Next**, then installation proceeds with a progress bar. After the installation, a confirmation message is displayed.
6. Click **Next** to exit the installation wizard.
7. Restart the host PC, when prompted. The Video Control GUI is installed.

For more information about the related steps, see DG0849: PolarFire 4K FPGA Dual Camera Video Kit.

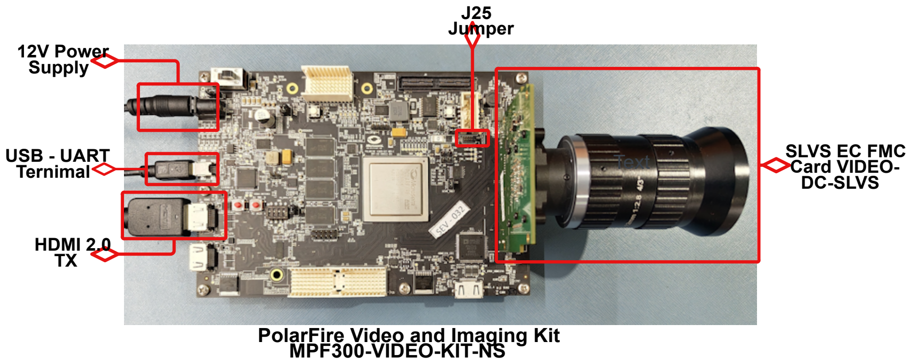
5. Setting Up the Demo (Ask a Question)

Setting up the demo involves the following steps.

5.1 Setting Up the Hardware (Ask a Question)

The following figure shows the hardware setup of SLVS-EC FMC with PolarFire video kit and interface with HDMI display.

Figure 5-1. Setting up the Hardware



The following table lists the jumper settings of PolarFire video kit.

Table 5-1. Jumper and Switch Settings of PolarFire Video Kit

Jumper	Default Position	Description
J15	Open	SPI Slave and Master mode selection By default, select SPI master
J17	Open	100K PD for TRSTn By default, 1K PD is connected
J19	Pin 1 and 2	Default: XCVR_VREF is connected to GND
J28	Pin 1 and 2	Default: Programming through the FTDI
J24	Pin 2 and 4	Default: VDDAUX4 voltage is set to 3.3V
J25	Pin 1 and 2	Bank4 voltage is set to 3.3V
J36	Pin 1 and 2	Default: Board power up through the SW4
SW4	OFF/ON	Power ON\OFF slide switch
SW6	OFF	User slide switch Default position: OFF
J20	12 Volts Input	12V input to the board

For setting up the hardware, perform the following steps:

1. Connect the VIDEO-DC-SLVS to the **J14** FMC Connector on the PolarFire video kit.
2. Connect the power supply cable to **J20** of the PolarFire video kit.
3. Connect the host PC to the PolarFire video kit through **J12** using a USB mini cable.
4. Connect the HDMI monitor to **J1** (HDMI 2.0 transmitter (Tx) port) of the PolarFire video kit.
5. Power up the HDMI monitor.
6. Power up the board using the **SW4** slide switch.

5.2 Programming the Device using FlashPro Express (Ask a Question)

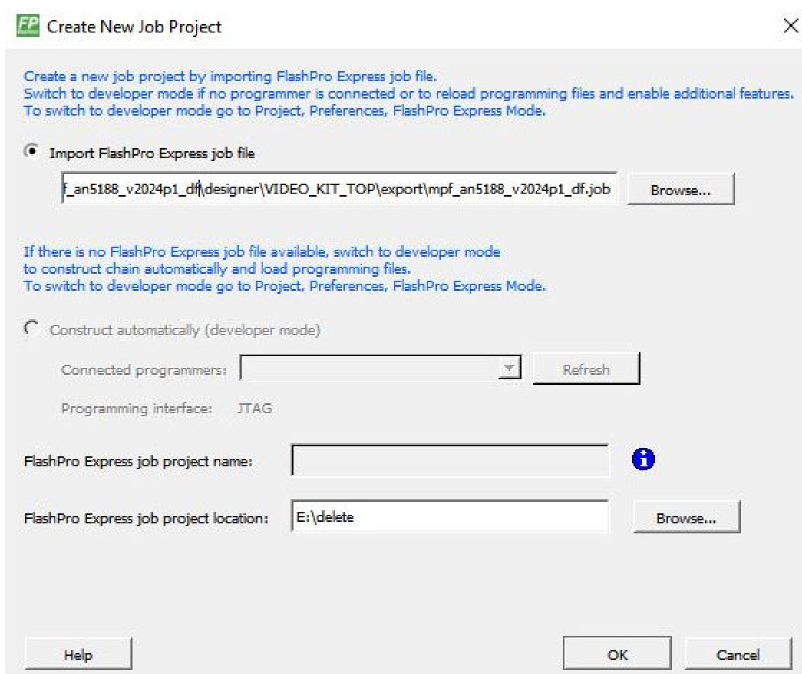
To program the PolarFire device with the `.job` file provided as part of the design files using the FlashPro Express software.

This section describes how to program the PolarFire device with the .job file using FlashPro Express. The mpf_an5188_v2024p1_df.job file is available at the following location: <download_folder>\mpf_an5188_v2024p1_jb

To program the PolarFire device with the .job file, perform the following steps:

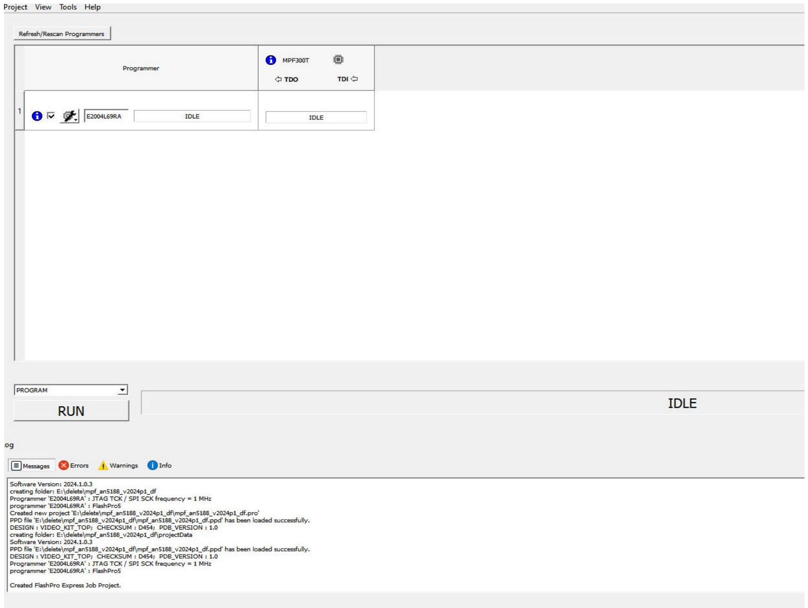
1. On the Host PC, start the FlashPro Express software from its installation directory.
2. To create a new job project on the Project menu, click **New** or **New Job Project from FlashPro Express Job**.
3. In the **New Job Project from FlashPro Express Job** dialog box, perform the following steps:
   – **Programming job file**: Click **Browse** and navigate to the location where the mpf_an5188_v2024p1_df.job file is located and select the file. The default location is <download_folder>\mpf_an5188_v2024p1_df\Programming_Job
   – **FlashPro Express job project location**: Select **Browse** and navigate to the location where you want to save the project.

Figure 5-2. New Job Project from FlashPro Express Job



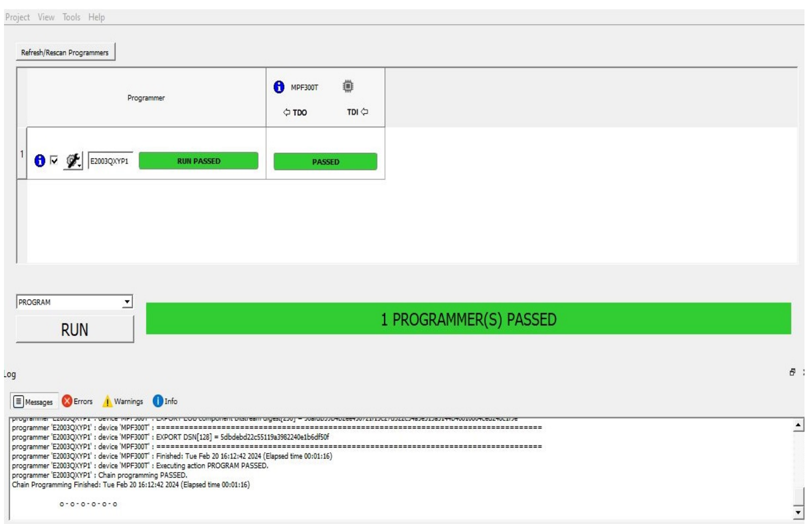
4. Click **OK**. The required programming file is selected and ready to be programmed in the device. The FlashPro Express window appears.
5. Verify that a programmer number appears in the **Programmer** box. If it does not, verify the board connections and click **Refresh/Rescan Programmers**.

Figure 5-3. Programming the Device



6. To program the device, click **Run**. When the device is programmed successfully, a **Run PASSED** status is displayed, as shown in the following figure.

Figure 5-4. FlashPro Express—RUN PASSED



7. To Close FlashPro Express, click **Project** > **Exit**. The PolarFire device is programmed.
8. To Power cycle the board, press the **SW4** switch. After power cycling, the full HD displays the video from the camera.

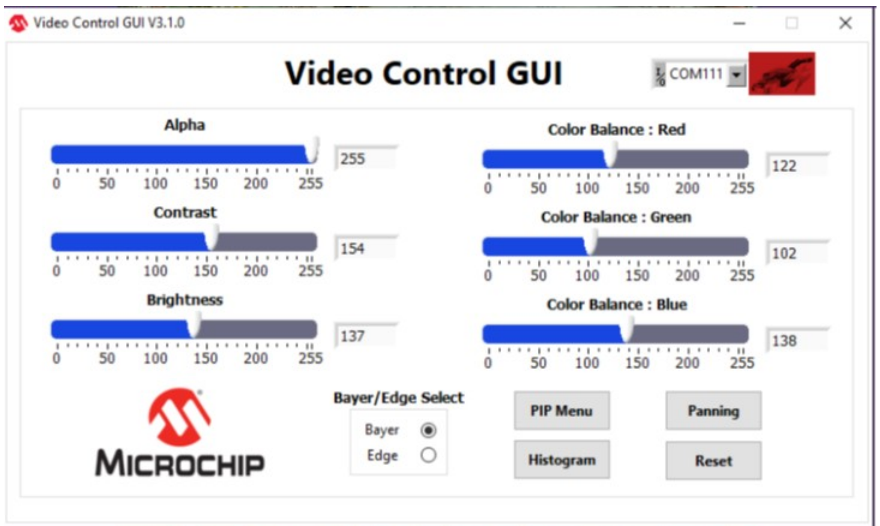
6. Running the Demo (Ask a Question)

Running the demo involves verifying the imaging and video settings using the Video Control GUI, and then observing the video output on the HDMI monitor.

To use the demo GUI, perform the following steps:

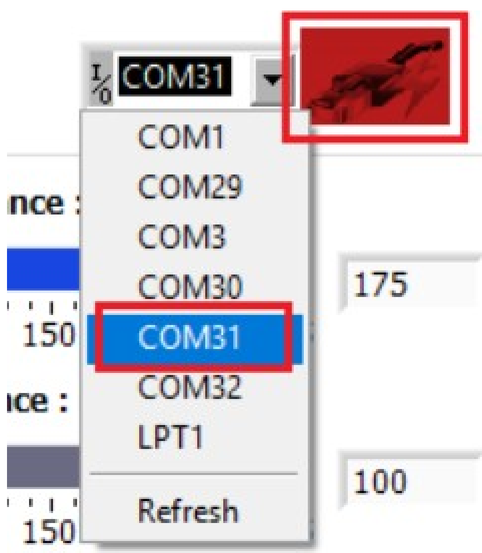
1. Start the **Video Control GUI** from the installation directory, see the following figure.

Figure 6-1. Video Control GUI



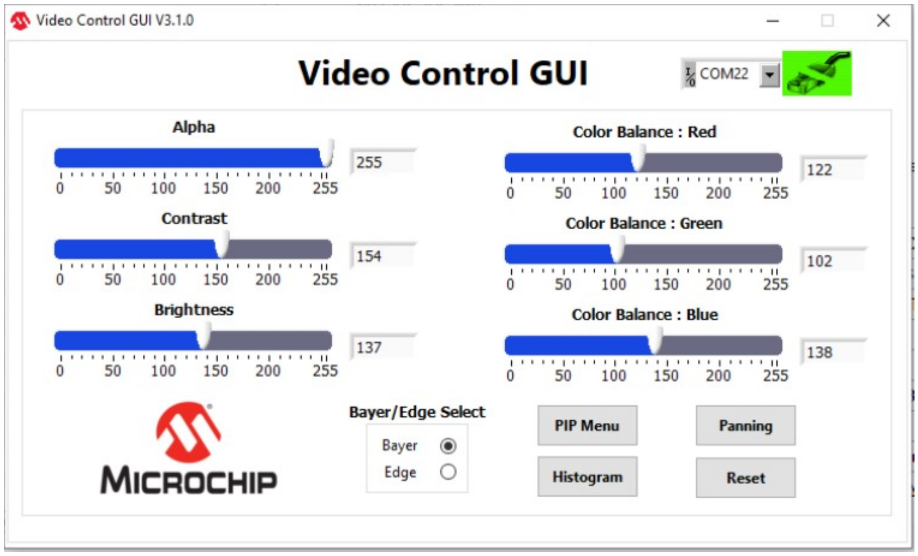
2. In the **I/O** list, click the second largest COM port, and then click **Connect**.

Figure 6-2. Connecting the GUI and Video Kit



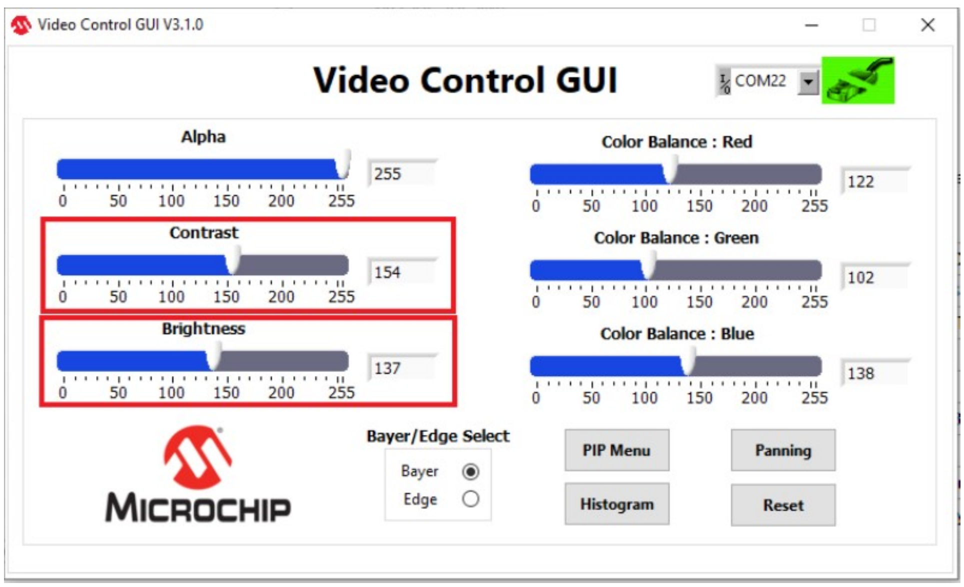
The following figure shows that the Connect button turns green indicating a successful connection.

Figure 6-3. Connection Successful



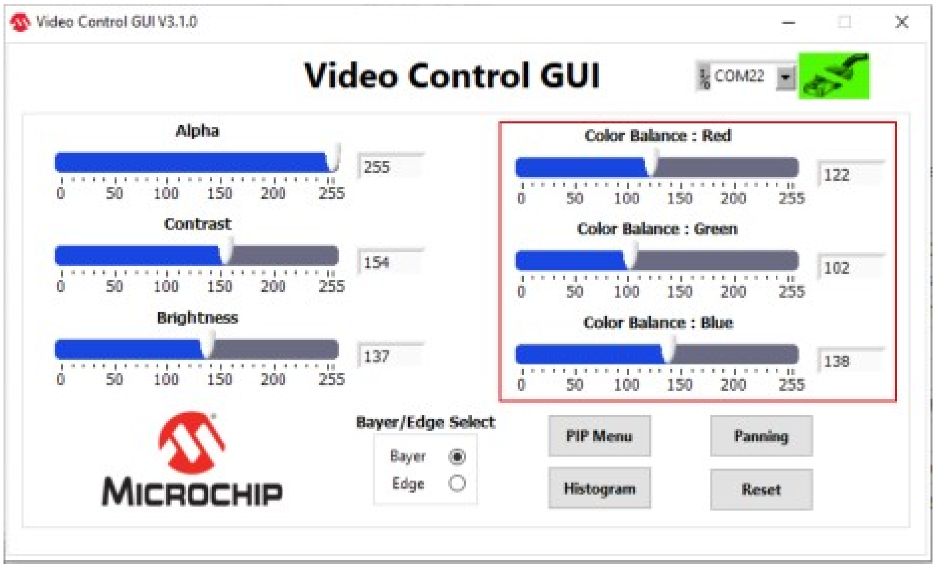
3. Move the corresponding sliders appropriately to adjust the contrast and brightness and observe the change on the HDMI monitor.

Figure 6-4. Adjusting Contrast and Brightness



4. Similarly, move the sliders to adjust the color balance of the image using the color balance sliders.

Figure 6-5. Color Balance



Important: **PIP Menu**, **Panning**, **Histogram**, and **Edge Detection** options are not supported in this demo.

7. Appendix A: Running the Tcl Script (Ask a Question)

Tcl scripts are provided in PolarFire Video Kit Reference Design.

To run Tcl, perform the following steps:

1. Launch the Libero software.
2. Click **Project** > **Execute Script**.
3. In the downloaded **mpf_an5188_v2024p1_df** directory, select `script.tcl`.
4. Click **Run**.

After successful execution of the Tcl script, the Libero project is created within the top directory. For more information, check the Log file `mpf_an5188_v2024p1_df_log`.

For more details about the folder structure of `mpf_an5188_v2024p1_df` and Tcl scripts and commands, see the `TCL_Scripts_readme.txt` and Tcl Commands Reference Guide. Contact Technical Support for any queries about running the Tcl script.

8. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 8-1. Revision History

Revision	Date	Description
B	06/2024	The following is the list of changes in revision B of the document: • Updated Figure 3-1 and Step 1 in 3. Design Description section • Updated Figure 3-4 and Figure 3-7 in 3.1. Hardware Implementation section • Updated Figure 5-1 and added Table 5-1 in 5.1. Setting Up the Hardware section • Updated `.job` file location in 5.2. Programming the Device using FlashPro Express section • Updated 7. Appendix A: Running the Tcl Script section
A	04/2024	Initial release

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