

2.5 GHz, Any Differential In-to-LVPECL, Programmable Clock Divider/Fanout Buffer with Internal Termination

Features

- Integrated Programmable Clock Divider and 1:2 Fanout Buffer
- Guaranteed AC Performance over Temperature and Voltage:
 - >2.5 GHz f_{MAX}
 - <250 ps t_r/t_f
 - <15 ps Within-Device Skew
- Low Jitter Design:
 - <10 ps_{pp} Total Jitter
 - <1 ps_{RMS} Cycle-to-Cycle Jitter
- Unique Input Termination and V_T Pin for DC-Coupled and AC-Coupled Inputs; CML, PECL, LVDS, and HSTL
- TTL/CMOS Inputs for Select and Reset
- 100KEP-Compatible LVPECL Outputs
- Parallel Programming Capability
- Programmable Divider Ratios of 1, 2, 4, 8, and 16
- Low-Voltage Operation: 2.5V or 3.3V
- Output Disable Function
- -40°C to +85°C Temperature Range
- Available in 16-Pin (3 mm x 3 mm) QFN Package

Applications

- SONET/SDH Line Cards
- Transponders
- High-End Multiprocessor Sensors

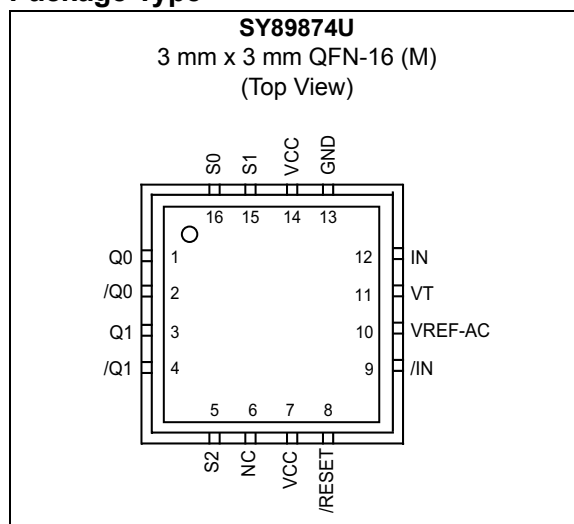
General Description

This low-skew, low-jitter device is capable of accepting a high-speed (e.g., 622 MHz or higher) CML, LVPECL, LVDS, or HSTL clock input signal and dividing down the frequency using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock. Available divider ratios are 2, 4, 8, and 16, or straight pass-through. In a typical 622 MHz clock system this would provide availability of 311 MHz, 155 MHz, 77 MHz, or 38 MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN).

Package Type



The diagram illustrates the internal architecture of the ADXL045 digital accelerometer. Key components include:

- ENABLE FF (Flip-Flop):** Receives $\overline{\text{RESET}}$ and S2 (via an inverter). Its output enables the MUX and the DIVIDED BY counter.
- ENABLE MUX:** Receives signals from the ENABLE FF and the DIVIDED BY counter to control the MUX.
- DIVIDED BY (2, 4, 8 or 16):** Receives signals from the ENABLE FF and the DECODER to provide a clock signal to the MUX.
- MUX (Multiplexer):** Selects between the IN signal (via a resistor network R0 , R1) and the output of the DIVIDED BY counter based on the S0 and S1 address inputs.
- Output Stage:** The MUX output is buffered and inverted to produce the Q0 , Q1 digital outputs and their complements /Q0 , /Q1 .

Inputs and outputs are labeled as follows:

- Inputs:** S2 , $\overline{\text{RESET}}$, IN , Vt , /IN , S0 , S1 .
- Outputs:** Q0 , /Q0 , Q1 , /Q1 .

/RESET	S2	S1	S0	Outputs
1	0	X	X	Reference clock (pass-through)
1	1	0	0	Reference clock ÷ 2
1	1	0	1	Reference clock ÷ 4
1	1	1	0	Reference clock ÷ 8
1	1	1	1	Reference clock ÷ 16
0	1	X	X	Q = Low, /Q = High clock disable

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (V_{IN})	–0.5V to $V_{CC} + 0.3V$
ECL Output Current	
Continuous	50 mA
Surge	100 mA
Input Current I_N , $/I_N$ (I_{IN})	±50 mA
V_T Current (I_{VT})	±100 mA
V_{REF-AC} Sink/Source Current ($I_{VREF-AC}$) (Note 1)	±2 mA

Operating Ratings ††

Supply Voltage (V_{CC})	+3.3V ±10% or +2.5V ±5%
-----------------------------------	-------------------------

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise stated.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply	V_{CC}	2.375	—	3.63	V	—
Power Supply Current	I_{CC}	—	50	75	mA	No load, max. V_{CC}
Differential Input Resistance (IN-to-/IN)	R_{IN}	90	100	110	Ω	—
Input High Voltage (IN, /IN)	V_{IH}	0.1	—	$V_{CC} + 0.3$	V	Note 2
Input Low Voltage (IN, /IN)	V_{IL}	-0.3	—	$V_{IH} - 0.1$	V	Note 2
Input Voltage Swing	V_{IN}	0.1	—	V_{CC}	V	Note 2, Note 3
Different Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	Note 2, Note 3, Note 4
Input Current (IN, /IN)	I_{IN}	—	—	45	mA	Note 2
Reference Voltage	V_{REF-AC}	$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	V	Note 5

- Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- 2:** Due to the internal termination (see [Input Buffer Structure](#)), the input current depends on the applied voltages at IN, /IN, and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit. Performance might be impacted if the differential inputs are driven single-ended.
- 3:** See [Timing Diagram](#) for V_{IN} definition. V_{IN} (maximum) is specified when V_{IN} is floating.
- 4:** See [Definition of Single-Ended and Differential Swing](#) section for V_{DIFF} definition.
- 5:** Operating using V_{REF-AC} is limited to AC-coupled PECL or CML applications only. Connect directly to the V_T pin.

LVPECL (100KEP) DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.3\text{V} \pm 10\%$ or $2.5\text{V} \pm 5\%$; $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $R_L = 50\Omega$ to $V_{CC} - 2\text{V}$, unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	$V_{CC} - 1.145$	$V_{CC} - 1.020$	$V_{CC} - 0.895$	V	—
Output Low Voltage	V_{OL}	$V_{CC} - 1.945$	$V_{CC} - 1.820$	$V_{CC} - 1.695$	V	—
Output Voltage Swing	V_{OUT}	550	800	1050	mV	—
Differential Output Voltage Swing	V_{DIFF_OUT}	1.10	1.60	2.10	V	—

- Note 1:** The circuit is designed to meet the DC specifications shown in the LVPECL (100KEP) Electrical Characteristics table after thermal equilibrium has been established.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	-125	—	20	μA	—
Input Low Current	I_{IL}	-300	—	—	μA	—

Note 1: The circuit is designed to meet the DC specifications shown in the LVTTL/CMOS Electrical Characteristics table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$; $T_A = -40^\circ C$ to $+85^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated. [Note 1](#), [Note 2](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Output Toggle Frequency	f_{MAX}	2.5	—	—	GHz	Output swing ≥ 400 mV
Maximum Input Frequency		3.2	—	—		Divide by 2, 4, 8, 16
Differential Propagation Delay IN-to-Q	t_{PD}	540	650	790	ps	Input swing < 400 mV
		480	600	730		Input swing ≥ 400 mV
Within Device Skew (Differential) Q0 - Q1	t_{SKEW}	—	7	15	ps	Note 3
Part-to-Part Skew (Differential)		—	—	250		
Reset Recovery Time	t_{RR}	600	—	—	ps	Note 4
Cycle-to-Cycle Jitter	t_{JITTER}	—	—	1	ps _{RMS}	Note 5
Total Jitter		—	—	10	ps _{PP}	Note 6
Additive Phase Jitter		—	81	—	fs _{RMS}	Integration Range: 12 kHz to 20 MHz, Carrier: 622.08 MHz, $T_A = +25^\circ C$
Rise/Fall Time (20% to 80%)	t_r/t_f	70	150	250	ps	—

Note 1: Measured with 400 mV signal, 50% duty cycle, all outputs loaded with 50Ω to $V_{CC} - 2V$, unless otherwise stated.

2: Specification for packaged product only.

3: Skew is measured between outputs under identical transitions.

4: See the [Timing Diagram](#) section.

5: Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER_CC} = t_n - t_{n+1}$, where "t" is the time between rising edges of the output signal.

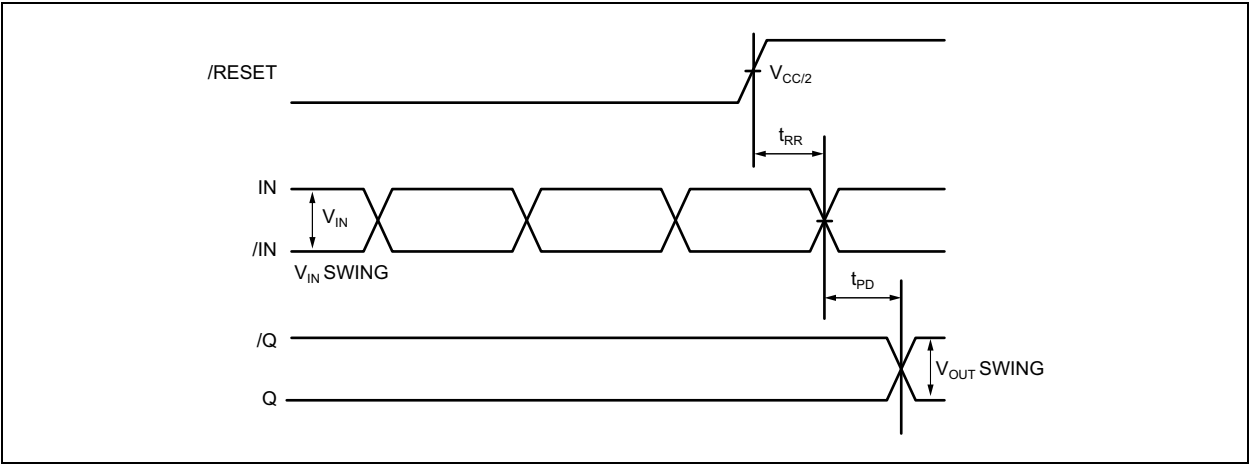
6: Total jitter definition: With an ideal clock input, of frequency $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T _A	−40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	T _S	−65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, 3x3 QFN-16Ld	θ _{JA}	—	60	—	°C/W	Still-air
	θ _{JA}	—	54	—	°C/W	500 lpm
	ψ _{JB}	—	32	—	°C/W	Junction-to-board, Note 1

Note 1: Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB.

Timing Diagram



2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

$V_{CC} = 3.3V$, $V_{IN} = 400\text{ mV}$, $T_A = +25^\circ\text{C}$, unless otherwise stated.

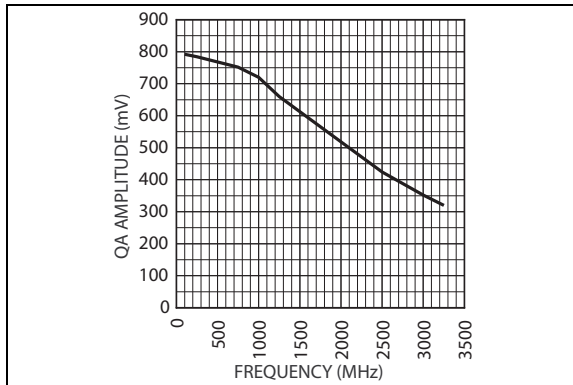


FIGURE 2-1: QA Output Amplitude vs. Frequency.

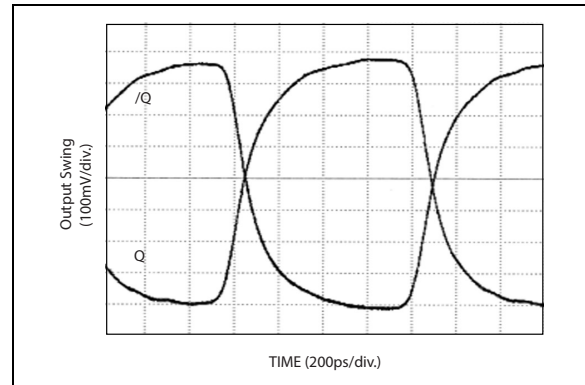


FIGURE 2-4: 622 MHz Output.

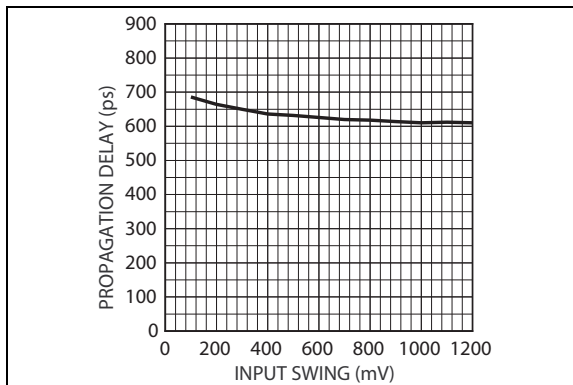


FIGURE 2-2: IN-to-Q Propagation Delay vs. Input Swing.

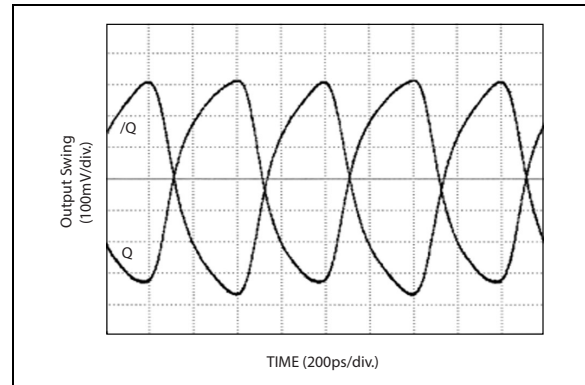


FIGURE 2-5: 1.25 GHz Output.

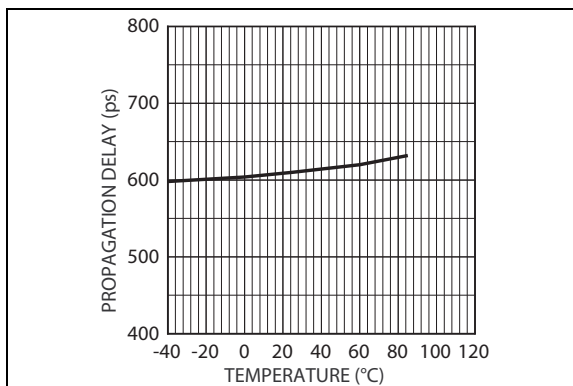


FIGURE 2-3: IN-to-Q Propagation Delay vs. Temperature.

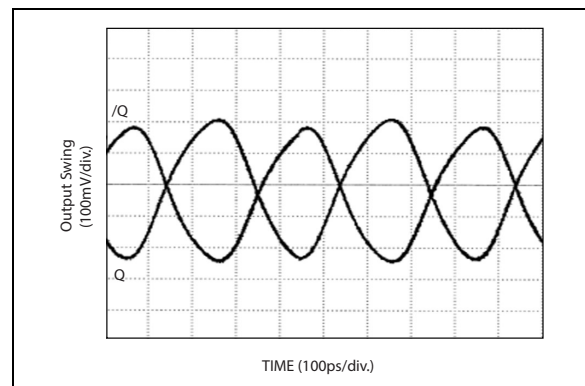


FIGURE 2-6: 2.5 GHz Output.

3.0 ADDITIVE PHASE NOISE PLOT

Additive jitter is defined as the RMS Jitter of the device added to the input signal and is calculated in [Equation 3-1](#).

EQUATION 3-1:

$$DeviceAdditiveJitter = \sqrt{OutputRMSJitter^2 - InputRMSJitter^2}$$

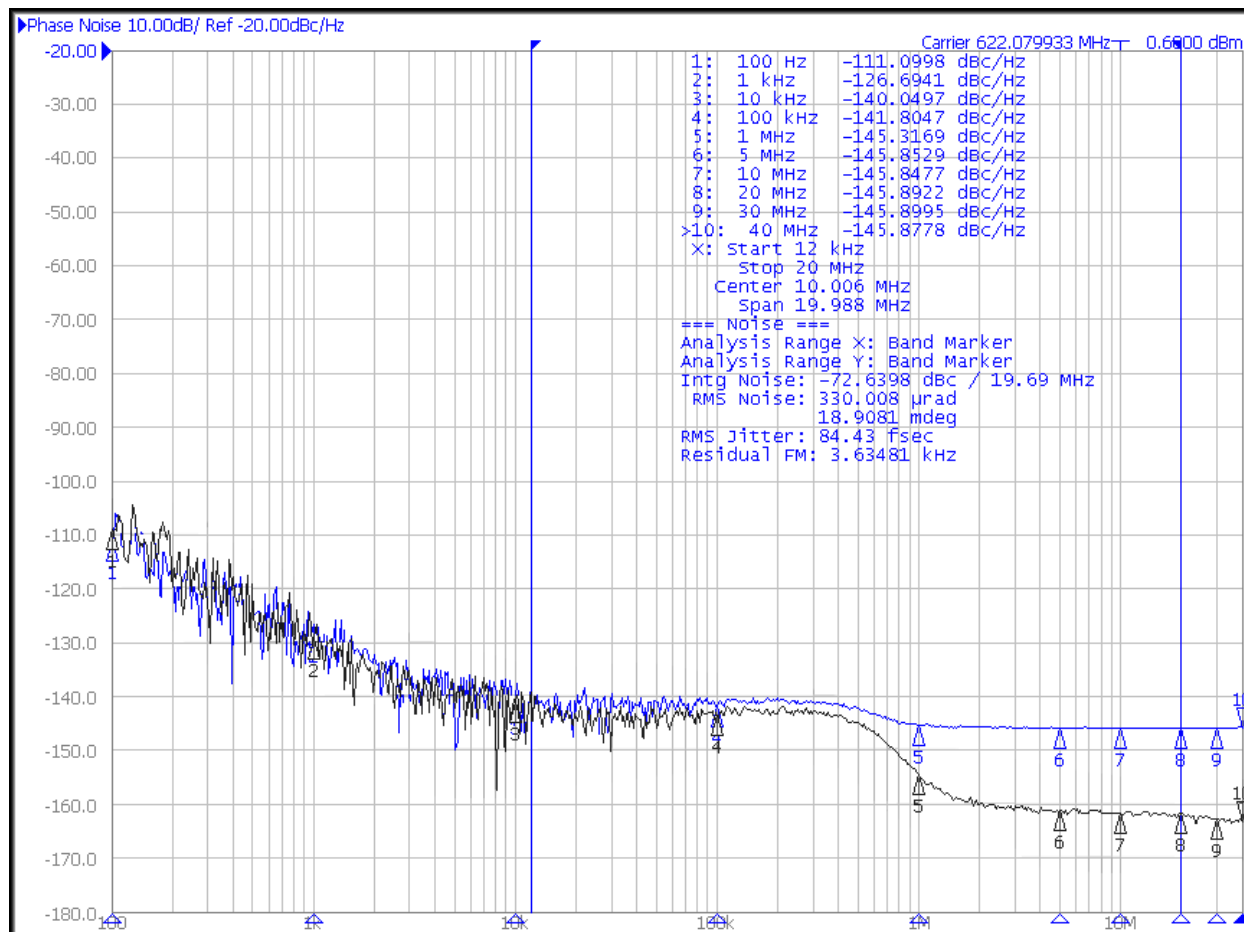


FIGURE 3-1: Integrated Phase Noise Plot of SY89874U (Device) and the Source (Input Signal).

From the plot shown in [Figure 3-1](#), the device additive jitter can be calculated as follows.

EQUATION 3-2:

$$CalculatedAdditiveJitter = \sqrt{84.43^2 - 23.07^2} = 81.21fs$$

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 4-1](#).

TABLE 4-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
12, 9	IN, /IN	Differential input. Internal 50Ω termination resistors to V_T input. Flexible input accepts any differential input. See the Input Interface Applications section.
1, 2, 3, 4	Q0, /Q0 Q1, /Q1	Differential buffered LVPECL Outputs. Divided by 1, 2, 4, 8, or 16. See Truth Table . Unused PECL outputs may be left floating with no impact on jitter performance.
16, 15, 5	S0, S1, S2	Select pins. See Truth Table . LVTTTL/CMOS logic levels. Internal 25 kΩ pull-up resistor. Logic high if left unconnected (divided by 16 mode). Input threshold is $V_{CC}/2$.
6	NC	No connect.
8	/RESET /DISABLE	LVTTTL/CMOS logic levels. Internal 25 kΩ pull-up resistor. Logic high if left unconnected. Apply low to reset the divider (divided by 2, 4, 8, or 16 mode). Also acts as a synchronous disable/enable function. The reset and disable function occurs on the next high-to-low clock input transition. Input threshold is $V_{CC}/2$.
10	V_{REF-AC}	Reference voltage. Equal to $V_{CC} - 1.4V$ (approximately). Used for AC-coupled applications only. Decouple the V_{REF-AC} pin with a 0.01 μF capacitor. See the Input Interface Applications section.
11	V_T	Termination center tap. For CML or LVDS inputs, leave this floating. Otherwise, see the figures within the Input Interface Applications section.
7, 14	V_{CC}	Positive power supply. Bypass with 0.1 μF//0.01 μF low-ESR capacitor.
13	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.

5.0 DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

Single-ended swing is defined as the amplitude of the signal when driven differentially. Differential swing is defined as $IN - \overline{IN}$ (or $Q - \overline{Q}$).

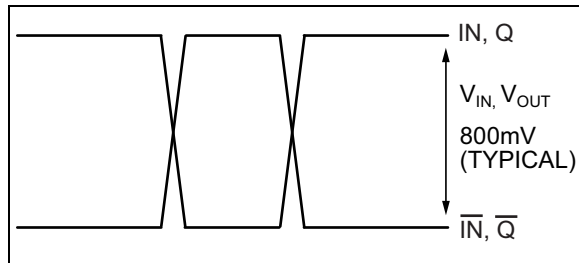


FIGURE 5-1: Single-Ended Swing.

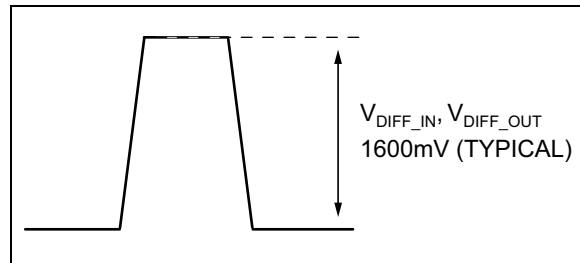


FIGURE 5-2: Differential Swing.

6.0 INPUT BUFFER STRUCTURE

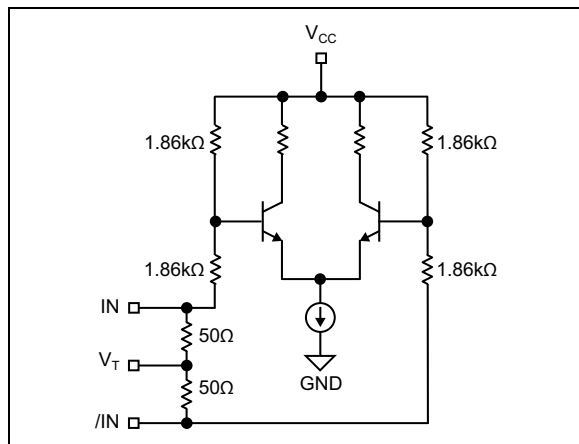


FIGURE 6-1: Simplified Differential Input Stage.

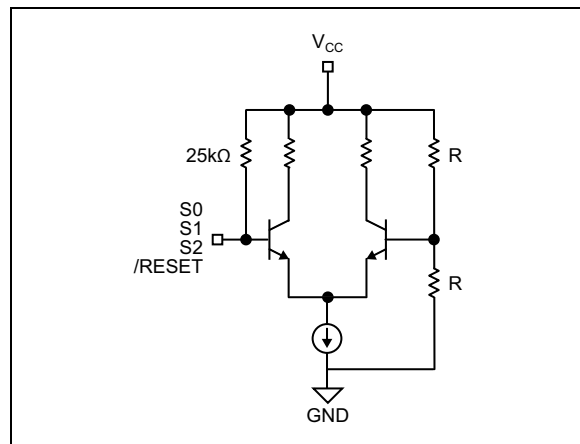


FIGURE 6-2: Simplified LVTTL/CMOS Input Stage.

7.0 INPUT INTERFACE APPLICATIONS

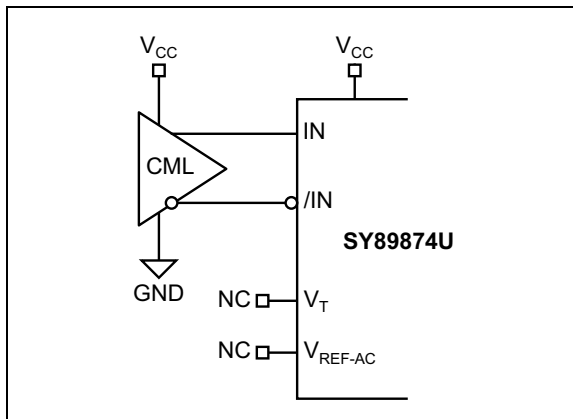


FIGURE 7-1: DC-Coupled CML Input Interface.

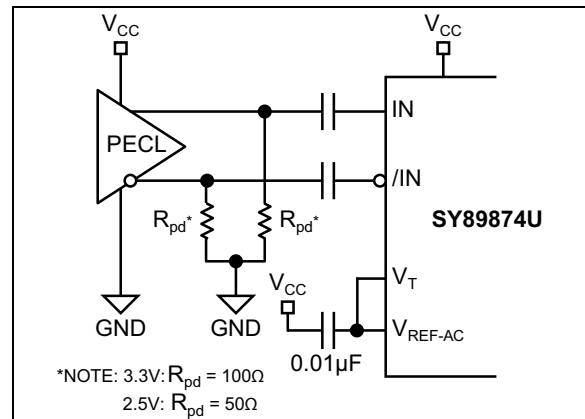


FIGURE 7-4: AC-Coupled PECL Input Interface.

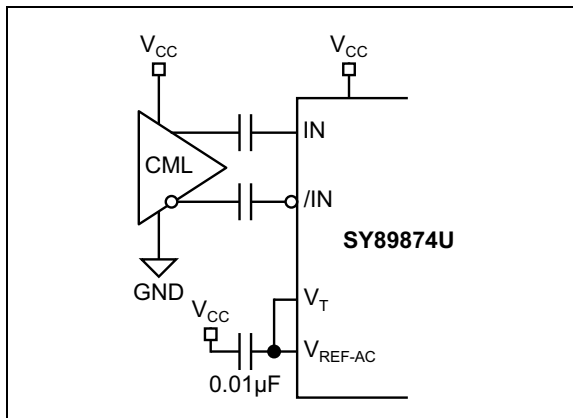


FIGURE 7-2: AC-Coupled CML Input Interface.

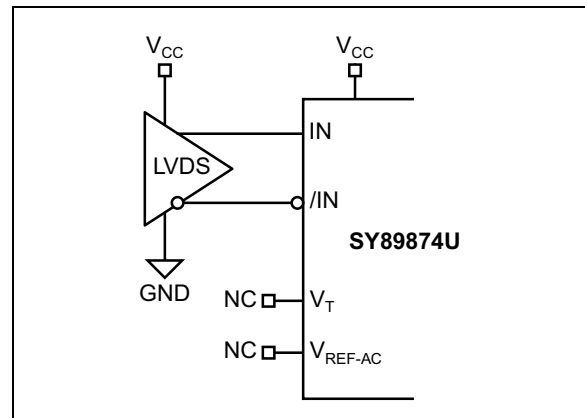


FIGURE 7-5: LVDS Input Interface.

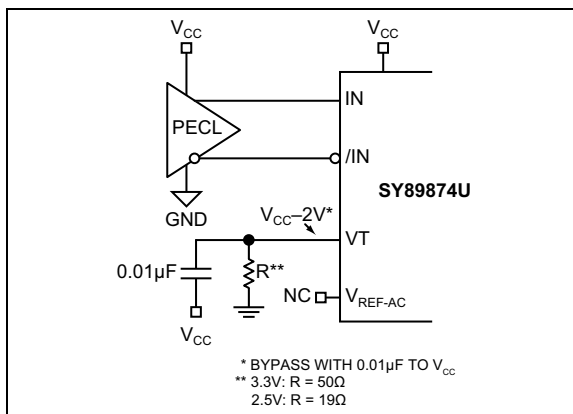


FIGURE 7-3: DC-Coupled PECL Input Interface.

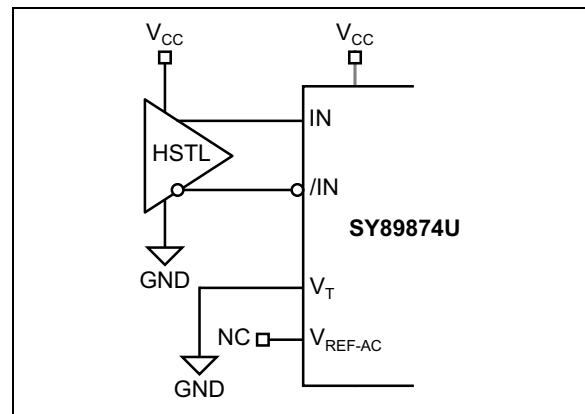


FIGURE 7-6: HSTL Input Interface.

8.0 LVPECL OUTPUT TERMINATION RECOMMENDATIONS

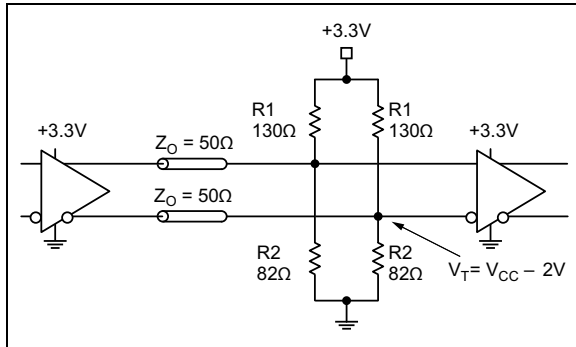


FIGURE 8-1: Parallel Termination Thevenin Equivalent.

For Figure 8-1, note that for +2.5V systems: $R_1 = 250\Omega$, $R_2 = 62.5\Omega$.

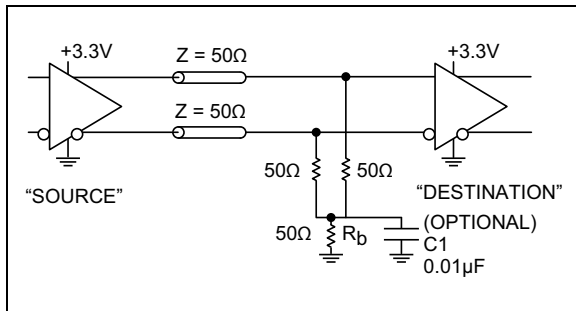


FIGURE 8-2: Three-Resistor "Y" Termination.

For Figure 8-2, note that this is a power-saving alternative to Thevenin termination. Place termination resistors as close to destination inputs as possible. The R_b resistor sets the DC bias voltage, equal to V_T . For +3.3V systems $R_b = 46\Omega$ to 50Ω . For +2.5V systems, $R_b = 39\Omega$. C_1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

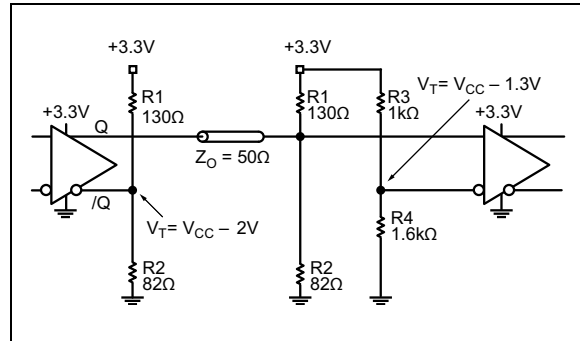


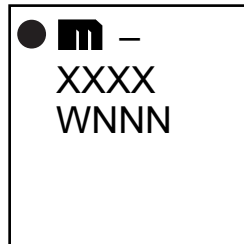
FIGURE 8-3: Terminating Unused I/O.

For Figure 8-3, note that the unused output (/Q) must be terminated to balance the output. For +2.5V systems: $R_1 = 250\Omega$, $R_2 = 62.5\Omega$, $R_3 = 1.25\text{ k}\Omega$, $R_4 = 1.2\text{ k}\Omega$.

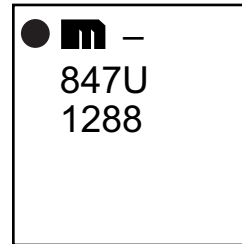
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

16-Lead QFN*

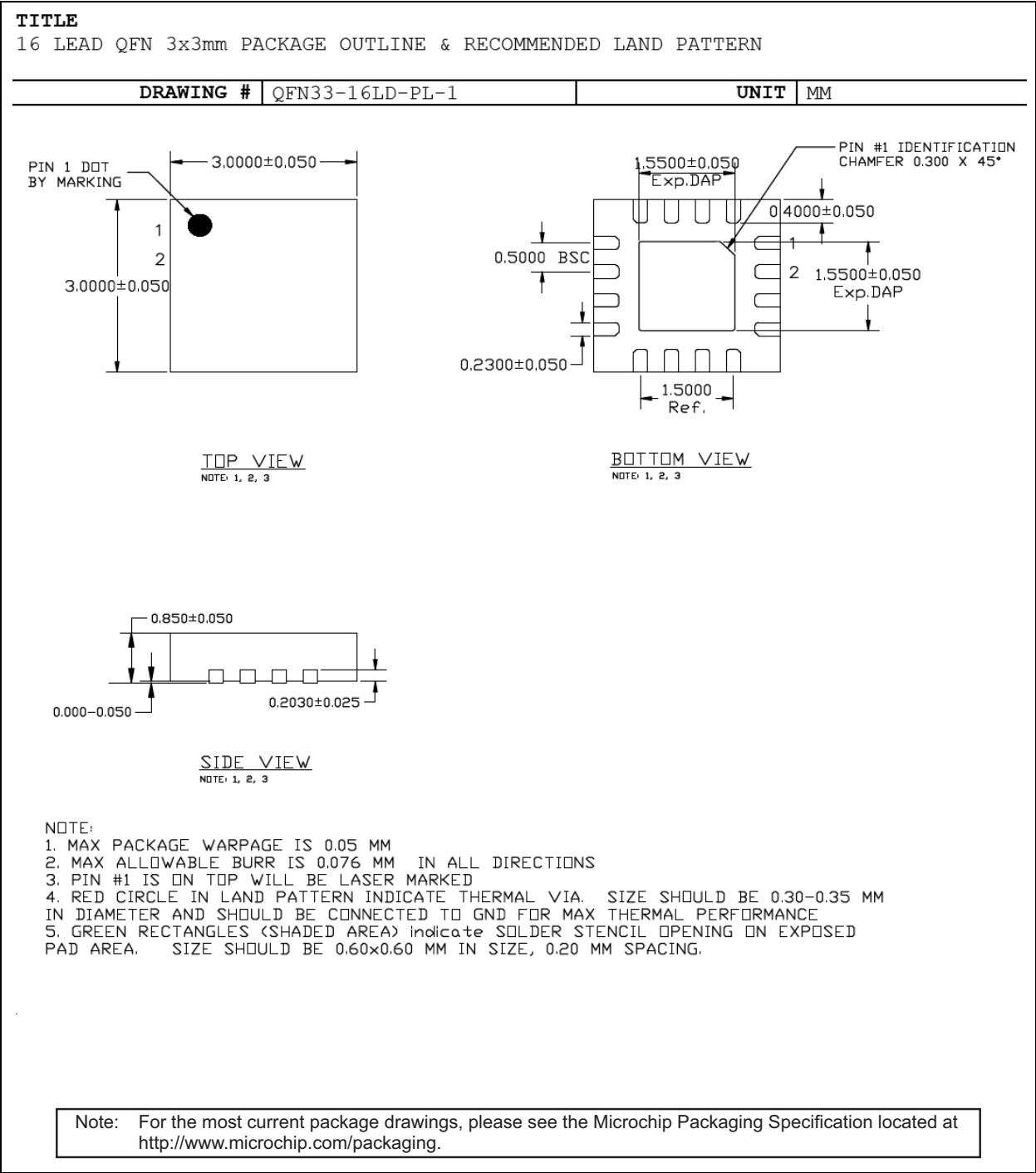


Example



Legend:	XX...X Product code or customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3))
	can be found on the outer packaging for this package.
	•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle
	mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will
	be carried over to the next line, thus limiting the number of available
	characters for customer-specific information. Package may or may not include
	the corporate logo.
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm x 3 mm QFN Package Outline and Recommended Land Pattern

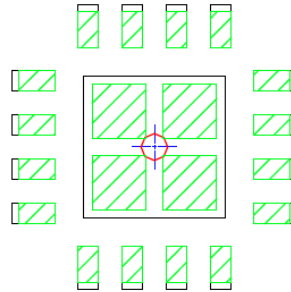


Note: Package meets Level 2 moisture sensitivity classification and is shipped in dry-pack. Exposed pads must be soldered to a ground for proper thermal management.

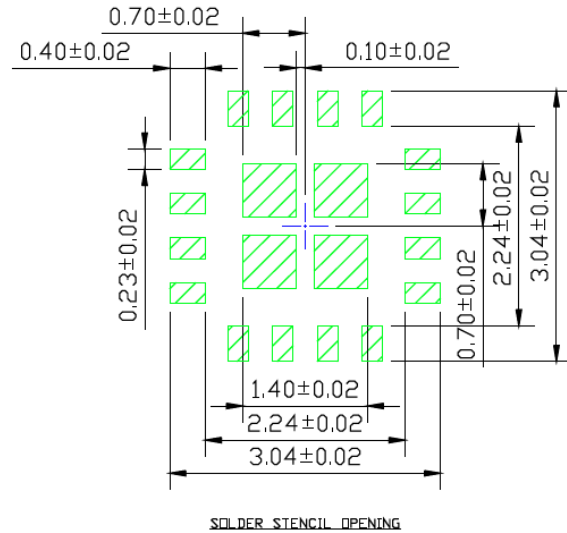
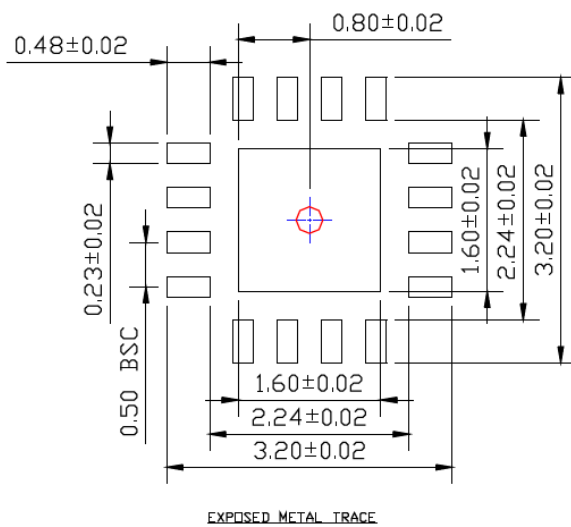
POD-Land Pattern drawing # QFN33-16LD-PL-1

RECOMMENDED LAND PATTERN

NOTE: 4, 5



STACKED-UP



Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document SY89874U to Microchip data sheet template DS20006108A.
- Minor text changes throughout.
- Added information about Additive Phase Jitter in [AC Electrical Characteristics](#) table and [Additive Phase Noise Plot](#) section.

Revision B (November 2018)

- Corrected units of measurement for Additive Phase Jitter in [AC Electrical Characteristics](#) from p_{SRMS} to f_{SRMS} .

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		<u>X</u>	<u>X</u>	<u>X</u>	<u>-XX</u>
Device		Input Voltage	Package	Temperature Range	Tape and Reel
Device:	SY89874:	2.5GHz, Any Differential In-to-LVPECL, Programmable Clock Divider/Fanout Buffer with Internal Termination			
Input Voltage:	U	=	2.5V/3.3V		
Package:	M	=	3 mm x 3 mm QFN-16		
Temperature Range:	G	=	-40°C to 85°C (NiPdAu Lead-Free)		
Special Processing:	<blank>	=	100/Tube		
	TR	=	1,000/Reel		

Examples:

a) SY89874UMG: SY89874, 2.5V/3.3V Input Voltage, 3 mm x 3 mm 16-Lead QFN, -40°C to +85°C Temperature Range, 100/Tube

b) SY89874UMG-TR: SY89874, 2.5V/3.3V Input Voltage, 3 mm x 3 mm 16-Lead QFN, -40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KeeLoq, Kleeer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KleeerNet, KleeerNet logo, memBrain, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2018, Microchip Technology Incorporated, All Rights Reserved.
ISBN: 978-1-5224-3886-1

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820