Image Scaler IP User Guide

Introduction (Ask a Question)

The Image Scaler provides both down-scaling and up-scaling ability to resize an image. The implementation uses a bilinear interpolation algorithm to resize the image. The input and output resolutions must be specified using the input ports that define the corresponding resolution.

Image Scaler Summary

Core Version	This document applies to Image Scaler v4.3.
Supported Device Families	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v12.0 or later releases.
Supported Interfaces	• Native Video Interface • AXI4 Lite interface • AXI4 Stream Video Interface
Licensing	Image Scaler IP clear RTL is license locked, and the encrypted RTL is available for free. **Encrypted**: Complete RTL code is provided for the core, allowing the core to be instantiated with the SmartDesign tool. Simulation, Synthesis and Layout are performed within Libero System-on-Chip (SoC). The RTL code for the core is encrypted. **RTL**: Complete RTL source code is provided for the core.
Installation Instructions	Image Scaler must be installed to the IP Catalog automatically through the IP Catalog update function. Alternatively, Image Scaler is manually downloaded from the catalog. Once the IP core is installed, it is configured, generated and instantiated for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information for Image Scaler is listed in Resource Utilization.

Key Features (Ask a Question)

The Image Scaler IP has the following key features:

- Supports Scale up and Down any Image or Video
- Supports AXI4 Stream Video and AXI4-Lite Configuration Interface
- Supports Programmable Image Dimensions (Through Input and Output Resolutions)
- Supports only RGB444
- Supports only Bi-linear Scaling

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1. Overview (Ask a Question)

The Image Scaler operates in up-scaling mode when either the horizontal or vertical output image resolution is greater than or equal to the respective horizontal or vertical input image resolution.

The horizontal and vertical scale factors must be provided as inputs to the IP that are calculated based on the horizontal and vertical resolution inputs to the IP using the following equations:

$$SCALE\_FACTOR\_HORZ\_I = \frac{(HORZ\_RES\_IN\_I) - 1}{HORZ\_RES\_OUT\_I} * 1024$$

$$SCALE\_FACTOR\_VERT\_I = \frac{(VERT\_RES\_IN\_I) - 1}{VERT\_RES\_OUT\_I} * 1024$$

The image scaler accepts the input image pixel data in RGB 8-bit format at the pixel clock rate. When the scaler IP is operating in downscaler only mode, the OUT_VIDEO_CLK_I is connected to the IN_VIDEO_CLK_I. When the scaler IP is operating in upscaler mode, the out video clock frequency should be higher than the input clock period frequency as per the following equation:

$$OUT\_VIDEO\_CLK\_PER < \frac{(INP\_CLK\_PER * HORZ\_RES\_IN\_I) + ROW\_BLANK\_PER}{\left(HORZ\_RES\_OUT\_I + 4\right) * CEILING\left(\frac{VERT\_RES\_OUT\_I}{VERT\_RES\_IN\_I - 1}\right)}$$

where,

- SCALE_FACTOR_HORZ_I represents the image scaling in the horizontal resolution
- SCALE_FACTOR_VERT_I represents the image scaling in the vertical resolution
- HORZ_RES_IN_I represents the horizontal resolution of the input image
- HORZ_RES_OUT_I represents the horizontal resolution of the output image
- VERT_RES_IN_I represents the vertical resolution of the input image
- VERT_RES_OUT_I represents the vertical resolution of the output image
- OUT_VIDEO_CLK_PER represents the clock period for the out video clock (OUT_VIDEO_CLK_I)
- INP_CLK_PER represents the clock period for the input image
- ROW_BLANK_PER represents the row blanking period for the input image

The IP scaling ratio can be changed dynamically by changing the resolution inputs and the scale factors. It is recommended to modify the scaling ratio only during frame blanking period. When the IP is dynamically switched between down scaling and upscaling, the IP clock must be calculated based on the maximum intended upscaling ratio.

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2. Interface (Ask a Question)

This section describes the ports and configuration parameters of the Image Scaler IP.

2.1 Configuration Parameters (Ask a Question)

The following table lists the configuration parameters used in the hardware implementation of the Image Scaler. These parameters are generic and can be varied based on the application requirement.

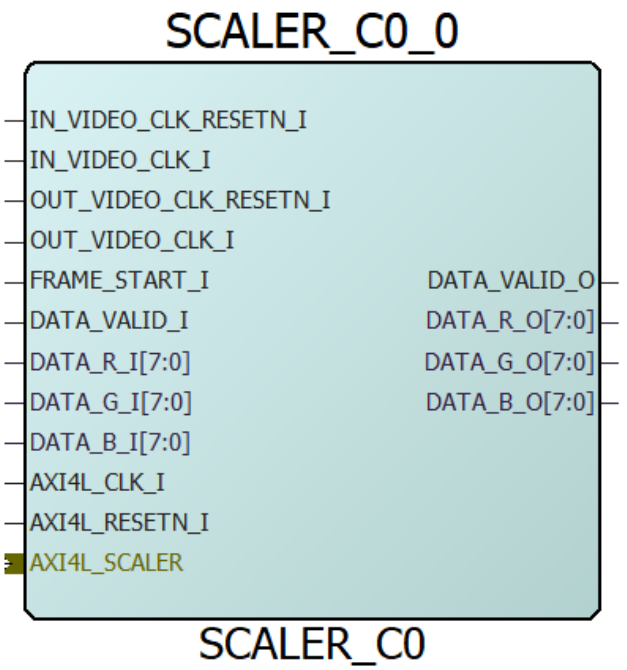
Table 2-1. Configuration Parameters

Parameter Name	Description
Data Width	Represents bit width of the input and output data The current version is only tested to support 8-bit input and output data.
Input FIFO Awidth	Represents depth of the input FIFO used to store one row of the input image 2^(Input FIFO Awidth) must be sufficient to store one entire row of the input image.
Output FIFO Awidth	Represents depth of the output FIFO which can be used to store one row of the output image. For Example: Output FIFO Awidth of 10 can store up to 1023 (2^10 - 1) resolution of the output image.
AXI4 Stream Interface	It can be enabled or disabled as per the requirement.

2.2 Inputs and Outputs (Ask a Question)

The following figure shows the block diagram of Image Scaler IP.

Figure 2-1. Image Scaler IP



The following table lists the input and output ports of the Image Scaler IP.

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Table 2-2. Input and Output Ports for Native Interface

Port Name	Direction	Width (bits)	Description
IN_VIDEO_CLK_I	Input	1	System clock This must be the same as the pixel clock used in Equation 3.
IN_VIDEO_CLK_RESETN_I	Input	1	Active-low asynchronous reset in IN_VIDEO_CLK_I domain.
OUT_VIDEO_CLK_I	Input	1	Scaler IP clock It is the same clock as IN_VIDEO_CLK_I, if the IP is only used for down-scaling. A separate clock that satisfies Equation 3 is needed for up-scaling configuration.
OUT_VIDEO_CLK_RESETN_I	Input	1	Active-low asynchronous reset signal in OUT_VIDEO_CLK_I domain
FRAME_START_I	Input	1	Frame start signal indicating the start of the frame in IN_VIDEO_CLK_I domain. This signal is expected to be 8 cycle wide for it to be sampled across other clock domains within this IP.
DATA_VALID_I	Input	1	Input data valid signal This signal must be asserted when the data is valid.
DATA_R_I	Input	8/10/12/16	Red data component of the input video
DATA_G_I	Input	8/10/12/16	Green data component of the input video
DATA_B_I	Input	8/10/12/16	Blue data component of the input video
AXI4L_CLK_I	Input	1	AXI4 Lite clock
AXI4L_RESETN_I	Input	1	AXI4 Lite clock Active-low reset signal
AXI4L_SCALER	Input	<AXI4 Lite Interface>	AXI4 Lite interface to access control registers for the IP.
DATA_VALID_O	Output	1	This signal is high, indicating valid video data at the output interface.
DATA_R_O	Output	8/10/12/16	Red component of the output video data
DATA_G_O	Output	8/10/12/16	Green component of the output video data
DATA_B_O	Output	8/10/12/16	Blue component of the output video data

The following table lists the input and output ports for AXI4 stream video interface.

Table 2-3. Input and Output Ports for AXI4 Stream Video Interface

Port Name	Type	Width (bits)	Description
IN_VIDEO_CLK_RESETN_I	Input	1	Active-low asynchronous reset signal in IN_VIDEO_CLK_I domain.
IN_VIDEO_CLK_I	Input	1	Input clock for streaming incoming video data

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.....continued			
Port Name	**Type**	**Width (bits)**	**Description**
TREADY_O	Output	1	Output target ready
TDATA_I	Input	Based on the data width parameter in the configurator, it can be set to 24/30/36/48.	Input Video Data
TVALID_I	Input	1	Input Video Valid
TUSER_I	Input	4	Bit 0 = Frame End signal for incoming video data Bit 1 = unused Bit 2 = unused Bit 3 = unused
TDATA_O	Output	Based on the data width parameter in the configurator, it can be set to 24/30/36/48.	Output Video Data
TVALID_O	Output	1	Output Video Valid
TUSER_O	Output	4	Bit 0 = Frame End signal of the video data Bit 1 = unused Bit 2 = unused Bit 3 = unused
TLAST_O	Output	1	Indicates the data valid boundary of the incoming video data.
TSTRB_O	Output	Based on the data width parameter in the configurator, it can be set to 1 or 2 bits.	It is always high, indicating valid Red, Green and Blue components on the data bus.
TKEEP_O	Output	Based on the data width parameter in the configurator, it can be set to 1 or 2 bits.	It always indicates high processing of Red, Green and Blue components of the data stream.

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3. Register Map and Descriptions (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	IP_VER	7:0	IP VERSION[7:0]							
		15:8	IP VERSION[15:8]							
		23:16	IP VERSION[23:16]							
		31:24								
0x04	Control_Register	7:0							IP RESET	ENABLE/ DISABLE
		15:8								
		23:16								
		31:24								
0x08	Input_Horizontal_Resolution	7:0	INPUT_HORIZONTAL_RESOLUTION[7:0]							
		15:8				INPUT_HORIZONTAL_RESOLUTION[12:8]				
		23:16								
		31:24								
0x0C	Input_Vertical_Resolution	7:0	INPUT_VERTICAL_RESOLUTION[7:0]							
		15:8				INPUT_VERTICAL_RESOLUTION[12:8]				
		23:16								
		31:24								
0x10	Output_Horizontal_Resolution	7:0	OUTPUT_HORIZONTAL_RESOLUTION[7:0]							
		15:8				OUTPUT_HORIZONTAL_RESOLUTION[12:8]				
		23:16								
		31:24								
0x14	Output_Vertical_Resolution	7:0	OUTPUT_VERTICAL_RESOLUTION[7:0]							
		15:8				OUTPUT_VERTICAL_RESOLUTION[12:8]				
		23:16								
		31:24								
0x18	Scale_Factor_Horizontal_Resolution	7:0	SCALE_FACTOR_HORIZONTAL_RESOLUTION[7:0]							
		15:8	SCALE_FACTOR_HORIZONTAL_RESOLUTION[15:8]							
		23:16								
		31:24								
0x1C	Scale_Factor_Vertical_Resolution	7:0	SCALE_FACTOR_VERTICAL_RESOLUTION[7:0]							
		15:8	SCALE_FACTOR_VERTICAL_RESOLUTION[15:8]							
		23:16								
		31:24								

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3.1 IP_VER (Ask a Question)

Name: IP_VER
Offset: 0x000
Reset: 0x40300
Property: Read-only

Current Image Scaler IP version number

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IP VERSION[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	0	0

Bit	15	14	13	12	11	10	9	8
	IP VERSION[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	1	1

Bit	7	6	5	4	3	2	1	0
	IP VERSION[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IP VERSION[23:0] Current Image Scaler IP version number

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3.2 Control_Register (Ask a Question)

Name: Control_Register
Offset: 0x004
Reset: 0x1
Property: Read-Write

Register to Enable/Disable/Reset the Image Scaler IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							IP RESET	ENABLE/ DISABLE
Access							W	R/W
Reset							0	1

Bit 1 – IP RESET To reset the IP core value of '1' needs to be written once to this bit. It does not hold the written data value.

Bit 0 – ENABLE/DISABLE This bit controls Enabling or Disabling the IP.
The following table lists the IP control register value with its functionality.

IP Control Register Value	Functionality
0	Disable
1	Enable

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3.3 Input_Horizontal_Resolution (Ask a Question)

Name: Input_Horizontal_Resolution
Offset: 0x008
Reset: 0x780
Property: Write-only

Horizontal Resolution input to the Image Scaler IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				INPUT_HORIZONTAL_RESOLUTION[12:8]				
Access				W	W	W	W	W
Reset				0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	INPUT_HORIZONTAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	1	0	0	0	0	0	0	0

Bits 12:0 – INPUT_HORIZONTAL_RESOLUTION[12:0] Horizontal Resolution input to the Image Scaler IP

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3.4 Input_Vertical_Resolution (Ask a Question)

Name: Input_Vertical_Resolution
Offset: 0x00C
Reset: 0x438
Property: Write-only

Vertical Resolution input to the Image Scaler IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				INPUT_VERTICAL_RESOLUTION[12:8]				
Access				W	W	W	W	W
Reset				0	0	1	0	0

Bit	7	6	5	4	3	2	1	0
	INPUT_VERTICAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	1	1	1	0	0	0

Bits 12:0 – INPUT_VERTICAL_RESOLUTION[12:0] Vertical Resolution input to the Image Scaler IP

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3.5 Output_Horizontal_Resolution (Ask a Question)

Name: Output_Horizontal_Resolution
Offset: 0x010
Reset: 0x780
Property: Write-only

Horizontal Resolution of the output of the Image Scaler IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				OUTPUT_HORIZONTAL_RESOLUTION[12:8]				
Access				W	W	W	W	W
Reset				0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	OUTPUT_HORIZONTAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	1	0	0	0	0	0	0	0

Bits 12:0 – OUTPUT_HORIZONTAL_RESOLUTION[12:0] Horizontal Resolution of the output of the Image Scaler IP

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3.6 Output_Vertical_Resolution (Ask a Question)

Name: Output_Vertical_Resolution
Offset: 0x014
Reset: 0x430
Property: Write-only

Vertical Resolution of the output of the Image Scaler IP

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				OUTPUT_VERTICAL_RESOLUTION[12:8]				
Access				W	W	W	W	W
Reset				0	0	1	0	0

Bit	7	6	5	4	3	2	1	0
	OUTPUT_VERTICAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	1	1	0	0	0	0

Bits 12:0 – OUTPUT_VERTICAL_RESOLUTION[12:0] Vertical Resolution of the output of the Image Scaler IP

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3.7 Scale_Factor_Horizontal_Resolution (Ask a Question)

Name: Scale_Factor_Horizontal_Resolution
Offset: 0x018
Reset: 0x3ff
Property: Write-only

Horizontal resolution scaling factor

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	SCALE_FACTOR_HORIZONTAL_RESOLUTION[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	1	1

Bit	7	6	5	4	3	2	1	0
	SCALE_FACTOR_HORIZONTAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – SCALE_FACTOR_HORIZONTAL_RESOLUTION[15:0] Horizontal Resolution scaling factor

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3.8 Scale_Factor_Vertical_Resolution (Ask a Question)

Name: Scale_Factor_Vertical_Resolution
Offset: 0x01C
Reset: 0x406
Property: Write-only

Vertical resolution scaling factor

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	SCALE_FACTOR_VERTICAL_RESOLUTION[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	1	0	0

Bit	7	6	5	4	3	2	1	0
	SCALE_FACTOR_VERTICAL_RESOLUTION[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	1	1	0

Bits 15:0 – SCALE_FACTOR_VERTICAL_RESOLUTION[15:0] Vertical Resolution scaling factor

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4. Testbench (Ask a Question)

A testbench is available to verify the functionality of the Image Scaler IP. To ensure that the testbench works correctly, configure the parameters listed in the following table at the beginning of the testbench file.

Table 4-1. Testbench Configuration Parameters

Name	Description
HORZ_RES_IN	Horizontal resolution of the input image
VERT_RES_IN	Vertical resolution of the input image
HORZ_RES_OUT	Horizontal resolution of the scaled output image
VERT_RES_OUT	Vertical resolution of the scaled output image
SCALE_FACTOR_HORZ_I	Scale factor in horizontal direction - Formula and example provided as comment.
SCALE_FACTOR_VERT_I	Scale factor in vertical direction - Formula and example provided as comment.
SYSCLKPERIOD	Pixel clock period of the input image
IPCLKPERIOD	Desired frequency for the Scaler IP It can reuse SYSCLKPERIOD for down-scaling. It must satisfy Equation 3 for up-scaling.
BLANK_PER	Blanking period between consecutive rows for input image
ACLK_PERIOD	Clock period to be used for AXI4 Lite interface
INPUT_IMG_FILE_NAME	Location and name of the input image file
OUTPUT_IMG_FILE_NAME	Location and name of the generated scaled image file

Before running the simulation, generate the Image Scaler instance with sufficient input and output FIFO depth. Ensure that the Input FIFO Awidth, Output FIFO Awidth values provided in the configurator GUI are correct.

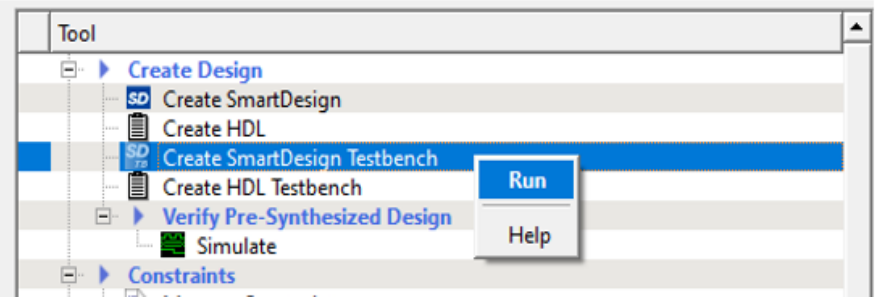
The packaged testbench upscales an input image with a 960 x 540 resolution to produce an output image with a 1280 x 720 resolution.

Important: Testbench works only in the native video interface.

To simulate the core using the testbench, perform the following steps:

1. In the **Design Flow** window, expand **Create Design**, right-click **Create SmartDesign Testbench**, and then click **Run** as shown in the following figure.

Figure 4-1. Create SmartDesign Testbench



2. Enter a name for the SmartDesign Testbench and click **OK**. The SmartDesign testbench is created, and a canvas appears to the right of the Design Flow pane.

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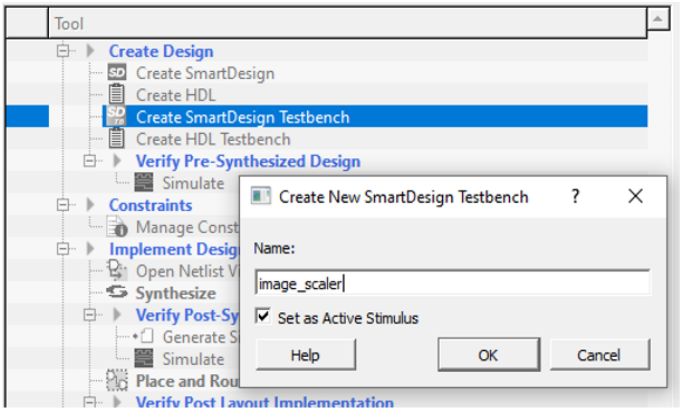
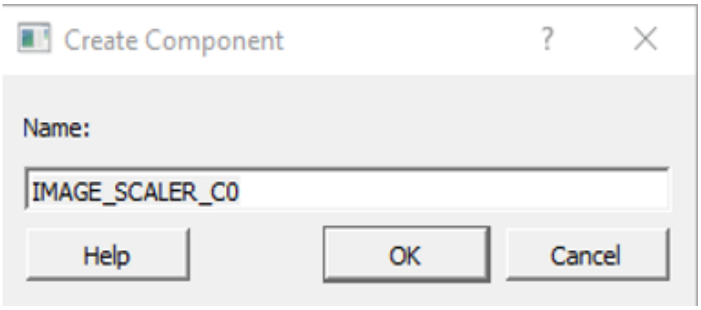
Figure 4-2. SmartDesign Testbench Name



3. In the **Libero SoC Catalog** (**View** > **Windows** > **Catalog**), expand **Solutions-Video**, and then drag the **Scaler IP** core onto the **SmartDesign Testbench** canvas.
4. Select the default component name and click **OK**.

Figure 4-3. Create Component



5. In the **Scaler Configurator GUI** window, update the Input FIFO Awidth to 11 and the Output FIFO Awidth to 10, then click **OK**.

Figure 4-4. Scaler Configurator—Configuration Tab

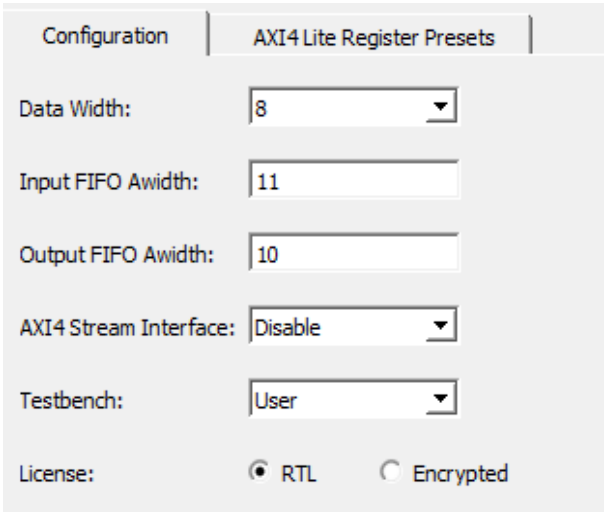


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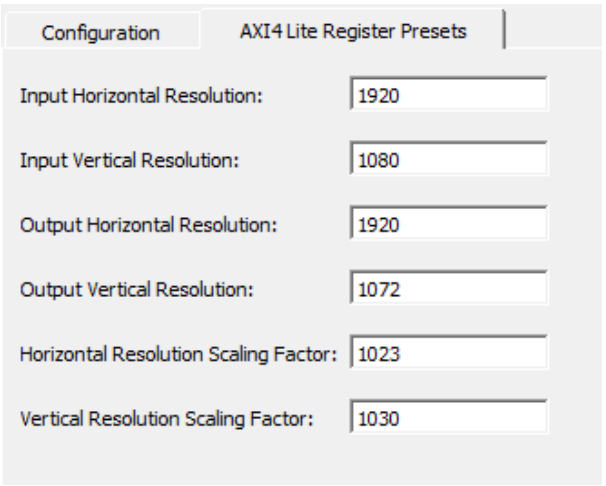
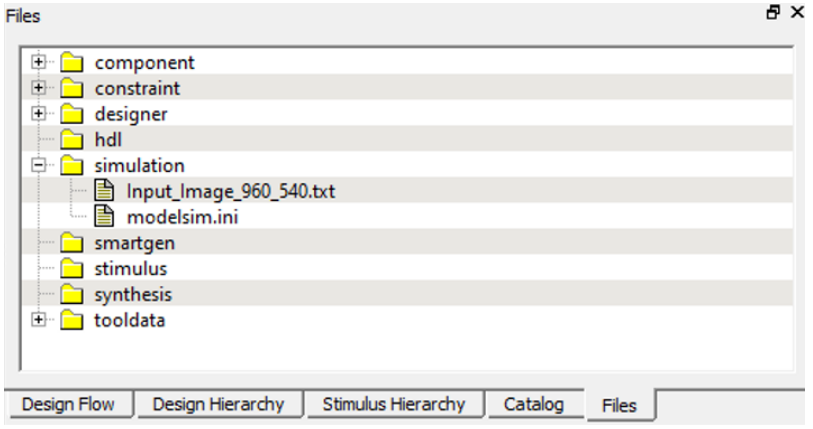
Figure 4-5. Scaler Configurator—AXI4 Lite Register Presets Tab



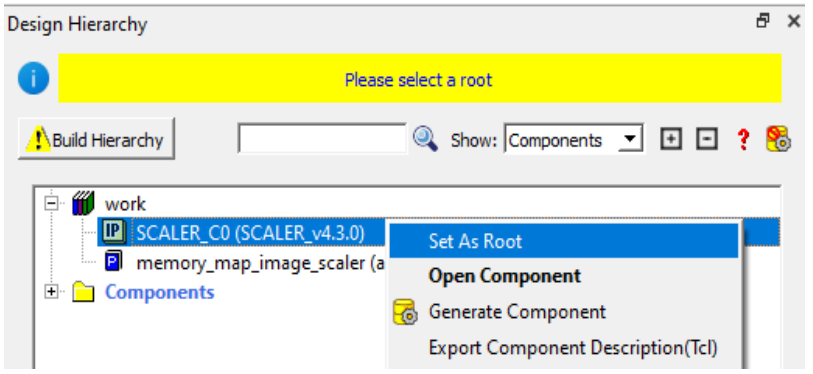
6. On the **Files** tab, click **Simulation** > **Import Files**.
7. Import the Input Image file `Input_Image_960_540.txt` from the following path: `\<Project_name>\component\Microchip\SolutionCore\IMAGE_SCALER\IP_VERSION_NUMBER\Stimulus`. To import a different file, browse to the folder that contains the required file and click **Open**. The imported file is listed under simulation, as shown in the following figure.

Figure 4-6. Input Image File



8. In the **Design Hierarchy** tab, click **Build Hierarchy**, then right-click on **SCALER_C0** and select **Set As Root**.

Figure 4-7. Design Hierarchy



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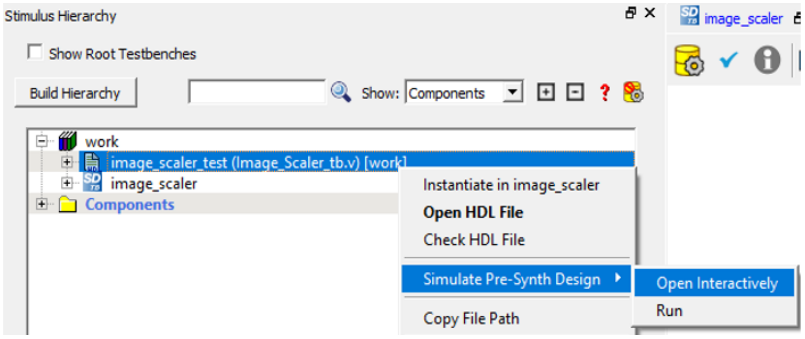
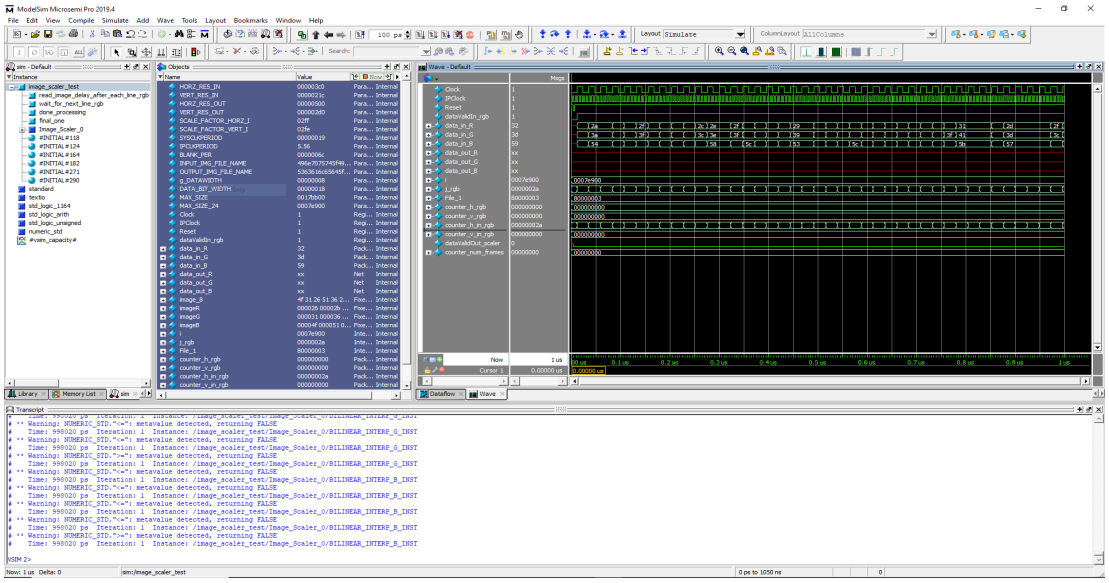
9. In the **Stimulus Hierarchy** tab, right-click the `image_scaler_test` testbench file, then hover over **Simulate Pre-Synth Design**, and click **Open Interactively**.

Figure 4-8. Stimulus Hierarchy



The ModelSim® tool appears with the testbench file loaded on to it, as shown in the following figure.

Figure 4-9. ModelSim Tool



If the simulation is interrupted because of the runtime limit in the `.DO` file, use the run `-all` command to complete the simulation. By default, the output image file is placed in the files or simulation directory and uses the `OUTPUT_IMG_FILE_NAME`.

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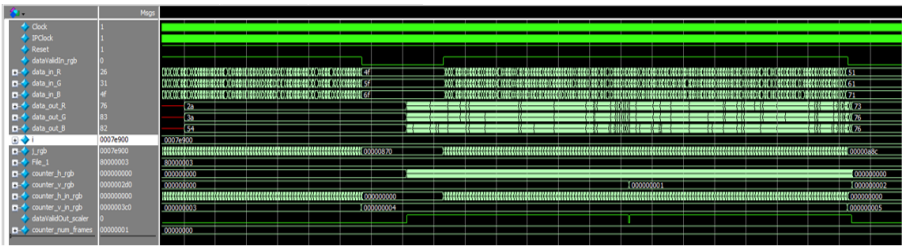
5. Simulation Results (Ask a Question)

This section discusses about timing diagram and output image.

5.1 Timing Diagram (Ask a Question)

The following is the timing diagram for Scaler IP showing video data and control signals for the first two rows of the output image.

Figure 5-1. Video Data and Control Signals



The following table lists the timing diagram configuration parameters.

Table 5-1. Timing Diagram Configuration Parameters

Name	Description
data_in_(R, G, B)	Input image pixel data
data_out_(R, G, B)	Scaled output image pixel data
counter_v_rgb	Counter tracking the number of scaled output image rows
counter_h_rgb	Counter tracking the number of scaled output image pixels per rows
dataValidOut_scaler	Data valid signal generated by Scaler IP
counter_num_frames	Number of input image frames processed

5.2 Output Image (Ask a Question)

The packaged testbench will upscale an inputimage with a 960 x 540 resolution to produce an output image with a 1280 x 720 resolution. The scaled output image is shown in the following figure.

Figure 5-2. Scaled Output

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6. Resource Utilization (Ask a Question)

Image Scaling is implemented on PolarFire® FPGA (MPFS250TS -1FCG1152I package). The following tables list the resource utilization report for the configuration parameters.

Table 6-1. Configuration Parameter and their Values

Parameter	Value
Data Width	8
Input FIFO Awidth	11
Output FIFO Awidth	10
AXI4 Stream Interface	Disable

Table 6-2. Resource Utilization

Resource	Usage
Fabric 4LUT	970
Fabric DFF	726
Interface 4LUT	540
Interface DFF	540
LSRAM (20K)	12
Math (18x18)	3
Chip Globals	3

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7. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
B	01/2025	The following is the list of changes in revision B of the document: • Updated core version to "v4.3" in Summary in the Introduction section. • Updated Figure 2-1, Table 2-2 and Table 2-3 in the Inputs and Outputs section. • Added Figure 4-4, Figure 4-5 and updated Figure 4-7 in the Testbench section. • Updated part number to "MPFS250TS -1FCG1152I" from "MPF100T -1FCG484" and Table 6-2 in Resource Utilization section.
A	01/2024	Initial revision.

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