Automotive Silicon Errata and Data Sheet Clarifications

ATtiny212/214/412/414 Automotive

The ATtiny212/214/412/414 Automotive devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002229), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny212/214/412/414 Automotive devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002229) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- \- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. B[1]	Rev. C
Device	2.2.1. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X	X
	2.2.2. Write Operation Lost if Consecutive Writes to Specific Address Spaces	X	X
ADC	2.3.1. One Extra Measurement Performed After Disabling ADC Free-Running Mode	X	X
	2.3.2. ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X	X
	2.3.3. Pending Event Stuck When Disabling the ADC	X	X
CCL	2.4.1. Connecting LUTs in Linked Mode Requires OUTEN Set to '1'	X	X
	2.4.2. D-latch is Not Functional	X	X
	2.4.3. The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X
NVMCTRL	2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register	X	X
PORTMUX	2.6.1. Selecting Alternative Output Pin for TCA0 Waveform Output 0-2 also Changes Waveform Output 3-5	X	X
RTC	2.7.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler Counter	X	X
	2.7.2. Disabling the RTC Stops the PIT	X	X
TCA	2.8.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X
TCB	2.9.1. Minimum Event Duration Must Exceed the Selected Clock Period	X	X
	2.9.2. The TCA Restart Command Does Not Force a Restart of TCB	X	X
	2.9.3. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X	X
TCD	2.10.1. Asynchronous Input Events Not Working When TCD Counter Prescaler is Used	X	X
	2.10.2. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is '0' or Dual Slope Mode is Used	X	X
USART	2.11.1. TXD Pin Override Not Released When Disabling the Transmitter	X	X
	2.11.2. Full Range Duty Cycle Not Supported When Validating LIN Sync Field	X	X
	2.11.3. Frame Error on a Previous Message May Cause False Start Bit Detection	X	X
	2.11.4. Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to '1' when using the OSC20M oscillator as the Main Clock source.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.2.2 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address > = 64 followed by an ST/STD instruction to address < 64 or SLPCTRL.CTRLA register will cause loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64, or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3 ADC - Analog-to-Digital Converter

2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.2 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work Around

If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.3.3 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around

Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4 CCL - Configurable Custom Logic

2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work Around

Use an event channel to link the LUTs, or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.4.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

The CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0') to reconfigure a LUT. Writing ENABLE to '0' will disable all the LUTs and affect the LUTs not under reconfiguration.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.5 NVMCTRL - Nonvolatile Memory Controller

2.5.1 Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the NVMCTRL.CTRLA reset value will not be '0x00'. Even reserved bits can be read as '1' after Reset.

Work Around

Ignore the initial value.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.6 PORTMUX - Port Multiplexer

2.6.1 Selecting Alternative Output Pin for TCA0 Waveform Output 0-2 also Changes Waveform Output 3-5

Selecting the alternative output pin for TCA0 in PORTMUX.CTRLC does not work as described when TCA0 operates in split mode.

- Writing PORTMUX.CTRLC bit 0 to '1' will shift the pin position for both WO0 and WO3
- Writing PORTMUX.CTRLC bit 1 to '1' will shift the pin position for both WO1 and WO4
- Writing PORTMUX.CTRLC bit 2 to '1'will shift the pin position for both WO2 and WO5

PORTMUX.CTRLC[5:3] are non-functional.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

Note: Not applicable to 8-pin devices.

2.7 RTC - Real-Time Counter

2.7.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler Counter

Any write to the RTC.CTRLA register resets the 15-bit prescaler counter. The next count occurs ½ prescaler period after the reset, resulting in a period length of 0.5 to 1.5 times the expected period, depending on when the reset occurs.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.7.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work Around

Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.8 TCA - Timer/Counter A

2.8.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.9 TCB - Timer/Counter B

2.9.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement*.

Work Around

Ensure that the high/low period of input events is equal to or longer than the selected clock source (CLKSEL in TCBn.CTRLA) period.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.9.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force restarting the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.9.3 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB operates in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.10 TCD - Timer/Counter D

2.10.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used

When configuring the TCD to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0' events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.10.2 Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is '0' or Dual Slope Mode is Used

Halting TCD and waiting for software restart (INPUTMODE in TCDn.INPUTCTRLA is '0x7') does not work if compare value A is 0 (CMPASET in TCDn.CMPASET is '0x0') or Dual Slope mode is used (WGMODE in TCDn.CTRLB is '0x3').

Work Around

Configure the compare value A (CMPASET in TCDn.CMPASET) to be different from '0' and do not use Dual Slope mode (WGMODE in TCDn.CTRLB is not '0x3').

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.11 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.11.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.11.2 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART validates each bit to be within ±15% instead of the time between falling edges as described in the LIN specification, which allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

Work Around

None.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.11.3 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work Around

Wait for the RXD pin to go high before reading RXDATA by, for instance, polling the bit in PORTn.IN where the RXD pin is located.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

2.11.4 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. B	Rev. C
X	X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002229).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 SLPCTRL - Sleep Controller

3.1.1 Sleep Mode Activity Overview

A clarification has been made to *Table 12-1 Sleep Mode Activity Overview*, where the single table has been split into three separate tables for clarity. Functional changes are shown in **bold**.

Table 12-1a. Sleep Mode Activity Overview for Peripherals

Peripheral	Active in Sleep Mode		
	Idle	Standby	Power-Down
CPU	-	-	-
RTC	X	X(1)	X(2)
WDT	X	X	X
BOD	X	X	X
EVSYS	**X**	**X**	**X**
CCL	X	X(1)	-
ACn			
ADCn			
TCBn			
All other peripherals	X	-	-

Notes:

1. The RUNSTBY bit of the corresponding peripheral must be set to enter the active state.
2. PIT only.

Table 12-1b. Sleep Mode Activity Overview for Clock Sources

Clock Source	Active in Sleep Mode		
	Idle	Standby	Power-Down
Main clock source	X	X(1)	-
RTC clock source	X	X(1)	X(2)
WDT oscillator	X	X	X
BOD oscillator(3)	X	X	X
CCL clock source	**X**	**X(1)**	-

Notes:

1. The RUNSTBY bit of the corresponding peripheral must be set to enter the active state.
2. PIT only.
3. The BOD oscillator runs only in Sampled mode.

Table 12-1c. Sleep Mode Wake-Up Sources

Wake-Up Sources	Active in Sleep Mode		
	Idle	Standby	Power-Down
PORTx Pin interrupt	X	X	X(1)
BOD VLM interrupt	**X**	**X**	**X**
RTC interrupts	X	X(2)	X(3)
TWIn Address Match interrupt	X	X	X
USARTn Start-of-Frame interrupt	-	**X**	-
TCBn interrupts	X	X(2)	-
ADCn interrupts	X	X(2)	-
ACn interrupts	**X**	**X(4)**	-
All other interrupts	X	-	-

Notes:

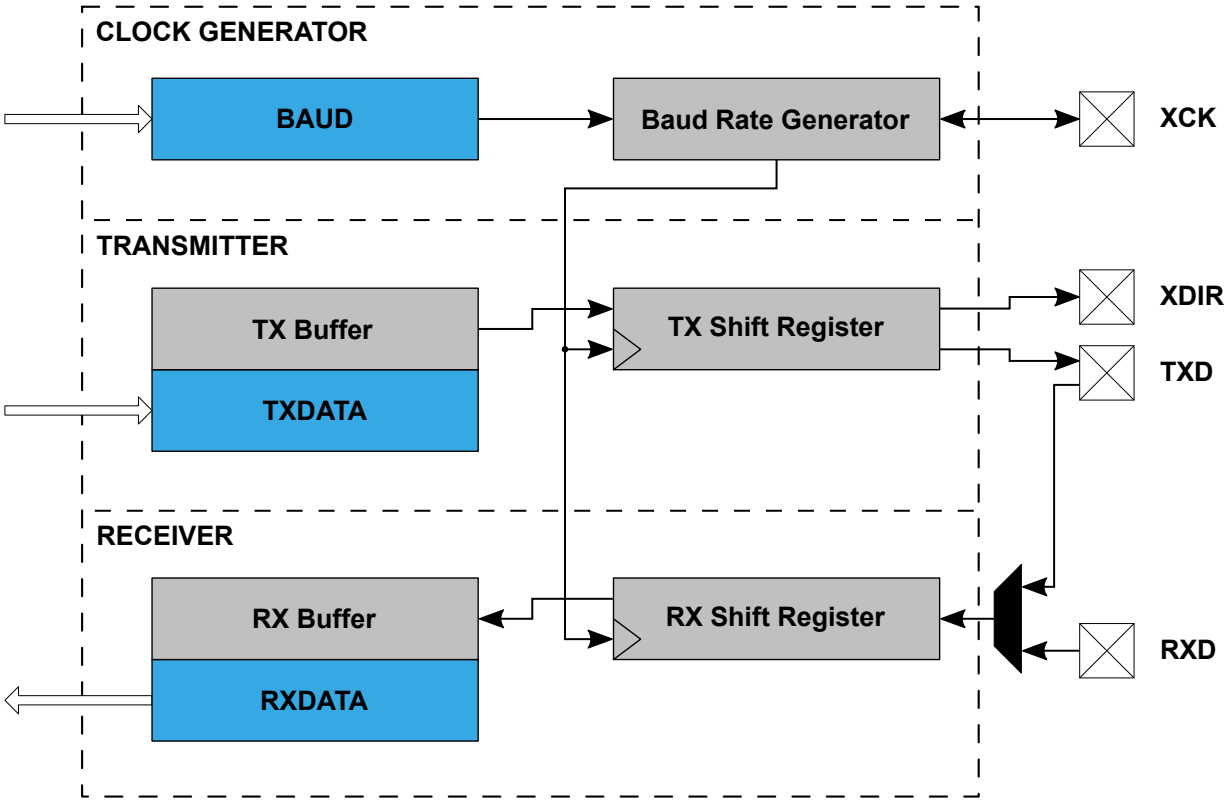
1. **The I/O pin must be configured according to *Asynchronous Sensing Pin Properties* in the PORT section.**
2. The RUNSTBY bit of the corresponding peripheral must be set to enter the active state.
3. PIT only.
4. **When the RUNSTDBY bit is set, the AC will operate without updating its Status register or triggering interrupts. If another peripheral has requested CLK_PER, the AC will use the clock to update the Status register and trigger interrupts.**

3.2 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

3.2.1 TXDATA Buffer

The block diagram is missing that USART TX is double-buffered from *Figure 25-1* in the data sheet. The figure below shows the added **TX Buffer**.

Figure 25-1. USART Block Diagram



The following text is changed in the *Overview* section:

The transmitter consists of a **two-level** write buffer.

The following text is changed in the *Data Transmission* section:

The data transmission is initiated by loading the **Transmit Data (USARTn.TXDATAL and USARTn.TXDATAH)** registers with the data to be sent. The data in the **Transmit Data registers are moved to the TX Buffer** once emptied and then to the Shift register once it is empty and ready to send a new frame.

3.3 SPI - Serial Peripherial Interface

3.3.1 SPI Clock

Clarifications regarding the SPI clock have been made in the *Operation - Slave Mode* and *Operation - Slave Mode - Buffer Mode* sections. Functional changes are shown in **bold**.

26.3.2.2 Slave Mode

In Slave mode, the SPI peripheral receives the SPI clock and Slave Select from a Master. Slave mode supports three operational modes: One Normal mode and two configurations for the Buffered mode. In Slave mode, the control logic will sample the incoming signal on the SCK pin. ~~**To ensure correct sampling of this clock signal, the minimum low and high periods must each be longer than two peripheral clock cycles.**~~

26.3.2.2.2 Buffer Mode

To avoid data collisions, the SPI peripheral can be configured in Buffered mode by writing a '1' to the Buffer Mode Enable (BUFEN) bit in the Control B (SPIn.CTRLB) register. In this mode, the SPI has additional interrupt flags and extra buffers. The extra buffers are shown in *Figure 26-1*. There are two different modes for the Buffer mode, selected with the Buffer mode Wait for Receive (BUFWR) bit. The two different modes are described below with timing diagrams.

Note: When operating as a slave in Buffered mode and the SPI clock is close to maximum frequency, the slave may not be able to set up data in time for the first sample edge during back-to-back transfers. Refer to the *Electrical Characteristics - SPI* section for details.

3.4 ADC - Analog-to-Digital Converter

3.4.1 VREFA

Documentation related to an external reference (VREFA) is removed from the ADC sections listed below, as the ATtiny212/214/412/414 Automotive devices do not have a VREFA pin:

- **Features**
- **Overview**
- **Signal Description**
- **ADC Voltage Reference**
- **REFSEL in ADCn.CTRLC**

The affected ADC sections are listed below, with corrections shown in **bold**:

Features

- 10-Bit Resolution
- 0V to V_{DD} Input Voltage Range
- Multiple Internal ADC Reference Voltages
- ~~**External Reference Input**~~
- Single Conversion Mode
- Interrupt Available on Conversion Complete
- Optional Interrupt on Conversion Results
- Temperature Sensor Input Channel
- Optional Event-Triggered Conversion
- Window Comparator Function for Accurate Monitoring or Defined Thresholds
- Accumulation of up to 64 Samples per Conversion

Overview

The Analog-to-Digital Converter (ADC) peripheral produces 10-bit results. The ADC input can either be internal (e.g., a voltage reference) or external through the analog input pins. The ADC is connected to an analog multiplexer, which allows the selection of multiple single-ended voltage inputs. The single-ended voltage inputs refer to 0V (GND).

The ADC supports sampling in bursts where a configurable number of conversion results are accumulated into a single ADC result (Sample Accumulation). Further, a sample delay can be configured to tune the ADC sampling frequency associated with a single burst. This is to tune the sampling frequency away from any harmonic noise aliased with the ADC sampling frequency (within the burst) from the sampled signal. An automatic sampling delay variation feature can be used to randomize this delay to slightly change the time between samples.

The ADC input signal is fed through a sample-and-hold circuit that ensures that the input voltage to the ADC is held at a constant level during sampling.

The voltage reference can be selected from the internal Voltage Reference (VREF) peripheral or the V_{DD} supply voltage.

~~**The selectable voltage references from the internal Voltage Reference (VREF) peripheral, are V_{DD} supply voltage, or external VREF pin (VREFA).**~~

A window compare feature is available for monitoring the input signal. This feature can be configured to only trigger an interrupt on user-defined thresholds for under, over, inside, or outside a window, with minimum software intervention required.

Signal Description

Pin Name	Type	Description
AIN[n:0]	Analog input	Analog input pin
~~**VREFA**~~	~~**Analog input**~~	~~**External voltage reference pin**~~

ADC Voltage Reference

The reference voltage for the ADC (V_{REF}) controls the conversion range of the ADC. Input voltages that exceed the selected V_{REF} will be converted to the maximum result value of the ADC. For an ideal 10-bit ADC, this value is `0x3FF`.

V_{REF} can be selected by writing the Reference Selection (REFSEL) bits in the Control C (ADCn.CTRLC) register as either V_{DD}~~**, external reference V_{REFA},**~~ or an internal reference from the VREF peripheral. V_{DD} is connected to the ADC through a passive switch.

~~**When using the external reference voltage V_{REFA}, configure ADCnREFSEL[0:2] in the corresponding VREF.CTRLn register to the value that is closest, but above the applied reference voltage. For external references higher than 4.3V, use ADCnREFSEL[0:2] = `0x3`.**~~

The internal reference is generated from an internal band gap reference through an internal amplifier controlled by the Voltage Reference (VREF) peripheral.

REFSEL in ADCn.CTRLC

Bit 5:4 - REFSEL Reference Selection

This bit field selects the voltage reference for ADC.

Value	Name	Description
`0x0`	INTERNAL	Internal reference
`0x1`	VDD	V_{DD}
~~**`0x2`**~~	~~**VREFA**~~	~~**External reference V_{REFA}**~~
`Other`	-	Reserved

3.5 Electrical Characteristics

3.5.1 Power Consumption

A clarification of the power consumption in the Power-Down sleep mode has been made to *Table 36-5*. Functional change is shown in **bold**.

Table 36-5. Power Consumption in Power-Down, Standby and Reset Mode

Mode	Description	Condition		Typ. 25°C	Max. 25°C	Max. 85°C(1)	Max. 125°C	Unit
Standby	Standby power consumption	RTC running at 1.024 kHz from external XOSC32K (C_L = 7.5 pF)	V_{DD} = 3V	0.7	-	-	-	µA
		RTC running at 1.024 kHz from internal OSCULP32K	V_{DD} = 3V	0.7	3.0	6.0	8.0	µA

.....continued								
Mode	Description	Condition		Typ. 25°C	Max. 25°C	Max. 85°C(1)	Max. 125°C	Unit
Power Down/ Standby	Power down/Standby power consumption are the same when all peripherals are stopped	All peripherals stopped	V_{DD} = 3V	0.1	**1.0**	5.0	7.0	µA
Reset	Reset power consumption	Reset line pulled down	V_{DD} = 3V	100	-	-	-	µA

Note:

1. These values are based on characterization and are not covered by production test limits.

3.5.2 I/O Pin Characteristics

A clarification of the maximum value of the pull-up resistor has been made to *Table 36-16* in the *Electrical Characteristics* section. Functional change is shown in **bold**.

Table 36-16. I/O Pin Characteristics (T_A = [-40, 105]°C, V_{DD} = [2.7, 5.5]V Unless Otherwise Stated)

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low-voltage, except $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH}	Input high-voltage, except $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
I_{IH} / I_{IL}	I/O pin input leakage current, except $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 5.5V, pin high	-	< 0.05	-	µA
		V_{DD} = 5.5V, pin low	-	< 0.05	-	
V_{OL}	I/O pin drive strength	V_{DD} = 3.0V, I_{OL} = 7.5 mA	-	-	0.6	V
		V_{DD} = 5.0V, I_{OL} = 15 mA	-	-	1	
V_{OH}	I/O pin drive strength	V_{DD} = 3.0V, I_{OH} = 7.5 mA	2.4	-	-	V
		V_{DD} = 5.0V, I_{OH} = 15 mA	4	-	-	
I_{total}	Maximum combined I/O sink current per pin group(1)		-	-	100	mA
	Maximum combined I/O source current per pin group(1)		-	-	100	
V_{IL2}	Input low-voltage on $\overline{\text{RESET}}$ pin as I/O		-0.2	-	0.3 × V_{DD}	V
V_{IH2}	Input high-voltage on $\overline{\text{RESET}}$ pin as I/O		0.7 × V_{DD}	-	V_{DD} + 0.2V	V
V_{OL2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 3.0V, I_{OL} = 0.25 mA	-	-	0.6	V
		V_{DD} = 5.0V, I_{OL} = 0.5 mA	-	-	1	
V_{OH2}	I/O pin drive strength on $\overline{\text{RESET}}$ pin as I/O	V_{DD} = 3.0V, I_{OH} = 0.25 mA	2.4	-	-	V
		V_{DD} = 5.0V, I_{OH} = 0.5 mA	4	-	-	
t_{RISE}	Rise time	V_{DD} = 3.0V, load = 20 pF	-	2.5	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.5	-	
t_{FALL}	Fall time	V_{DD} = 3.0V, load = 20 pF	-	2.0	-	ns
		V_{DD} = 5.0V, load = 20 pF	-	1.3	-	
C_{PIN}	I/O pin capacitance except TOSC and TWI pins		-	3	-	pF
C_{PIN}	I/O pin capacitance on TOSC pins		-	5.5	-	pF
C_{PIN}	I/O pin capacitance on TWI pins		-	10	-	pF
R_P	Pull-up resistor		20	35	**60**	kΩ

Note:

1. Pin group x (Px[7:0]). The combined continuous sink/source current for all I/O ports should not exceed the limits.

3.5.3 SPI - Timing Characteristics

A clarification regarding the SPI clock has been made in *Table 36-19. SPI - Timing Characteristics*. Functional changes are shown in **bold**.

Table 36-19. SPI - Timing Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	Master	-	-	10	MHz
t_{SCK}	SCK period	Master	100	-	-	ns
t_{SCKW}	SCK high/low width	Master	-	0.5 × t_{SCK}	-	ns
t_{SCKR}	SCK rise time	Master	-	2.7	-	ns
t_{SCKF}	SCK fall time	Master	-	2.7	-	ns
t_{MIS}	MISO setup to SCK	Master	-	10	-	ns
t_{MIH}	MISO hold after SCK	Master	-	10	-	ns
t_{MOS}	MOSI setup to SCK	Master	-	0.5 × t_{SCK}	-	ns
t_{MOH}	MOSI hold after SCK	Master	-	1.0	-	ns
f_{SSCK}	Slave SCK clock frequency	Slave	-	-	5	MHz
t_{SSCK}	Slave SCK Period	Slave	**6 × t_{CLK_PER}**	-	-	ns
t_{SSCKW}	SCK high/low width	Slave	**3 × t_{CLK_PER}**	-	-	ns
t_{SSCKR}	SCK rise time	Slave	-	-	1600	ns
t_{SSCKF}	SCK fall time	Slave	-	-	1600	ns
t_{SIS}	MOSI setup to SCK	Slave	**0.0**	-	-	ns
t_{SIH}	MOSI hold after SCK	Slave	**3 x t_{CLK_PER}**	-	-	ns
t_{SSS}	SS setup to SCK	Slave	**-**	**t_{CLK_PER}**	-	ns
t_{SSH}	SS hold after SCK	Slave	**-**	**t_{CLK_PER}**	-	ns
t_{SOS}	MISO setup to SCK	Slave	-	8.0	-	ns
t_{SOH}	MISO hold after SCK	Slave	-	13	-	ns
t_{SOSS}	MISO setup after SS low	Slave	-	11	-	ns
t_{SOSH}	MISO hold after SS low	Slave	-	8.0	-	ns

3.5.4 Programming Time

A clarification of the *Programming Time* section has been made. *Table 36-34* has been upgraded from *Programming Times* to *Memory Programming Specifications* in the *Electrical Characteristics*. Functional change is shown in **bold**.

Table 36-34. Memory Programming Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Data EEPROM Memory Specifications						
E_{EE}*	**Data EEPROM byte endurance**	**100k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{EE_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
t_{EE_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{EE_EEER}	Full EEPROM Erase (EEER)	—	4	—	ms	
t_{EE_WP}	Page Write (WP)	—	2	—	ms	
t_{EE_ER}	Page Erase (ER)	—	2	—	ms	
t_{EE_ERWP}	Page Erase-Write (ERWP)	—	4	—	ms	
Program Flash Memory Specifications						
E_{FL}*	**Flash memory cell endurance**	**10k**	**—**	**—**	**Erase/Write cycles**	**-40°C ≤ T_A ≤ +105°C**
t_{FL_RET}	**Characteristic retention**	**—**	**40**	**—**	**Year**	**T_A = 55°C**
V_{FL_UPDI}	**V_{DD} for Chip Erase operation**	**$V_{BODLEVEL0}$(1)**	**—**	**V_{DDMAX}**	**V**	
t_{FL_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK_{CPU} cycles	
t_{FL_CHER}	Chip Erase (CHER)	—	4	—	ms	
t_{FL_WP}	Page Write (WP)	—	2	—	ms	
t_{FL_ER}	Page Erase (ER)	—	2	—	ms	
t_{FL_ERWP}	Page Erase/Write (ERWP)	—	4	—	ms	
t_{FL_UPDI}	**Chip Erase with UPDI**	**—**	**50**	**—**	**ms**	**4 KB Flash**
		—	**30**	**—**	**ms**	**2 KB Flash**

† Data found in the "Typ." column is at T_A = 25°C and V_{DD} = 3.0V unless otherwise specified. These parameters are not tested and are for design guidance only.

*** These parameters are characterized but not tested in production.**

Note:

1. **During Chip Erase, the Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON. The erase attempt will fail if the supply voltage V_{DD} is below V_{BOD} for BODLEVEL0.**

3.6 Package Drawings

3.6.1 Package Marking Information

Package marking information is missing in the data sheet. This section contains all package marking information for:

ATtiny212/214/412/414 Automotive devices.

Figure 3-1. Package Marking Information

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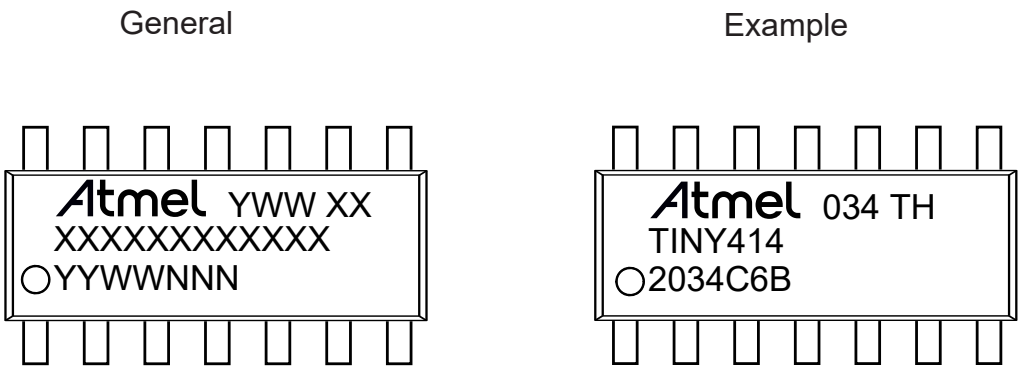
11/02/2020

Legend:	XX...X	Customer-specific information or Microchip part number
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Figure 3-2. 8-Pin SOIC

Figure 3-3. 14-Pin SOIC



4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
D	03/2024	• Document: – Editorial updates • Added new data sheet clarification: – SPI: 3.3.1. SPI Clock – Electrical Characteristics: • 3.5.1. Power Consumption. The Power Consumption in Power-Down (Max 25°C) reduced from 2.0 µA to 1.0 µA. • 3.5.3. SPI - Timing Characteristics • 3.5.4. Programming Time
C	06/2023	• Document: – Editorial updates • Silicon Errata Issues added: – Device: 2.2.2. Write Operation Lost if Consecutive Writes to Specific Address Spaces – NVMCTRL: 2.5.1. Wrong Reset Value of NVMCTRL.CTRLA Register • Silicon Errata Issues updated: – Device: 2.2.1. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values – RTC: 2.7.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler Counter • Added new data sheet clarification: – Electrical Characteristics: 3.5.2. I/O Pin Characteristics

.....continued

Doc. Rev.	Date	Comments
B	04/2021	• Added silicon revision C • Added new errata: – ADC: 2.3.3. Pending Event Stuck When Disabling the ADC – CCL: 2.4.3. The CCL Must be Disabled to Change the Configuration of a Single LUT – TCA: 2.8.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode – TCB: 2.9.3. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode – TCD: • 2.10.1. Asynchronous Input Events Not Working When TCD Counter Prescaler is Used • 2.10.2. Halting TCD and Waiting for SW Restart Does Not Work if Compare Value A is '0' or Dual Slope Mode is Used • Updated RTC erratum: 2.7.1. Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler Counter • Removed Device erratum: *The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)* • Added new data sheet clarification: – SLPCTRL: 3.1.1. Sleep Mode Activity Overview – USART: 3.2.1. TXDATA Buffer – ADC: 3.4.1. VREFA – Package Drawings: 3.6.1. Package Marking Information
A	05/2020	Initial document release

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