PIC18(L)F25/45K22 Rev. A2/A3/A4/A5 Silicon Errata and Data Sheet Clarification

The PIC18(L)F25/45K22 family devices that you have received conform functionally to the current Device Data Sheet (DS41412**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F25/45K22 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F25/45K22 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A2	A3	A4	A5
PIC18F25K22	0101 0101 010x xxxx	0 0010	0 0011	0 0100	0 0101
PIC18LF25K22	0101 0101 011x xxxx	0 0010	0 0011	0 0100	0 0101
PIC18F45K22	0101 0101 000x xxxx	0 0010	0 0011	0 0100	0 0101
PIC18LF45K22	0101 0101 001x xxxx	0 0010	0 0011	0 0100	0 0101

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the *"PIC18(L)F2XK22/4XK22 Flash Memory Programming Specification"* (DS41398) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A2	A3	A4	A5
Voltage Reference	Default Value	1.1	VREFCON0 = 0x00 at Reset.	X	X		
Voltage Reference	Internal Reference	1.2	Reference may be unstable at low temperatures.	X	X		
HLVD	HLVD module	2.	The HLVD module does not function.	X	X		
Comparators	CxSYNC Control	3.	The comparator output to the device pin (Cx) always bypasses the Timer1 synchronization latch.	X	X		
HS Oscillator	HS Oscillator Start-up	4.	HS oscillator may not start at low voltage/ high temperature.	X	X		
Clock Switching	Fail-Safe mode	5.1	Execution is delayed when waking from Sleep.	X	X		
Clock Switching	Fail-Safe Clock Monitor	5.2	When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.	X	X	X	X
CTMU	Current Source	6.1	Current source is noisy.	X	X		
CTMU	Control Register	6.2	Control registers are not cleared by Resets.	X	X		
CCP3, CCP4 and CCP5	PWM mode	7.	Clock selection by CCP2 only.	X	X		
ADC	GO/$\overline{\text{DONE}}$ bit	8.	GO/$\overline{\text{DONE}}$ bit gets stuck.	X	X		
Power-on Reset (POR)	Power-on Reset	9.	Transient current spikes on some parts during power-up may cause the part to become stuck in Reset.	X	X	X	
Timer1/3/5 Gate	Timer1/3/5 Gate	10.	The Timer1/3/5 gate times cannot be resolved to the two Least Significant bits, when using FOSC as the Timer1/3/5 source.	X	X	X	X
Timer1/3/5	Interrupt	11.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X	X	X	X
EUSART	EUSART Asynchronous Operation	12.1	The EUSART asynchronous operation may miss the Start bit edge.	X	X	X	
EUSART	EUSART Synchronous Operation	12.2	LSb of transmitted data can be corrupt.	X	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Master mode	13.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: Voltage Reference

1.1 The default value of VREFCON0 after Reset is `0x00` instead of `0x10`.

Work around

Select the desired Fixed Voltage Reference buffer as part of initialization.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

1.2 Internal voltage reference may become unstable at cold temperature.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

2. Module: HLVD

Although the HLVDIF flag will be set immediately after enabling the HLVD circuit, the HLVD module is not functional and should not be used.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

3. Module: Comparators

The CxSYNC controls are inoperative. The comparator output (Cx) always bypasses the Timer1 synchronization latch.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

4. Module: HS Oscillator

The HS oscillator may not start when V_{DD} is less than 3V, especially at high temperatures.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

5. Module: Clock Switching

5.1 When Clock Fail-Safe mode or Clock Switchover mode is selected, then code execution will be delayed after waking from Sleep by the start-up time of the HFINTOSC.

Work around

Disable HFINTOSC stabilization time by setting the HFOFST bit of the Configuration register 3H.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

5.2 When the FCMEN Configuration bit is set and the IESO Configuration bit is not set, then a clock failure during Sleep will not be detected.

Work around

The IESO Configuration bit must also be set when the FCMEN Configuration bit is set.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

6. Module: CTMU

6.1 Current source may be noisy to the CTMU module.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

6.2 CTMU control registers are not cleared by the RESET instruction or MCLR Reset.

Work around

Clear the CTMU control registers as part of device initialization.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

7. Module: CCP3, CCP4 and CCP5

PWM mode does not work independently of CCP2. Clock selection is cross-wired with that of CCP2.

Work around

Use CCP1 and/or CCP2 for PWM applications. Reserve CCP3, CCP4 and CCP5 for capture and compare applications.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

8. Module: ADC

GO/DONE bit may become stuck in GO mode.

Work around

Use the ADC FRC clock selection to reduce the probability of the GO bit becoming stuck. To capture the events when the GO bit does become stuck, use one of the timers to determine if the GO bit stays set longer than expected. When this occurs, restart the ADC conversion by clearing the GO/DONE bit and then setting the GO/DONE bit.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X						

9. Module: Power-on Reset (POR)

There may be transient current spikes on some parts during power-up. If the application cannot supply enough current to get past these transients, then the part may become stuck in Reset.

Work around

Ensure that the application is capable of supplying at least 30 mA of transient current during power-up.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X					

10. Module: Timer1/3/5 Gate

The Timer gate times cannot be resolved to the two Least Significant timer bits when the source frequency is FOSC (TMRxCS[1:0]=01). This is because the gate edges are synchronized with the FOSC/4 clock.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

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11. Module: Timer1/3/5

When Timer1, Timer3 or Timer5 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 1.

EXAMPLE 1: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;          //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                  //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;          //Turn on timer

//Now wait at least two full T1CKI periods + 2T_CY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
                               //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                         //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

12. Module: EUSART

12.1 The EUSART asynchronous operation has a probability of 1 in 256 of missing the Start bit edge for all combinations of BRGH and BRG16 values, other than BRGH = 1, BRG16 = 1.

Work around

Set BRGH = 1, and BRG16 = 1 and use this baud rate formula:

$$Baud\_Rate = Fosc/[4([SPBRGH{:}SPBRGL]+1)]$$

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X					

12.2 In Synchronous mode operation, if SPBRG[H:L] = 0x0001, any character that is put in TXREG while a character is still in TSR, will transmit TX9D as the LSb.

Work around

Use the TRMT bit in place of, or in addition to the TXIF bit to ensure that only one character is set to transmit at a time.

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

13. Module: MSSP (Master Synchronous Serial Port)

13.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A2	A3	A4	A5				
X	X	X	X				

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41412**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: ECCP

The auto-shutdown options for the ECCPxAS register (Register 14-5) have been changed as shown below in **bold**.

REGISTER 14-5: ECCPxAS: CCPX AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCPxASE	CCPxAS<2:0>			PSSxAC<1:0>		PSSxBD<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **CCPxASE:** CCPx Auto-shutdown Event Status bit
if PxRSEN = 1;
1 = An Auto-shutdown event occurred; CCPxASE bit will automatically clear when event goes away; CCPx outputs in shutdown state
0 = CCPx outputs are operating
if PxRSEN = 0;
1 = An Auto-shutdown event occurred; bit must be cleared in software to restart PWM; CCPx outputs in shutdown state
0 = CCPx outputs are operating

bit 6-4 **CCPxAS<2:0>:** CCPx Auto-Shutdown Source Select bits **(1)**
000 = Auto-shutdown is disabled
001 = Comparator C1 (async_C1OUT) – output high will cause shutdown event
010 = Comparator C2 (async_C2OUT) – output high will cause shutdown event
011 = Either Comparator C1 or C2 – output high will cause shutdown event
100 = FLT0 pin - low level will cause shutdown event
101 = **FLT0 pin – low level will cause shutdown event or Comparator C1 (async_C1OUT) – output high will cause shutdown event**
110 = **FLT0 pin – low level will cause shutdown event or Comparator C2 (async_C2OUT) – output high will cause shutdown event**
111 = **FLT0 pin – low level will cause shutdown event or Comparators C1 or C2 – output high will cause shutdown event**

bit 3-2 **PSSxAC<1:0>:** Pins PxA and PxC Shutdown State Control bits
00 = Drive pins PxA and PxC to ‘0’
01 = Drive pins PxA and PxC to ‘1’
1x = Pins PxA and PxC tri-state

bit 1-0 **PSSxBD<1:0>:** Pins PxB and PxD Shutdown State Control bits
00 = Drive pins PxB and PxD to ‘0’
01 = Drive pins PxB and PxD to ‘1’
1x = Pins PxB and PxD tri-state

Note 1: If C1SYNC or C2SYNC bits in the CM2CON1 register are enabled, the shutdown will be delayed by Timer1.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2010)

Initial release of this document.

Rev B Document (8/2010)

Updated errata to the new format; Updated for Revision A4 silicon release; Added Modules 5.2, 9.1, 9.2 and 10.

Data Sheet Clarifications: Added Module 1.

Rev C Document (7/2011)

Updated for Revision A5 silicon release; Module 9.1 errata fixed.

Data Sheet Clarifications: No changes.

Rev D Document (8/2011)

Added Module 11, EUSART; Module 11 errata fixed on Silicon revision A5.

Data Sheet Clarifications: No changes.

Rev E Document (2/2012)

Removed Module 9.2; Other minor corrections.

Data Sheet Clarifications: Removed Module 1.

Rev F Document (7/2012)

Added MPLAB X IDE; Added Module 11.2.

Rev G Document (7/2014)

Added Module 11, Timer1/3/5.

Rev H Document (4/2015)

Added Module 12.3.

Rev J Document (7/2015)

Added Module 13.1, MSSP (Master Synchronous Serial Port); Removed Module 12.3, EUSART.

Rev K Document (12/2015)

Data Sheet Clarifications: Added Module 1: ECCP.

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