AVR32801: UC3A3 Schematic Checklist

Features

- **Power circuit**
- **Reset circuit**
- **USB connection**
- **External bus interface**
- **ABDAC sound DAC interface**
- **JTAG and Nexus debug ports**
- **Clocks and crystal oscillators**
- **MMC, SD-card, SDHC, SDIO and CE-ATA interface**

1 Introduction

A good hardware design comes from a proper schematic. Since UC3A3 devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a UC3A3 design.

32-bit AVR® Microcontrollers

Application Note

Rev. 32130B-AVR32-04/10

2 Power circuit

2.1 Single 3.3 volt power supply

Figure 2-1. Single 3.3 volt power example schematic

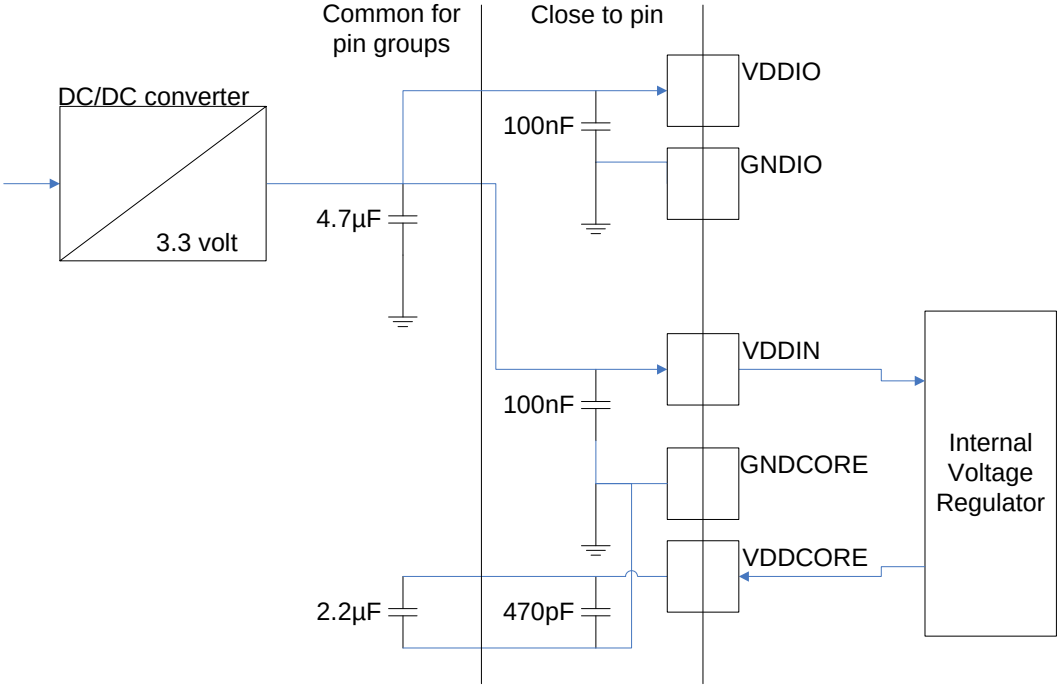

Table 2-1. Single 3.3 volt power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	3.0 V to 3.6 V Decoupling/filtering capacitors 100 nF(1)(2) and 4.7 µF(1)	Powers I/O lines. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	GNDIO	Connect to digital ground	VDDIO ground pin.
	VDDIN	2.7 V to 3.6 V Decoupling/filtering capacitors 100 nF(1)(2) and 4.7 µF(1)	Powers internal voltage regulator. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDCORE	Decoupling/filtering capacitors 470 pF(1)(2) and 2.2 µF(1)	Output of the internal 1.8 V voltage regulator. Decoupling/filtering capacitors must be added to guarantee 1.8 V stability.
	GNDCORE	Connect to digital ground	VDDCORE and VDDIN ground pin.

Note 1: These values are given only as a typical example.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

2.2 ADC reference power supply

The following schematic checklist is mandatory even if the internal analog to digital converter is not in use.

Figure 2-2. ADC power supply example schematic

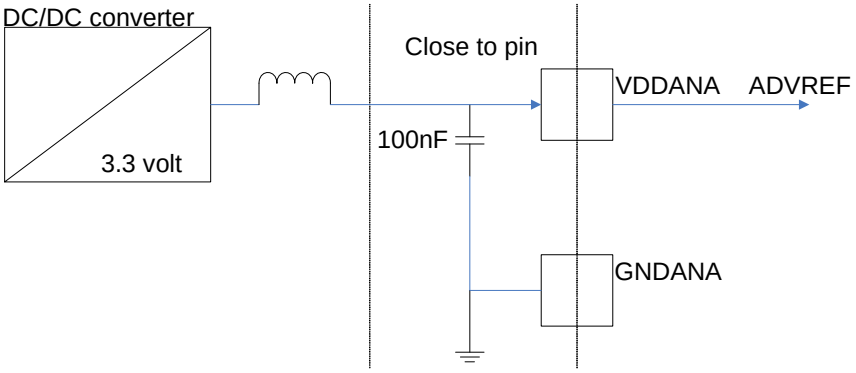

Table 2-2. ADC reference power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDANA	3.0 V to 3.6 V Decoupling/filtering capacitor 100 nF(1)(2)	Powers the on-chip ADC, must always be powered since the analog multiplexer is powered by another domain. Decoupling/filtering capacitor must be added to improve startup stability and reduce source voltage drop. ADVREF (ADC reference voltage) is internally connected to VDDANA
	GNDANA	Connect to analog ground	VDDANA ground pin.

Note 1: These values are given only as a typical example.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

3 Reset circuit

Figure 3-1. Reset circuit example schematic

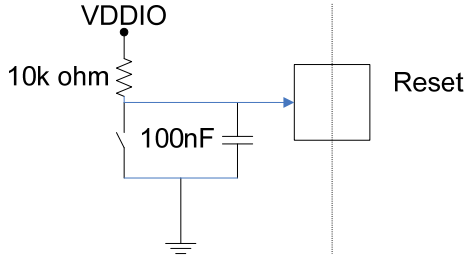

Table 3-1. Reset circuit checklist

☑	Signal name	Recommended pin connection	Description
	RESET	Can be left unconnected in case no reset from the system needs to be applied to the product	The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIO.

4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source schematic

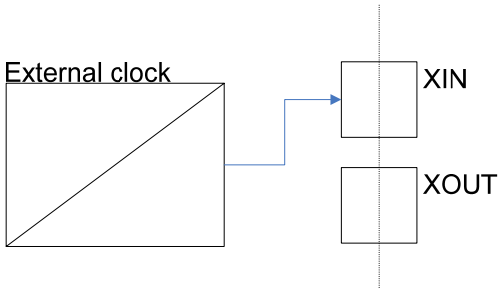

Table 4-1. External clock source checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Connected to clock output from external clock source	Up to VDDIO volt square wave signal up to 50 MHz.
	XOUT	Can be left unconnected or used as GPIO	

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic

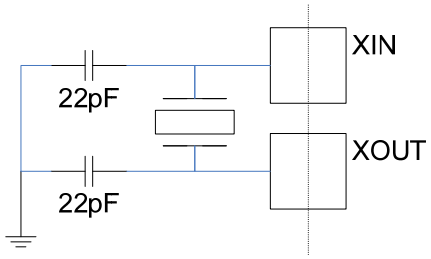

Table 4-2. Crystal oscillator checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Biasing capacitor 22 pF(1)(2)	External crystal between 3 MHz and 16 MHz for XIN0/XOUT0 and XIN1/XOUT2, 32 kHz for XIN32/XOUT32.
	XOUT	Biasing capacitor 22 pF(1)(2)	

Note 1: These values are given only as a typical example. The capacitance *C* of the biasing capacitors can be computed based on the crystal load capacitance C_L and the internal capacitance C_i of the MCU as follows:

$C = 2 (C_L – C_i)$

The value of C_L can be found in the crystal datasheet and the value of C_i can be found in the MCU datasheet.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

5 USB connection

USB high-speed PCB layout design is covered in application note *AVR32787*, more information in chapter 10.3 on page 21.

5.1 Not used

When the USB interface is not used, FSPDM, HSDM, FSDP and HSDP should be connected to ground.

5.2 Device mode, powered from bus connection

Figure 5-1. USB in device mode, bus powered connection example schematic

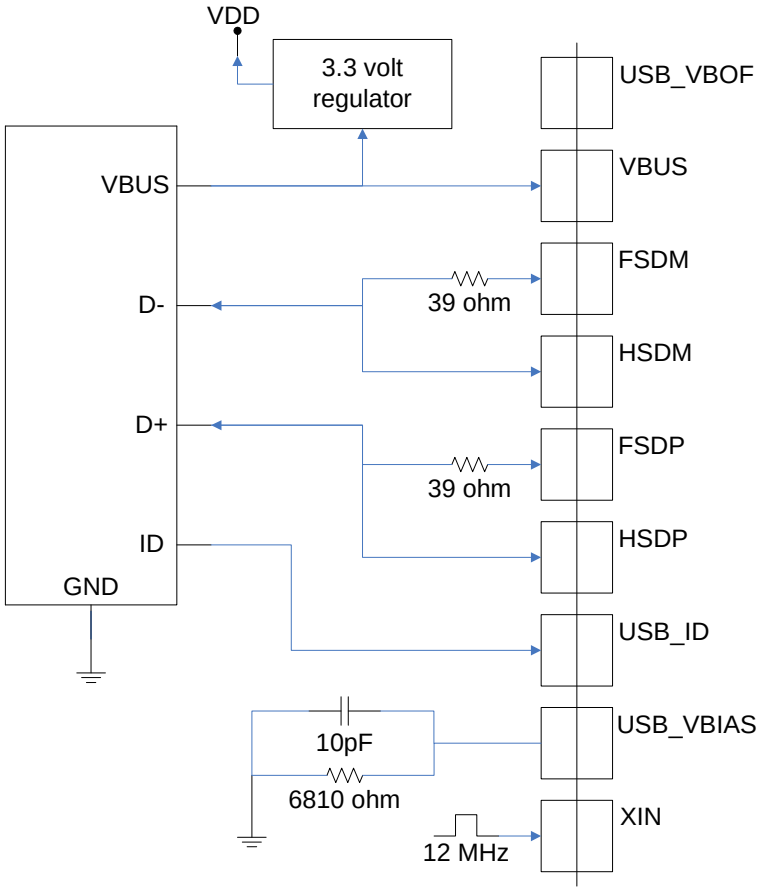

Table 5-1. USB bus powered connection checklist

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	Can be left unconnected or used as GPIO	USB power control pin.
	VBUS	Directly to connector	USB power measurement pin.
	FSDM	39 ohm series resistor Placed as close as possible to pin	Negative differential full-speed data line.
	FSDP	39 ohm series resistor Placed as close as possible to pin	Positive differential full-speed data line.

☑	Signal name	Recommended pin connection	Description
	HSDM	Directly to connector	Negative differential high-speed data line.
	HSDP	Directly to connector	Positive differential high-speed data line.
	USB_ID	Can be left unconnected	Mini connector USB identification pin.
	USB_VBIAS	6810 ohm ±1% resistor in parallel to a 10pF capacitor to ground	USB bias voltage reference.
	XIN	External 12 MHz clock or crystal	The UTMI transceiver requires an external 12 MHz clock as a reference to its internal 480Mhz PLL. This clock is provided by GCLK4 and the generic clock needs a 12 MHz source.

5.3 Device mode, self powered connection

Figure 5-2. USB in device mode, self powered connection example schematic

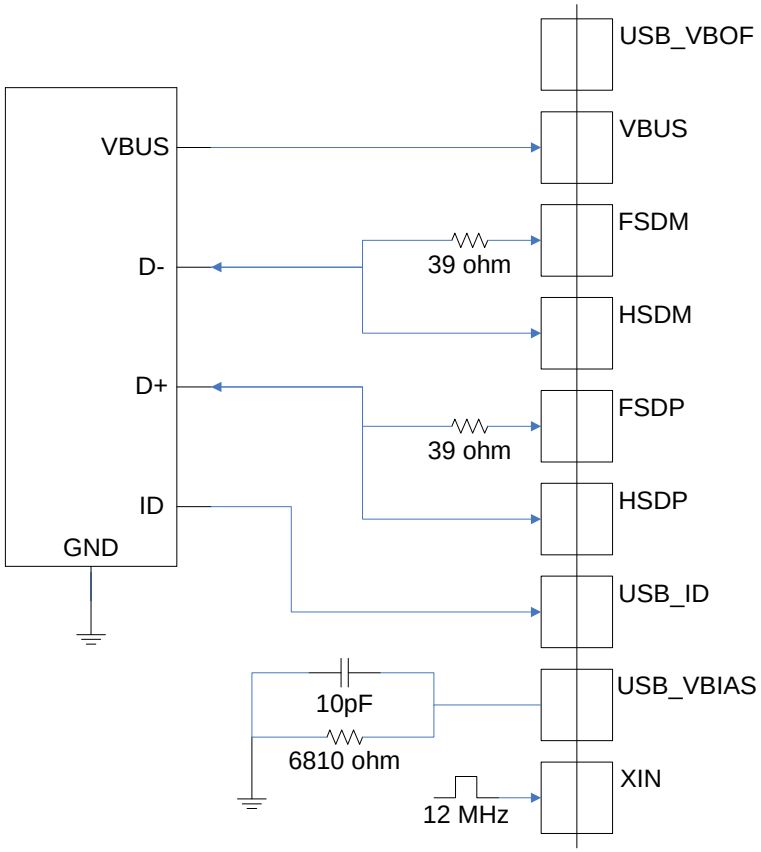

Table 5-2. USB self powered connection checklist

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	Can be left unconnected or used as GPIO	USB power control pin.
	VBUS	Directly to connector	USB power measurement pin.
	FSDM	39 ohm series resistor Placed as close as possible to pin	Negative differential full-speed data line.
	FSDP	39 ohm series resistor Placed as close as possible to pin	Positive differential full-speed data line.

☑	Signal name	Recommended pin connection	Description
	HSDM	Directly to connector	Negative differential high-speed data line.
	HSDP	Directly to connector	Positive differential high-speed data line.
	USB_ID	Can be left unconnected	Mini connector USB identification pin.
	USB_VBIAS	6810 ohm ±1% resistor in parallel to a 10pF capacitor to ground	USB bias voltage reference.
	XIN	External 12 MHz clock or crystal	The UTMI transceiver requires an external 12 MHz clock as a reference to its internal 480Mhz PLL. This clock is provided by GCLK4 and the generic clock needs a 12 MHz source.

5.4 Host/OTG mode, power from bus connection

Figure 5-3. USB host and OTG powering connection example schematic

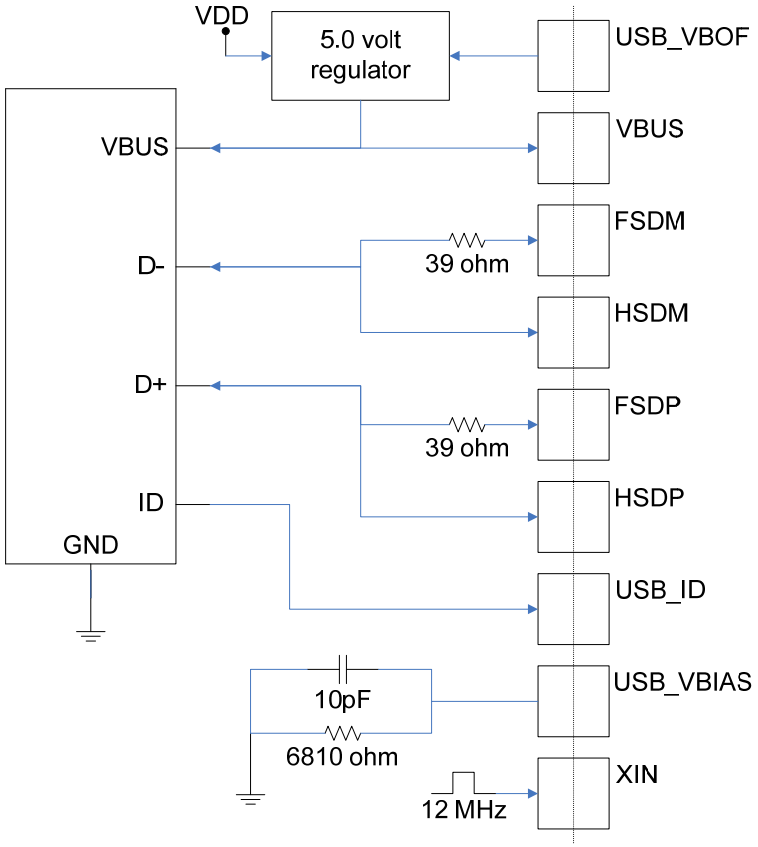

Table 5-3. USB host and OTG powering connection checklist

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	Can be left unconnected or used as GPIO	USB power control pin.
	VBUS	Directly to connector	USB power measurement pin.
	FSDM	39 ohm series resistor Placed as close as possible to pin	Negative differential full-speed data line.
	FSDP	39 ohm series resistor Placed as close as possible to pin	Positive differential full-speed data line.

☑	Signal name	Recommended pin connection	Description
	HSDM	Directly to connector	Negative differential high-speed data line.
	HSDP	Directly to connector	Positive differential high-speed data line.
	USB_ID	GPIO directly connected to connector, mandatory in OTG mode	Mini connector USB identification pin. For OTG it will be tied to ground in host mode, and left floating in device mode. Pull-up on GPIO pin must be enabled.
	USB_VBIAS	6810 ohm ±1% resistor in parallel to a 10pF capacitor to ground	USB bias voltage reference.
	XIN	External 12 MHz clock or crystal	The UTMI transceiver requires an external 12 MHz clock as a reference to its internal 480Mhz PLL. This clock is provided by GCLK4 and the generic clock needs a 12 MHz source.

6 External bus interface

6.1 Static memory

6.1.1 16-bit static memory

Table 6-1. 16-bit static memory pin wiring

☑	GPIO line name	16-bit static memory
	D[0:15]	D[0:15]
	A[1:23]	A[0:22]
	A[0] (NBS0)	LBE
	NWE1 (NBS1)	HBE
	NWE0	WE
	NRD	OE
	NWAIT	WAIT
	NCSx	CS

6.1.2 8-bit static memory

Table 6-2. 8-bit static memory pin wiring

☑	GPIO line name	8-bit static memory
	D[0:7]	D[0:7]
	A[0:23]	A[0:23]
	NWE0	WE
	NRD	OE
	NWAIT	WAIT
	NCSx	CS

6.1.3 2 x 8-bit static memory

Table 6-3. 2 x 8-bit static memory pin wiring

☑	GPIO line name	8-bit static memory	8-bit static memory
	D[0:7]	D[0:7]	

☑	GPIO line name	8-bit static memory	8-bit static memory
	D[8:15]		D[0:7]
	A[1:23]	A[0:22]	A[0:22]
	NWE0 (NBS0)	WE	
	NWE1 (NBS1)		WE
	NRD	OE	OE
	NWAIT	WAIT	WAIT
	NCSx	CS	CS

6.2 SDRAM

6.2.1 16-bit SDRAM

Table 6-4. 16-bit SDRAM pin wiring

☑	GPIO line name	16-bit SDRAM
	D[0:15]	DQ[0:15]
	A[2:11]	A[0:9]
	SDA10	A[10]
	A[13:14]	A[11:12]
	A[16] (BA0)	BA0
	A[17] (BA1)	BA1
	SDCK	CLK
	SDCKE	CKE
	SDWE	WE
	RAS	RAS
	CAS	CAS
	A[0] (NBS0)	DQML
	NWE1 (NBS1)	DQMH
	NCS[1] (SDCS)	CS

6.2.2 2 x 8-bit SDRAM

Table 6-5. 2 x 8-bit SDRAM pin wiring

☑	GPIO line name	8-bit SDRAM	8-bit SDRAM
	D[0:7]	DQ[0:7]	
	D[7:15]		DQ[0:7]
	A[2:11]	A[0:9]	A[0:9]
	SDA10	A[10]	A[10]
	A[13:14]	A[11:12]	A[11:12]
	A[16] (BA0)	BA0	BA0
	A[17] (BA1)	BA1	BA1
	SDCK	CLK	CLK
	SDCKE	CKE	CKE

☑	GPIO line name	8-bit SDRAM	8-bit SDRAM
	SDWE	WE	WE
	RAS	RAS	RAS
	CAS	CAS	CAS
	A[0] (NBS0)	DQM	
	NWE1 (NBS1)		DQM
	NCS[1] (SDCS)	CS	CS

6.2.3 4 x 4-bit SDRAM

Table 6-6. 4 x 4-bit SDRAM pin wiring

☑	GPIO line name	4-bit SDRAM	4-bit SDRAM	4-bit SDRAM	4-bit SDRAM
	D[0:3]	DQ[0:3]			
	D[4:7]		DQ[0:3]		
	D[8:11]			DQ[0:3]	
	D[12:15]				DQ[0:3]
	A[2:11]	A[0:9]	A[0:9]	A[0:9]	A[0:9]
	SDA10	A[10]	A[10]	A[10]	A[10]
	A[13:14]	A[11:12]	A[11:12]	A[11:12]	A[11:12]
	A[16] (BA0)	BA0	BA0	BA0	BA0
	A[17] (BA1)	BA1	BA1	BA1	BA1
	SDCK	CLK	CLK	CLK	CLK
	SDCKE	CKE	CKE	CKE	CKE
	SDWE	WE	WE	WE	WE
	RAS	RAS	RAS	RAS	RAS
	CAS	CAS	CAS	CAS	CAS
	A[0] (NBS0)	DQM	DQM		
	NWE1 (NBS1)			DQM	DQM
	NCS[1] (SDCS)	CS	CS	CS	CS

6.3 CompactFlash

Table 6-7. 8-bit and 16-bit CompactFlash pin wiring

☑	GPIO line name	16-bit CompactFlash
	D[0:7]	D[0:7]
	D[8:15](1)	D[8:15]
	A[0:10]	A[0:10]
	A[22]	REG
	NSC[4](2)	CFCS[0]
	NSC[5](2)	CFCS[1]
	NRD	OE
	NWE0	WE
	NWE1	IOR
	NWE0 *OR* A[23](3)	IOW
	CFRNW(2)	CFRNW
	CFCE1	CE1
	CFCE2	CE2
	NWAIT	WAIT
	GPIO[n](4)	CD1 or CD2

Notes:
1. Only needed for 16-bit CompactFlash.
2. Not directly connected to the CompactFlash slot. Permits control of a bidirectional buffer between the EBI and the CompactFlash slot.
3. NWE0 and A[23] must be combined externally using an OR logic gate to produce the IOW signal for the CompactFlash slot.
4. Any GPIO line.

6.4 NAND flash

6.4.1 8-bit and 16-bit NAND flash

Table 6-8. 8-bit and 16-bit NAND flash pin wiring

☑	GPIO line name	8-bit or 16-bit NAND flash
	D[0:7]	I/O[0:7] (data bus)
	D[8:15](1)	I/O[8:15] (data bus)
	A[21]	CLE (command latch enable)
	A[22]	ALE (address latch enable)
	NANDOE	RE (read enable)
	NANDWE	WE (write enable)
	GPIO[n](2)	CE (chip enable)
	GPIO[n](2)	R/B (ready/busy)

Notes:
1. Only needed for 16-bit NAND.
2. Any GPIO line.

7 ABDAC stereo sound DAC interface

The output from the ABDAC is not intended for driving headphones or speakers. The pads are limiting the maximum amount of current. In the majority of all practical cases, this will not be enough to drive a low impedance source.

Because of this limitation, an external amplifier should be connected to the output lines to amplify these signals. This amplifier device could also be used to control the volume.

For testing purposes a line in or microphone input on a sound system can be used to evaluate the output signal.

7.1 Line out with passive filter

Figure 7-1. Line out with passive filter example schematic

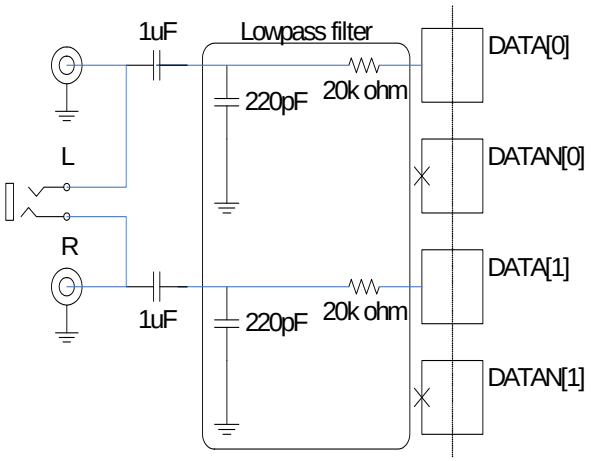

Table 7-1. Line out with passive filter checklist

☑	Signal name	Recommended pin connection	Description
	DATA[0]	Connected to low pass filter and 1 µF capacitor to remove DC bias	
	DATAN[0]	Not in use	
	DATA[1]	Connected to low pass filter and 1 µF capacitor to remove DC bias	
	DATAN[1]	Not in use	

7.2 High power output with external amplifier

Figure 7-2. High power output with external amplifier example schematic

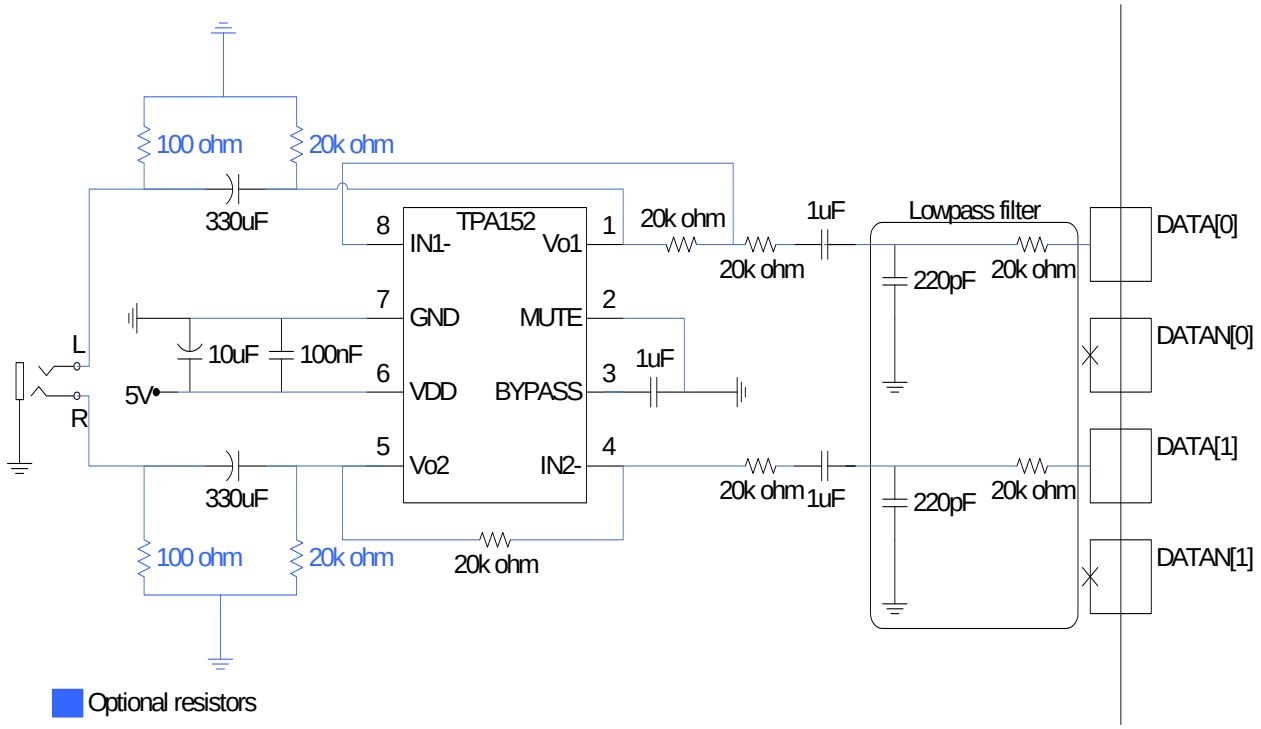

Table 7-2. High power output with external amplifier checklist

☑	Signal name	Recommended pin connection	Description
	DATA[0]	Connected to low pass filter and external amplifier	
	DATAN[0]	Not in use	
	DATA[1]	Connected to low pass filter and external amplifier	
	DATAN[1]	Not in use	

8 JTAG and Nexus debug ports

8.1 JTAG port interface

Figure 8-1. JTAG port interface example schematic

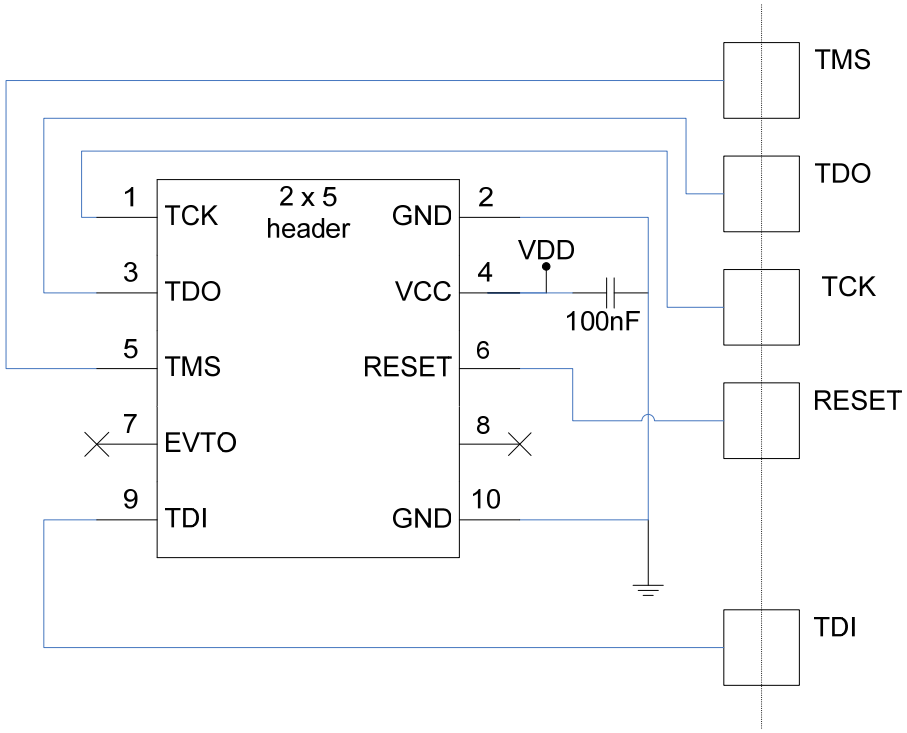

Table 8-1. JTAG port interface checklist

☑	Signal name	Recommended pin connection	Description
	TMS		Test mode select, sampled on rising TCK.
	TDO		Test data output, driven on falling TCK.
	TCK		Test clock, fully asynchronous to system clock frequency.
	RESET		Device external reset line.
	TDI		Test data input, sampled on rising TCK.
	EVTO		Event output, not used.

8.2 Nexus port interface

Figure 8-2. Nexus port interface example schematic

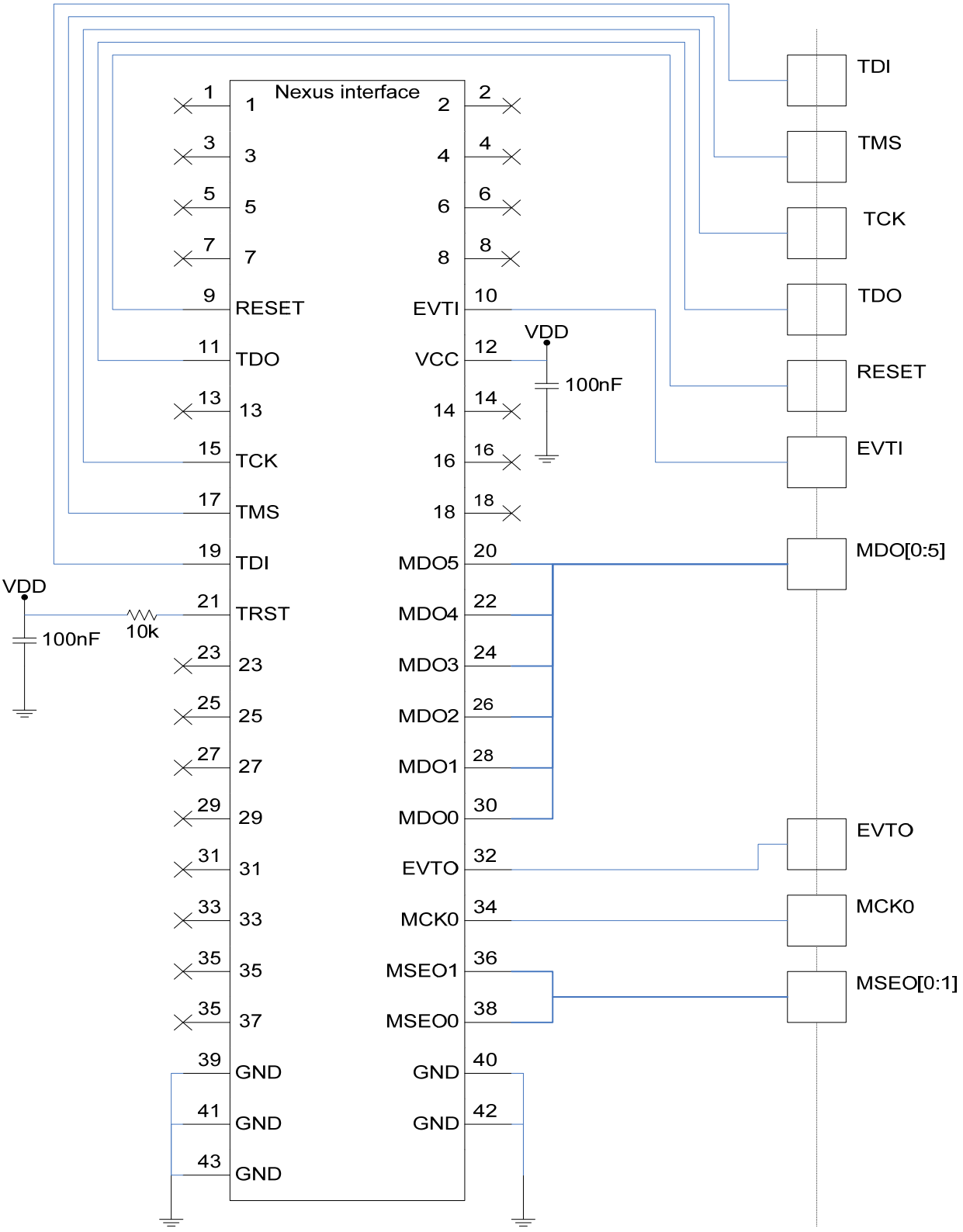

Table 8-2. Nexus port interface checklist

☑	Signal name	Recommended pin connection	Description
	TDI		Test data input, sampled on rising TCK.
	TMS		Test mode select, sampled on rising TCK.
	TCK		Test clock, fully asynchronous to system clock frequency.
	TDO		Test data output, driven on falling TCK.
	RESET		Device external reset line.
	EVTI		Event input.
	MDO[0:5]		Trace data output.
	EVTO		Event output.
	MCK0		Trace data output clock.
	MSE[0:1]		Trace frame control.

9 MMC, SD, SDHC, SDIO and CE-ATA interface

The MMC, SD, SDHC, SDIO and CE-ATA interface is provided by the MultiMedia Card Interface (MCI). Designers are free to mix MMC, SD, SDHC, SDIO and CE-ATA on the bus, but each slot on the MCI can only interface one type of memory.

Examples:

- Slot A is used for MMC bus while slot B is used for SD/SDHC/SDIO.
- Slot A is used for SD/SDHC/SDIO while slot B is used for SD/SDHC/SDIO.
- Slot A is used for SD/SDHC/SDIO while slot B is used for CE-ATA.
- Slot A is used for CE-ATA while slot B is used for MMC bus.

9.1 MMC bus connection

Figure 9-1. MMC bus connection example schematic

Error! No topic specified.

Table 9-1. MMC bus connection checklist

☑	Signal name	Recommended pin connection	Description
	CMD0	Connect to MMC CMD signal Pull-up resistor required, 68 kohm(1)	Command and response signal for the MMC bus on MCI slot A.
	CMD1	Connect to MMC CMD signal Pull-up resistor required, 68 kohm(1)	Command and response signal for the MMC bus on MCI slot B.
	CLK	Connect to MMC CLK signal	Shared clock signal for both MCI slot A and slot B.
	DATA[0:7]	Connect to MMC data lines Pull-up resistors required, 68 kohm(1)	MMC bus data lines for slot A. Only DATA0 is needed in 1-bit mode, DATA[0:3] is needed for 4-bit mode and DATA[0:7] is needed for 8-bit mode.
	DATA[8:15]	Connect to MMC data lines Pull-up resistors required, 68 kohm(1)	MMC bus data lines for slot B. Only DATA8 is needed in 1-bit mode, DATA[8:11] is needed for 4-bit mode and DATA[8:15] is needed for 8-bit mode.
	Card detect	Optional, connect to any GPIO line Pull-up resistor required, 68 kohm(1)	Card detection signal from the card slot, can be used by the firmware to detect card insertion and removal.

Note 1: These values are given as a typical example and must be placed as close as possible to the MMC card slot.

9.2 SD, SDHC and SDIO bus connection

Figure 9-2. SD, SDHC and SDIO bus connection example schematic

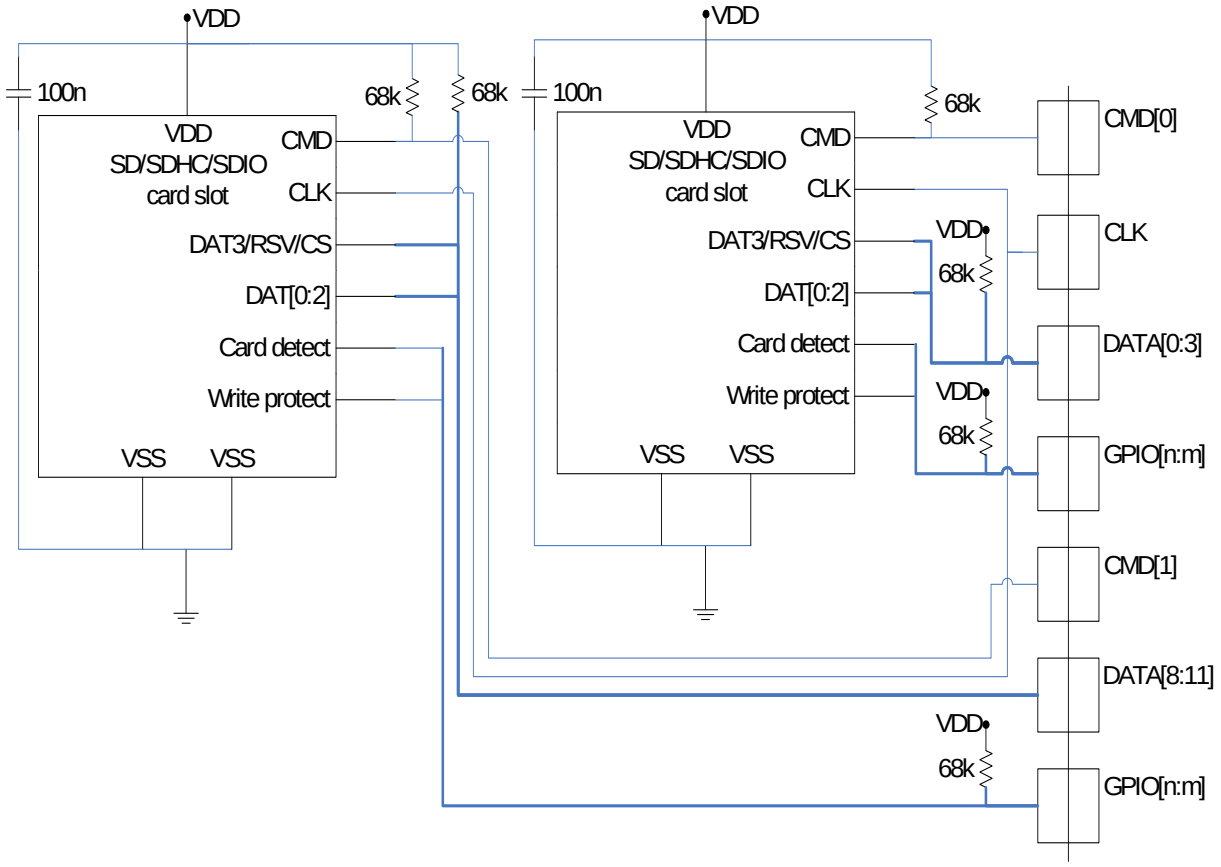

Table 9-2. SD, SDHC and SDIO bus connection checklist

☑	Signal name	Recommended pin connection	Description
	CMD0	Connect to SD/SDHC/SDIO CMD signal Pull-up resistor required, 68 kohm(1)	Command and response signal for the SD/SDHC/SDIO bus on MCI slot A.
	CMD1	Connect to SD/SDHC/SDIO CMD signal Pull-up resistor required, 68 kohm(1)	Command and response signal for the SD/SDHC/SDIO bus on MCI slot B.
	CLK	Connect to SD/SDHC/SDIO CLK signal	Shared clock signal for both MCI slot A and slot B.
	DATA[0:4]	Connect to SD/SDHC/SDIO data lines Pull-up resistors required, 68 kohm(1)	SD/SDHC/SDIO bus data lines for MCI slot A. Only DATA0 is needed in 1-bit mode and DATA[0:3] is needed for 4-bit mode.
	DATA[8:11]	Connect to SD/SDHC/SDIO data lines Pull-up resistors required, 68 kohm(1)	SD/SDHC/SDIO bus data lines for MCI slot B. Only DATA8 is needed in 1-bit mode and DATA[8:11] is needed for 4-bit mode
	Card detect	Optional, connect to any GPIO line Pull-up resistor required, 68 kohm(1)	Card detection signal from the card slot, can be used by the firmware to detect card insertion and removal.
	Write protect	Optional, connect to any GPIO line Pull-up resistor required, 68 kohm(1)	Write protect signal from the card slot, can be used by the firmware to identify if the card has the write protect switch set.

Note 1: These values are given as a typical example and must be placed as close as possible to the SD/SDHC/SDIO card slot.

9.3 CE-ATA bus connection

9.3.1 4-bit CE-ATA bus connection

Table 9-3. 4-bit CE-ATA connector pin wiring

☑	I/O line name	Connector pin	4-bit CE-ATA
	Ground	1	VSS
	DAT2(1) / DAT10(1)	2	DAT2
	DAT3(1) / DAT11(1)	3	DAT3
	VCC 3.3 V(2)	4	Supply voltage
	CMD0(1) / CMD1(1)	5	CMD
	VCC 3.3 V(2)	6	Interface voltage
	CLK	7	CLK
	Ground	8	VSS
	DAT0(1) / DAT8(1)	9	DAT0
	DAT1(1) / DAT9(1)	10	DAT1
	Ground	11	VSS
	Not connected	12	Reserved

Notes:
1. Data lines and CMD line must mach for selected MCI slot. I.e. CMD0 must be used along with DAT[0:4] and CMD1 must be used along with DAT[8:11].
2. 100 nF decoupling capacitor should be placed as close as possible to connector.

9.3.2 8-bit CE-ATA bus connection

Table 9-4. 8-bit CE-ATA connector pin wiring

☑	I/O line name	Connector pin	8-bit CE-ATA
	Ground	1	VSS
	DAT2(1) / DAT10(1)	2	DAT2
	DAT3(1) / DAT11(1)	3	DAT3
	Ground	4	VSS
	DAT4(1) / DAT12(1)	5	DAT4
	DAT5(1) / DAT13(1)	6	DAT5
	VCC 3.3 V(2)	7	Supply voltage
	CMD0(1) / CMD1(1)	8	CMD
	VCC 3.3 V(2)	9	Interface voltage
	CLK	10	CLK
	Ground	11	VSS
	DAT6(1) / DAT14(1)	12	DAT6
	DAT7(1) / DAT15(1)	13	DAT7
	Ground	14	VSS
	DAT0(1) / DAT8(1)	15	DAT0
	DAT1(1) / DAT9(1)	16	DAT1
	Ground	17	VSS
	Not connected	18	Reserved

Notes:
1. Data lines and CMD line must mach for selected MCI slot. I.e. CMD0 must be used along with DAT[0:7] and CMD1 must be used along with DAT[8:15].
2. 100 nF decoupling capacitor should be placed as close as possible to connector.

10 Suggested reading

10.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/AVR32 in the *Datasheets* section.

10.2 Evaluation kit schematic

The evaluation kit EVK1104 contains the full schematic for the board; it can be used as a reference design. The schematic is available on http://www.atmel.com/AVR32 in the *Tools & Software* section.

10.3 High-speed USB PCB layout

The application note *AVR32787 AVR32 UC3A3 High Speed USB Design Guidelines* covers the basic topics of high-speed USB layout design using AVR UC3A3.

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