

ENT-AN0144
Application Note
VSC8664 Design and Layout Guide

May 2007



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in May 2007.

2 Introduction

This document provides useful guidelines for the design and layout of printed circuit boards utilizing the VSC8664 Quad PHY. It is geared toward achieving first pass design success.

2.1 References

2.1.1 Vitesse Documents

- VSC8664 Datasheet

2.1.2 IEEE Standards

- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification

2.1.3 External Documents

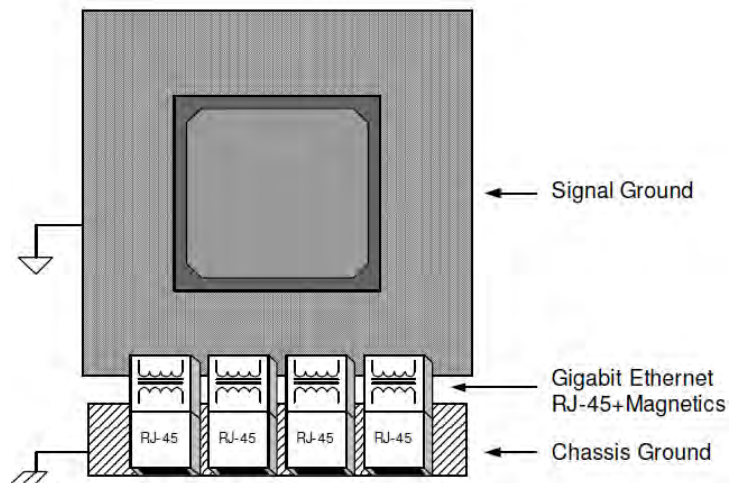
- High Speed Digital Design, Author: Howard Johnson, PH.D., ISBN 0-13-395724-1

3 Ground Considerations

3.1 Ground Isolation

To isolate the board from ESD events and to prevent a common-mode noise ground path, a separate chassis ground region should be allocated. This separate chassis ground should be electrically connected to the external chassis and to the shield ground of the RJ-45 connectors.

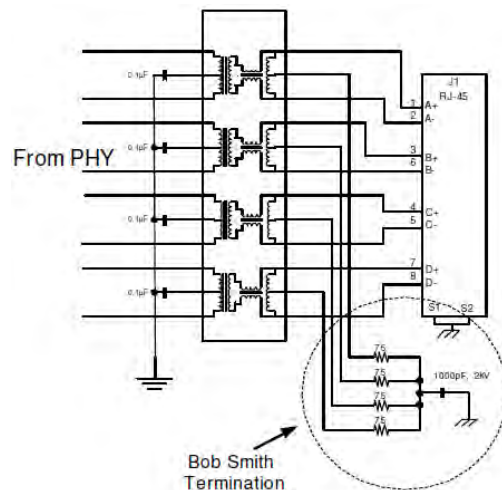
Figure 1 • Ground Plane Layout



3.2 Bob Smith Termination

In addition, the “Bob Smith” termination impedance should be connected between the chassis ground and the cable-side center taps of the transformer module.

Figure 2 • Bob Smith Termination Diagram



4 Power Considerations

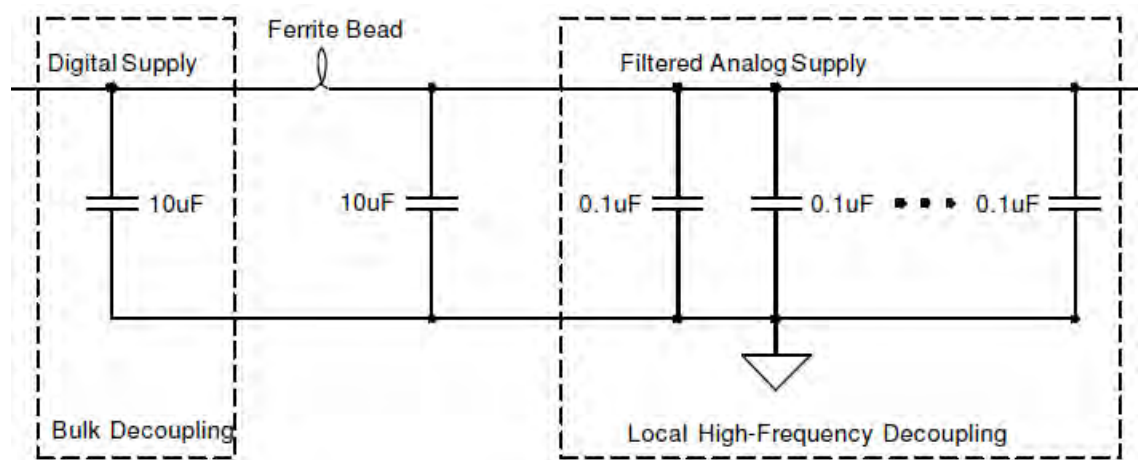
4.1 Power Supply Planes

The VSC8664 requires three power supplies: 3.3 V, 1.2 V, and 1.2 V filtered analog that connect to the power pins of the device. For four layer PCBs with only one designated power plane, proper design techniques must be adhered to prevent random system event such as CRC errors. Each of these supplies to the power pins of the VSC8664 require the lowest resistive drop possible with properly placed local decoupling as described in Section 3.3.

4.2 Analog Power Plane Filtering

A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.

Figure 3 • Filtered Supply Schematic



The beads should be chosen to have the following characteristics:

- Current rating of at least 150% of the maximum current of the power supply
- Impedance of 80 Ω to 100 Ω at 100 MHz

Recommended beads are:

- Panasonic EXCELSA39 or similar
- Steward HI1206N101R-00 or similar

Since all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0 Ω resistors, once thorough evaluation of system performance is completed.

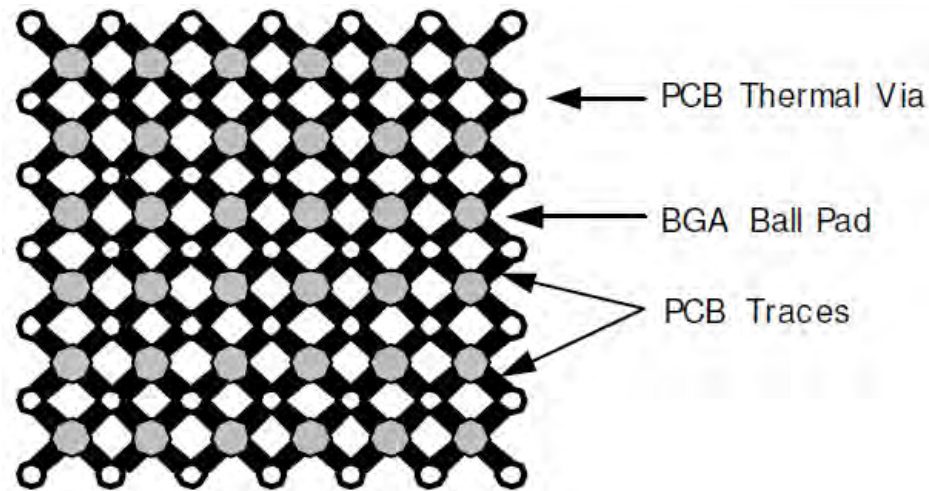
4.3 Local Decoupling

Bulk decoupling capacitors should be tantalum and can be placed at any convenient position on the board. Local decoupling capacitors should be placed as closed to the VSC8664's power pins as possible. The best location for local decoupling capacitors is on the bottom of the board, directly under the device.

5 Thermal Considerations

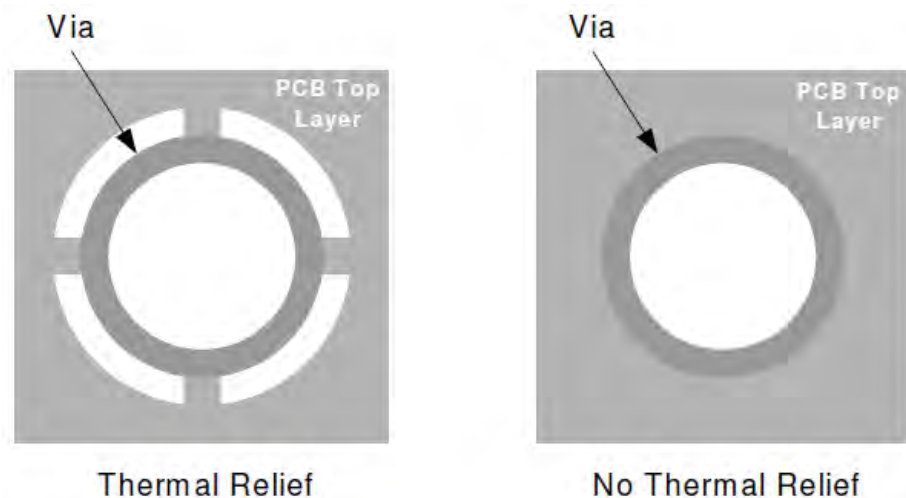
For proper cooling, a PCB via must be placed between the thermal BGA ball pads in a checkerboard pattern. Each of these “thermal vias” should then be routed to the BGA ball pads near it with a wide trace or solid copper fill to increase the conductive area on the surface of the PCB. The following figure shows thermal via layout.

Figure 4 • Thermal Via Layout

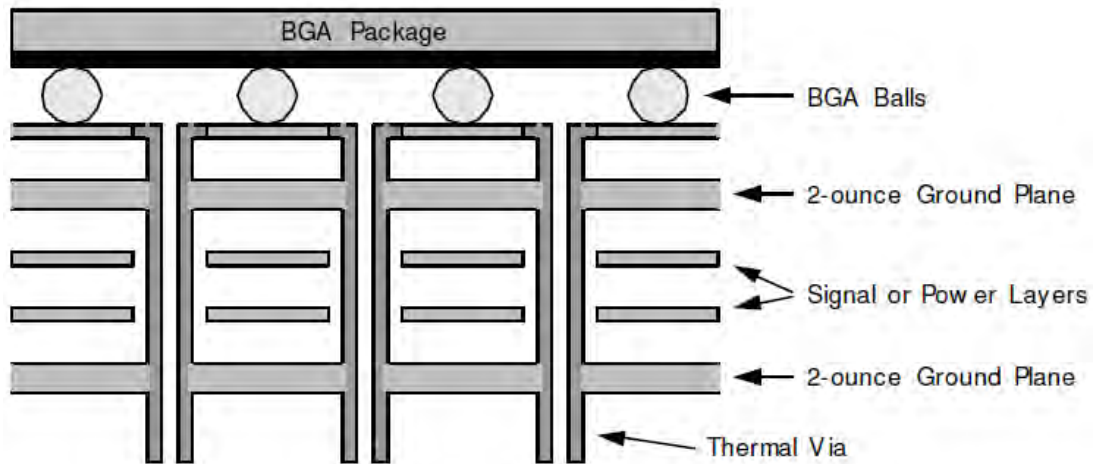


When connecting these thermal vias to ground planes, it is advisable not to use thermal-relief connection traces, as these are designed to prevent the flow of heat through the PCB. Instead, the thermal via should have a solid connection to the traces and planes on each layer. The following figure shows thermal vias.

Figure 5 • Thermal Vias



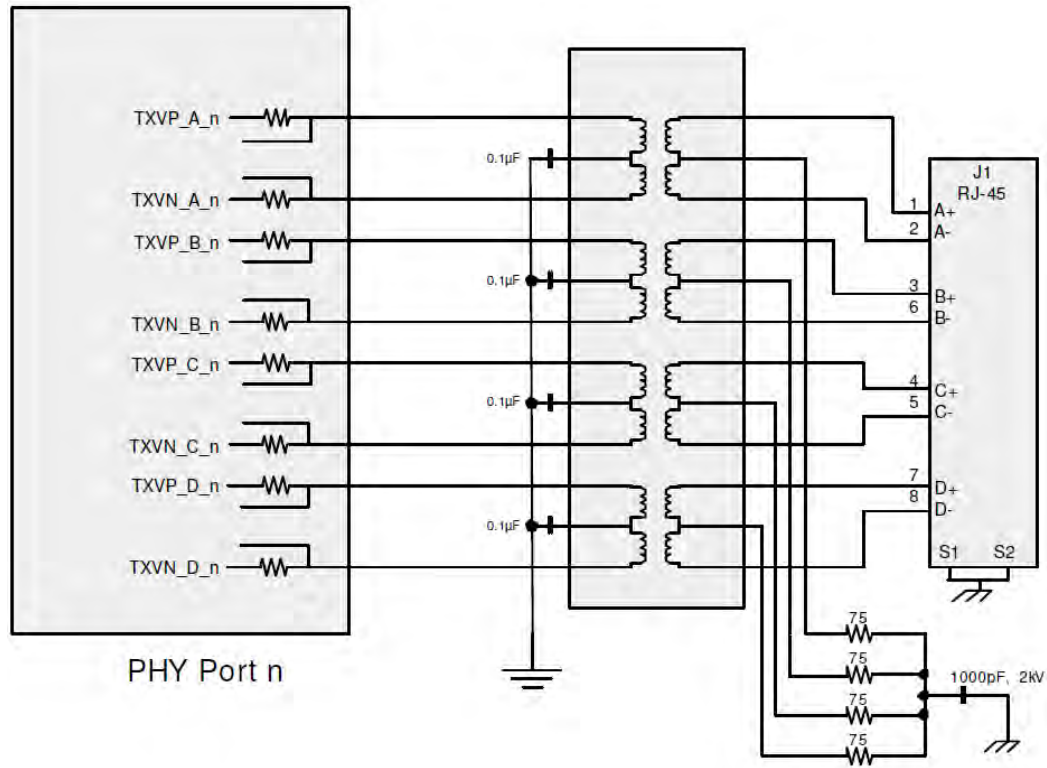
In order to dissipate heat below the BGA package, the PCB thermal vias should connect to the solid ground planes within the board. It is recommended that each ground plane have a minimum thickness of two ounces for best MJB thermal dissipation. The following figure shows the thermal ground plane connections.



6 Copper Interface

A copper PHY media interface is shown in the figure.

Figure 6 • Copper/CAT-5 Interface Diagram



6.1 Layout Considerations

The TXVPx_n and TXVNx_n pins interface to the external CAT5 cable and are organized in four differential pairs (x = A, B, C, D) for each PHY port (n = 0...7). When routing these pairs on a PCB, the characteristics must match one of the following:

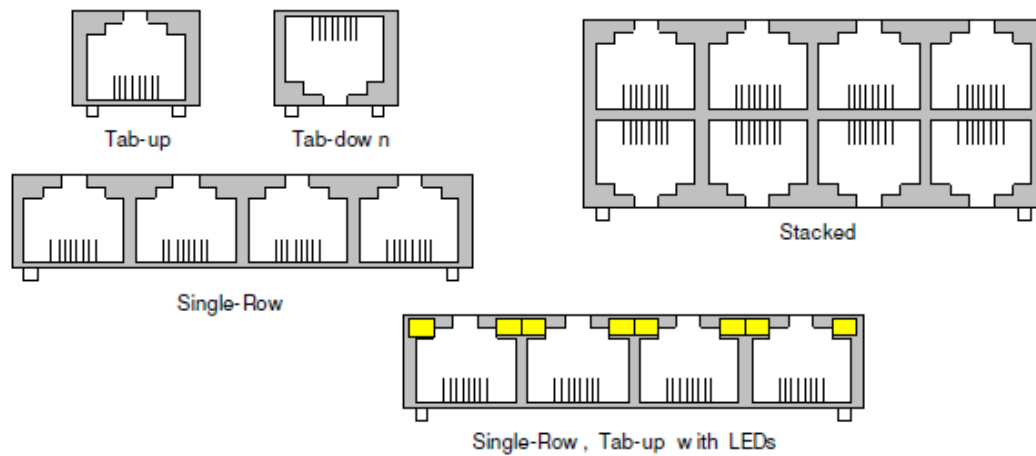
- Route each trace single-ended with a characteristic impedance of 50P referenced to ground.
OR
- Route each positive and negative trace on each port as differential pairs with 100P characteristic differential impedance.

6.2 RJ-45 Connectors

For system designers, several options exist for the choice of RJ-45 connectors. These are summarized as follows:

- Two tab orientations: tab-up and tab-down
- For multi-port connectors, two orientations: stacked and single-row
- Single and bi-colored LEDs can be integrated into the connectors.
- Magnetics can be integrated into the connectors.

Most manufacturers can mix or match any combination of features. For example, LEDs can be added to any connector, or single-row, multi-port configurations can be tab-up or tab-down. The exception is the stacked connector, which contains both tab-up and tab-down orientations.

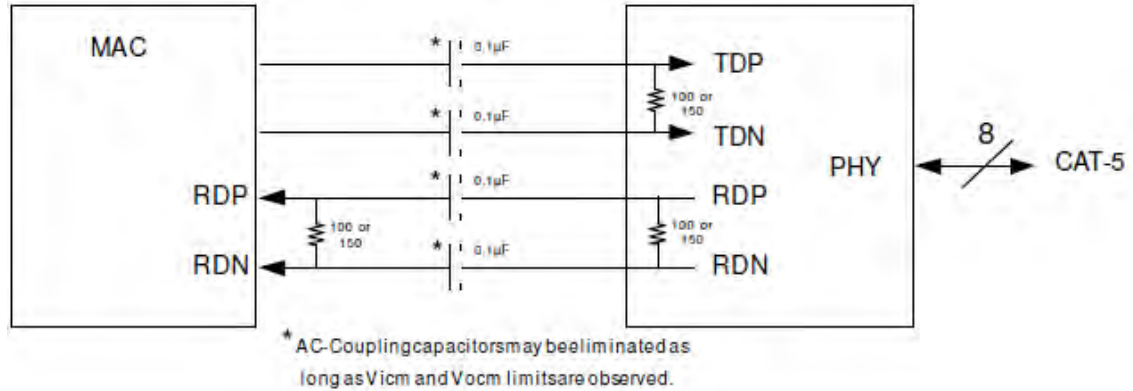
Figure 7 • RJ-45 Example Configurations

An additional consideration is the pinout of tab-up versus tab-down connectors. Due to the orientation, the pinouts of these two are reversed. While the VSC8664 will work equally well using either orientation, signal routing will be simpler with the tab-down pinout. For the stacked variety, both orientations exist in one package, so both pinouts typically exist in one package. Some manufacturers have provided an option for “vertical” pin orientation, which allows for ease in PCB routing.

7 SerDes Interface

A typical MAC-to-PHY serial interface is shown in the following figure.

Figure 8 • Typical MAC-to-PHY Serial Interface



7.1 Design Rules

Best performance will result when SerDes traces are placed using the following design rules:

- Traces should be routed as 50P (100P differential) controlled impedance transmission lines (microstrip, or stripline).
- Traces should be of equal length on each differential pair and port to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Traces should avoid vias and layer changes.
- For applications not requiring a specific port's SGMII interface pins, these pins should be left floating (no-connects).

7.2 AC Coupling Capacitors

In general SerDes interfaces require series AC coupling capacitors to prevent common mode voltages from interfering with transmit and receive operation. If the common mode input and output specifications for the MAC and VSC8664 are compatible (refer to the VSC8664 datasheet) then the AC capacitors can be removed. Note that the VSC8664 has integrated AC coupling Capacitors on their receive paths of the SerDes MAC and media interfaces. For more information, refer to the VSC8664 datasheet.

7.3 SerDes Media

The VSC8664 has an additional SerDes interface to support SerDes Media such as 1000BASE-X Fiber, 100BASE-FX fiber, or 10/100/1000BASE-T Copper SFPs. For more design implementation information, refer to AN0065 Dual Copper/Fiber/SFP Guide. [Section 6.1](#) of this document will apply to this interface.

8 Miscellaneous Design Considerations

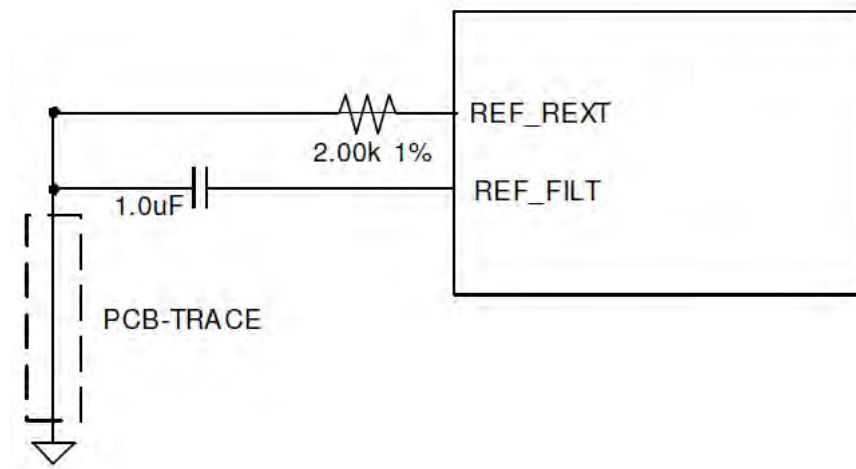
8.1 REF_FILT / REF_REXT Pins

For proper operation, the VSC8664 must generate an on-chip bad gap reference voltage at the REF_FILT pin. For this, the following components are required for each VSC8664 in the system:

- 2.0 k Ω resistor, 1% tolerance, minimum 1/16 W
- 1 μ F capacitor, 10% tolerance, NPO, X7R, or X5R ceramic materials are all acceptable

For best performance, special considerations for the ground connection of the voltage reference circuit are necessary to prevent bus drops that would cause inaccuracy of the reference voltage. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace, rather than being connected individually to a common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8664. See the following figure.

Figure 9 • Voltage Reference Schematic

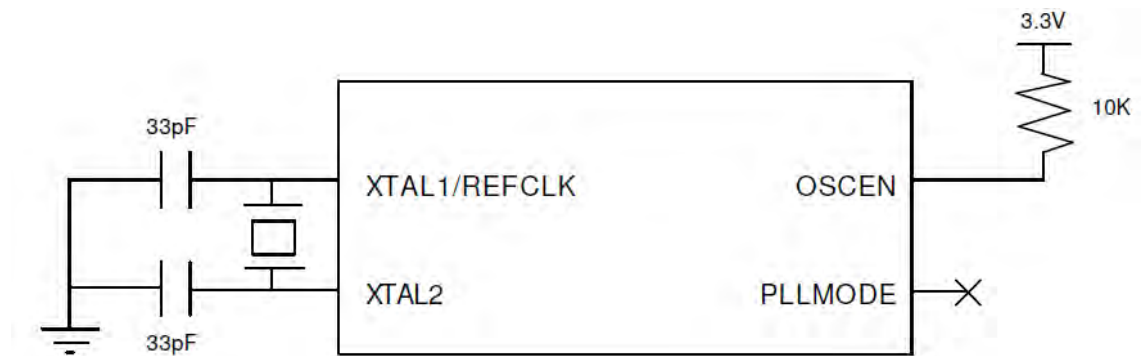


8.2 Clock Inputs

The VSC8664 can be driven by three different clocking schemes providing the end user with design flexibility for their system clock strategy.

8.2.1 Crystal Clock Option

A 25 MHz crystal can be connected to the XTAL1 and XTAL2 pins. The OSCEN pin will need to be pulled high and the PLLMODE can be left floating. See the following figure.

Figure 10 • Crystal Clock Option

8.2.2 25 MHz Reference Clock Option

A 25 MHz reference clock can be connected to XTAL1, with XTAL2 left floating. The OSCEN pin and the PLLMODE pin can be left floating. See the following figure.

Figure 11 • 25MHz Reference Clock Option

8.2.3 125 MHz Reference Clock Option

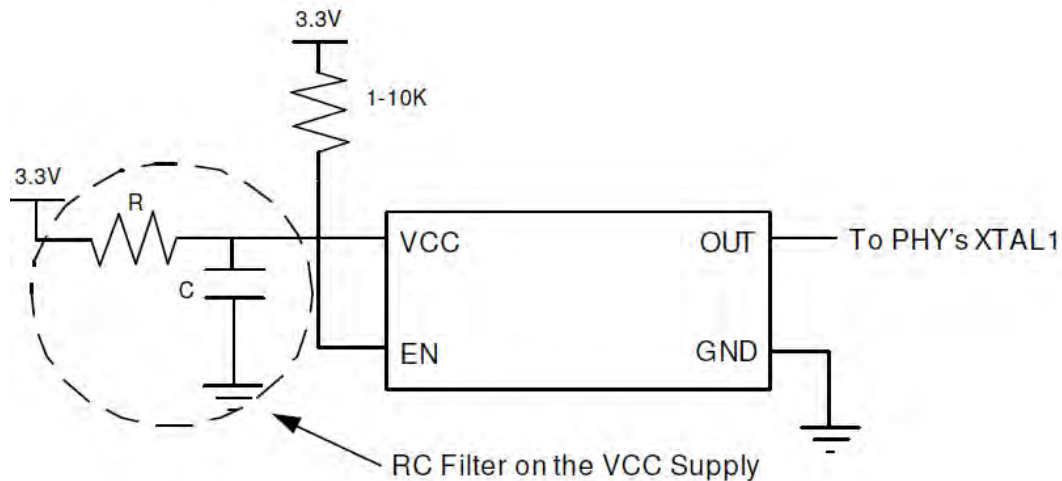
A 125 MHz reference clock can be connected to XTAL1, with XTAL2 left floating. The OSCEN pin can be left floating and the PLLMODE pin will need to be pulled high. Refer to following figure.

Figure 12 • 125MHz Reference Clock Option

8.2.4 Clock Power Supply Filtering

If using a 25 MHz or a 125 MHz 4-pin oscillator with a VCC pin, to avoid having power supply switching noise from coupling into the PHY, it is recommended an RC filter be implemented. The filter should be set to filter out the frequency of the supply's switching regulation frequency.

Figure 13 • Clock Power Supply Filtering



For example, for a supply with a switching frequency of 350 kHz, use an R value = 2.2 P and a C value = 11 μ F.

8.3 CLKOUT pin

The VSC8664 provides a selectable 125 MHz or 156.25 MHz clock out reference. The purpose of this pin is to drive MAC logic that requires an additional 125 MHz or 156.25 MHz clock source. The clock is active only if the NRESET pin is de-asserted. If not used, then set this pin to be disabled (MII Register 18.0 = 1) to avoid potential EMI issues associated with having an un-terminated output driver. This clock pin is also derived from the internal PLL of the VSC8664 and therefore is not advisable to be used to clock other devices that have internal PLLs.

8.4 Serial Management Interface (SMI)

The VSC8664 uses MDC and MDIO pins as a management interface as defined by the IEEE 802.3 standard. The MDIO pin is an open-drain signal and requires an external pull-up resistor. Only a single pull-up resistor is needed for the system, regardless of the number of devices. The pull-up resistor for the MDIO pin must be chosen to match the characteristics of the system. Of critical importance is the rise time needed to charge the total capacitive load on the MDIO pin up to a logic '1' through the pull-up resistor. This time constant is defined simply as:

$$\tau = R_{pu}C_{total}$$

Therefore, as more devices are added to the bus, the rise time increases due to the increased bus capacitance. In order to lower the rise time, a smaller resistor value must be used. However, if too small of a value is used, devices will be unable to transition the bus to logic '0'. This occurs when the current sinking capability of the pins in a logic '0' state is exceeded. For the VSC8664, the MDIO input capacitance is approximately 5 pF, and the maximum current sinking capacity is 10 mA.

Typical values are listed as follows:

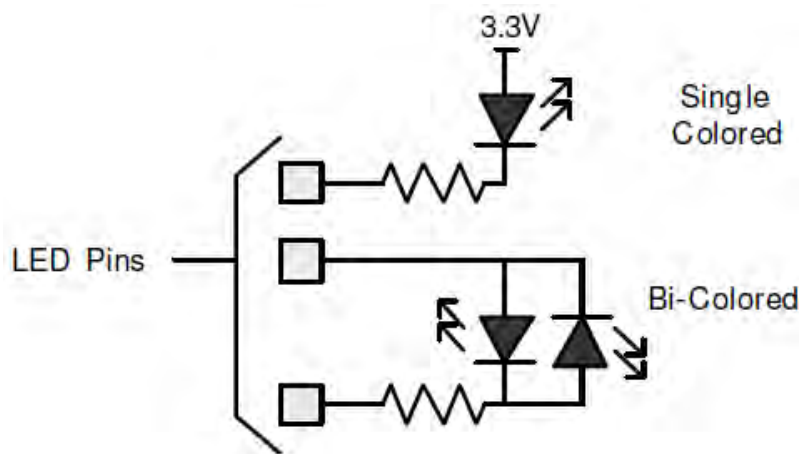
- For MDC frequencies of 2.5 MHz and below, a 2 kP pull-up resistor should be acceptable for most applications. This assumes the input capacitance of each device is between 5 pF–10 pF and that each device can sink at least 1.65 mA of current from each of their MDIO pins.

- For faster MDC frequencies (>2.5 MHz), a smaller pull-up is necessary. The smallest recommended pull-up resistor for use with the VSC8664 is 470 Ω .

8.5 LEDs

Each VSC8664 PHY port can support up to four single-colored LEDs and two bi-colored LEDs. Each LED pin sinks current when an indication is present and deasserts when inactive. By design, each LED pin can also drive current when not active. This is very useful in the case for bi-colored LEDs. Each LED pin in the VSC8664 can be designated to indicate any of the possible LED status signals thereby further simplifying the overall design.

Figure 14 • LED Configurations



8.6 GPIO Pins

GPIO pins on the VSC8664 are provided to allow a user to eliminate unnecessary glue logic for lower speed external control and status pins of support devices such as Power Over Ethernet Controllers and SFPs. In addition unused LED pins can be used as general-purpose outputs as well.

8.7 Optional CMODE Interface

The CMODE pins are provided to ease initialization of the VSC8664 especially for systems that have limited software capability. This feature is optional and does not require implementation, which allows for additional BOM cost savings. The exception is the case with CMODE where the PHY_ADDR and PHY_REVERSAL must be configured.

9 Bringing Up the Device

9.1 Reset Sequence

The following events occur in the following order when the VSC8664 is brought out of reset. This is triggered by a low-to-high transition of the NRESET pin.

1. Values for the PLLMODE, OSCEN, and CMODE pins are latched asynchronously immediately out of reset.
2. Approximately <11 ms after reset, the analog reference voltages and current stabilize. This is seen on the REF_REXT and REF_FILT pins.
3. Once a stable analog reference is established, the internal PLL will require 50 μ s to lock. The PLL provides the device its internal clocks.
4. With a locked PLL, the analog-to-digital blocks are calibrated. Usually requires approximately 2 ms.
5. Once the ADC is calibrated, the CLKOUT pin is activated.
6. The device is now in normal operation and its MDC and MDIO pins are operational.

Important Note: Since the values of the PLLMODE, OSCEN, and CMODE pins are latched on the rising edge of the NRESET pin, it is required that the power supply is stable before the rising edge of NRESET. Therefore, if NRESET is tied directly to logic high on the PCB, the VSC8664 will behave unpredictably. If a design requires the NRESET pin to remain high at all times, a small RC circuit can be added to this line to provide the necessary delay.

9.2 Minimum Firmware Settings

The following describes the minimum register settings that are needed to configure the PHY to normal operation. This assumes changes that are made from the default settings that are set during reset. Also to decrease configuration time period the broadcast write bit (MII Register 22.0) can be set that allows writing to all PHYs from one location. This can be the first register bit set.

1. If MAC interface configuration changes are needed such as disabling SGMII auto-negotiation, the first register writes should be to Register 23.
2. If the MAC interface settings in Register 23 are changed, then the next step is to perform a Software Reset (MII Register 0.15 = 1).
3. After the reset completes any required initialization scripts are to be written at this time.
4. At this step other user-defined configuration settings can be applied such as LED changes.

**Microsemi Headquarters**

One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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