AT88RF1354 Command

Reference Guide

5150B—RFID—4/09

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Section 1
Introduction

Features

- AT88RF1354 Instruction Set
- AT88RF1354 Register Definitions
- Initialization Procedure

Description

This document describes the instruction set and register definitions for the AT88RF1354 13.56 MHz ISOI/IEC 14443 Type B Reader IC. Device initialization examples are included for reference by the software developer or embedded systems programmer using this RF reader.

This specification is formatted as a reference document, with each command description and register definition on a separate page. The related definitions and data field requirements are located on the same page for ease of use.

1.1 Product Description

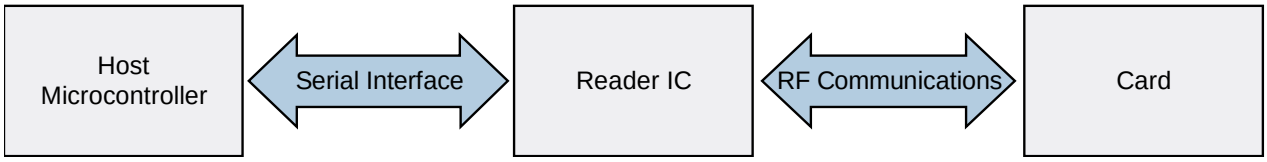
The AT88RF1354 is a smart, high performance ISO/IEC 14443 Type B RF Reader IC. The AT88RF1354 communicates with RFID Transponders or Contactless Smartcards using the industry standard ISO/IEC 14443-2 Type B signal modulation scheme and ISO/IEC 14443-3 Type B frame format. Data is exchanged half duplex at a 106k bit per second rate. A two byte CRC_B provides communication error detection capability.

The AT88RF1354 is compatible with 3.3 V and 5 V host microcontrollers with two-wire or SPI serial interfaces. In two-wire interface mode the AT88RF1354 operates as a TWI slave and requires four microcontroller pins for data communication and handshaking. In SPI interface mode the AT88RF1354 operates as a mode 0 SPI slave and requires six microcontroller pins for data communication and handshaking.

To communicate with an RFID transponder the host microcontroller sends a data packet for transmission over the RF communications channel, and receives the response data packet that is received from the transponder over the RF communications channel. AT88RF1354 performs all RF communication packet formatting, decoding, and communication error checking. The host microcontroller is not burdened with RF encoding, timing, or protocol functions since these tasks are all performed by the AT88RF1354.

1.2 System Diagram

*Figure 1. Communications in an **RFID** System*



1.3 Scope

This *AT88RF1354 Command Reference Guide* document includes all command and register information for the AT88RF1354 RF Reader. The RF Reader electrical specifications are described in the *AT88RF1354 Specification* document. Reference Designs and additional technical information is available in *AT88RF1354 Application Notes and Other Documents*. See www.atmel.com

1.4 Conventions

ISO/IEC 14443 nomenclature is used in this document where applicable. The following terms and abbreviations are utilized throughout this document. Additional terms are defined in the section in which they are used.

Card: A Contactless Smart Card or RFID Tag in proximity to the reader antenna.

Host: The microcontroller connected to the serial interface of the reader IC.

PCD: Proximity Coupling Device – is the host and reader with antenna.

PICC: Proximity Integrated Circuit Card – is the tag/card containing an IC and antenna.

Reader: The AT88RF1354 Integrated Circuit with loop antenna and associated circuitry

RFU: Reserved for Future Use – is any feature, memory location, or bit that is held as reserved for future use by the ISO standards committee or by Atmel.

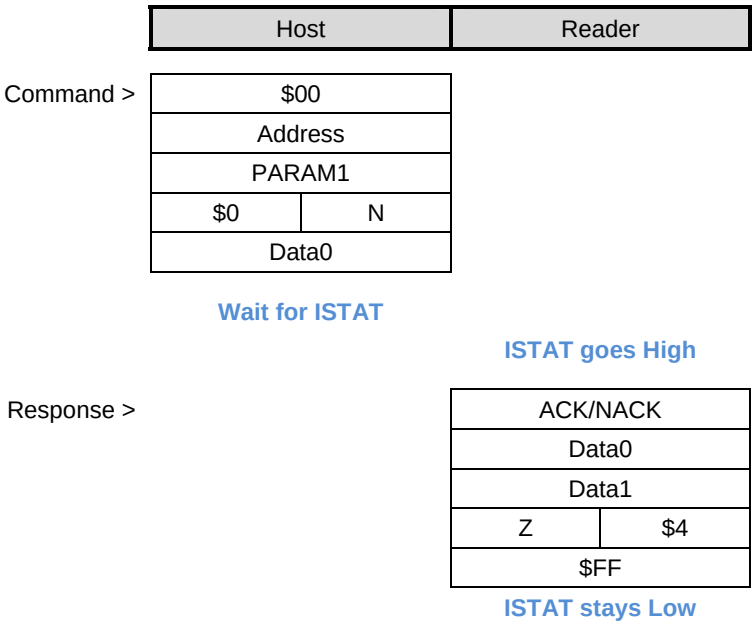
$ xx: Hexadecimal Number – denotes a hex number “xx” (Most Significant Bit on left).

xxxx b: Binary Number – denotes a binary number “xxxx” (Most Significant Bit on left).

See Atmel Application Note *Understanding the Requirements of ISO/IEC 14443 for Type B Proximity Contactless Identification Cards* at www.atmel.com for detailed information regarding the ISO/IEC 14443 RF communication protocol.

1.4.1 SPI Command Format

Figure 2. Serial Communications with the SPI Interface

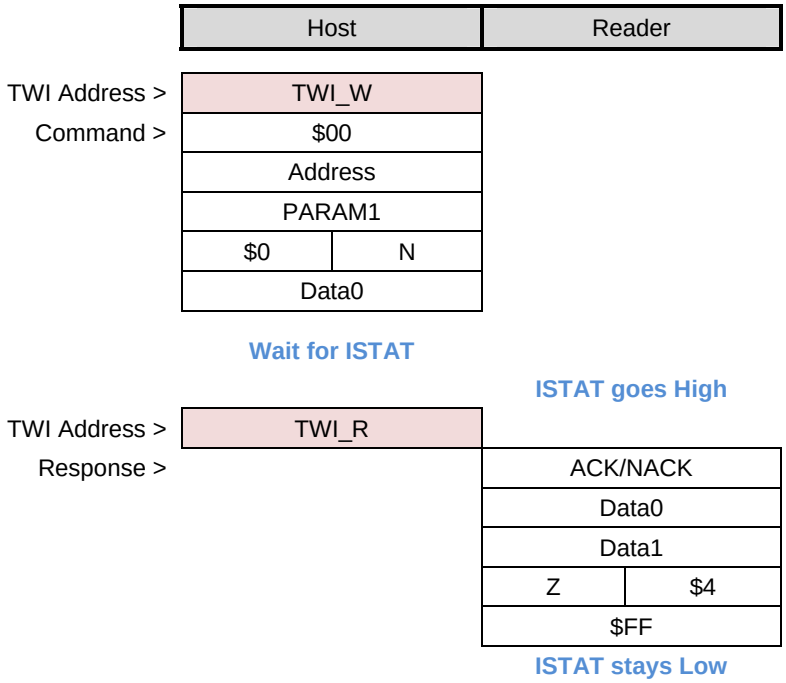


Each SPI serial interface command / response exchange between the Host microcontroller and AT88RF1354 is formatted as shown above in Figure 2. The bytes are shown in the order in which they are transmitted, with Host transmissions in the left column, and Reader transmissions in the right column. Blue text is used for notes regarding the ISTAT serial interface handshaking signal.

Each byte contains one or more fields as indicated by lines drawn vertically within the byte. The field in the left half of the byte is the upper nibble of the byte, and the field to the right is the lower nibble of the byte. In Figure 2, four fields contain values ($00, $0, $4, $FF), eight fields contain field names (“Address”, “PARAM1”, “N”, “Data0”, “ACK/NACK” “Data1”, “Z”). Any field name containing the word “register” indicates an IC register value.

1.4.2 TWI Command Format

Figure 3. Serial Communications with the TWI Interface



Each TWI serial interface command / response exchange between the Host microcontroller and AT88RF1354 is formatted as shown in Figure 3. The bytes are shown in the order in which they are transmitted, with Host transmissions in the left column, and Reader transmissions in the right column. Blue text is used for notes regarding the ISTAT serial interface handshaking signal.

Each byte contains one or more fields as indicated by lines drawn vertically within the byte. The field in the left half of the byte is the upper nibble of the byte, and the field to the right is the lower nibble of the byte. In Figure 3, four fields contain values ($00, $0, $4, $FF), ten fields contain field names (“TWI_W”, “Address”, “PARAM1”, “N”, “Data0”, “TWI_R”, “ACK/NACK” “Data1”, “Z”). Any field name containing the word “register” indicates an IC register value.

The “TWI_W” and “TWI_R” fields contain the Two Wire Interface device address of the AT88RF1354 Reader with either the read (TWI_R) or write (TWI_W) bit set. Note that TWI ACK polling is not supported by the AT88RF1354.

TWI Device Address

The TWI device address is selected with the ADDR address select pin of the AT88RF1354.

Table 1. TWI Device Address

ADDR Pin	TWI Device Address							TWI_R	TWI_W
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Vss	0	1	0	1	0	0	0	$51	$50
Vcc	1	1	0	1	0	1	0	$D5	$D4
All other values are NOT supported									

1.4.3 ACK/NACK Response Byte

The first byte of each response is usually an ACK/NACK byte which indicates if the requested operation succeeded or failed. The bit definitions for the ACK/NACK byte are shown in Figure 4 and Figure 5. This response byte contains 6 bits from the Error Register, and 2 bits which indicate the success or failure of the requested operation. 01b in the least significant bits is an ACK, indicating success. 10b in the least significant bits is a NACK, indicating failure. The contents of the error register are not relevant to non-RF commands and can be ignored.

Figure 4. ACK/NACK Byte Format for ACK Response

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRC	FRAME	BYTE	TIME	COL	SPE	0 b	1 b
Error Register Bits						ACK	

Figure 5. ACK/NACK Byte Format for NACK Response

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRC	FRAME	BYTE	TIME	COL	SPE	1 b	0 b
Error Register Bits						NACK	

The three RF communication commands Poll Continuous, Poll Single, and TX Data return the Error Register contents in the first byte of the response. Figure 6 shows the Error Register format.

Figure 6. Error Register Format in RF Command Responses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRC	FRAME	BYTE	TIME	COL	SPE	0 b	0 b

Section 2
Instruction Set

Table 2. Instruction Set Sorted by Command Name

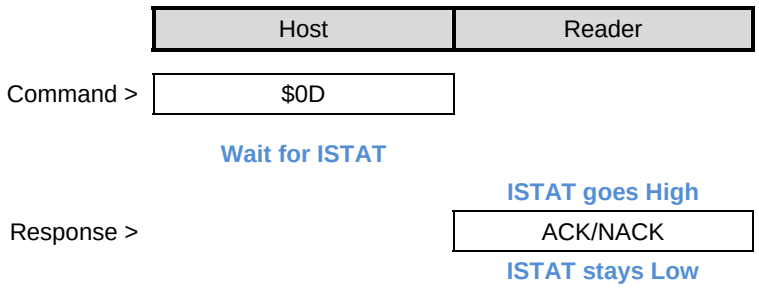
Command Name	Description	Code
Abort	Exit Command in Progress	$0D
Clear	Exit Command in Progress, Clear Buffer, Turn RF OFF	$0E
Poll Continuous	Poll Continuously for Type B PICCs	$02
Poll Single	Poll Once for Type B PICCs	$01
Read Buffer	Read Data Buffer	$08
Read Register	Read Configuration Register	$07
RF OFF	Turn Off 13.56 MHz RF Field	$0B
RF ON	Turn On 13.56 MHz RF Field	$0A
Sleep	Activate Standby Mode	$0C
TX Data	Transmit Data to PICC and Receive the Response	$03
Write Buffer	Write Data Buffer	$09
Write Register	Write Configuration Register	$06
All other command code values are NOT supported		

Commands in the following sections are listed in alphabetical order.

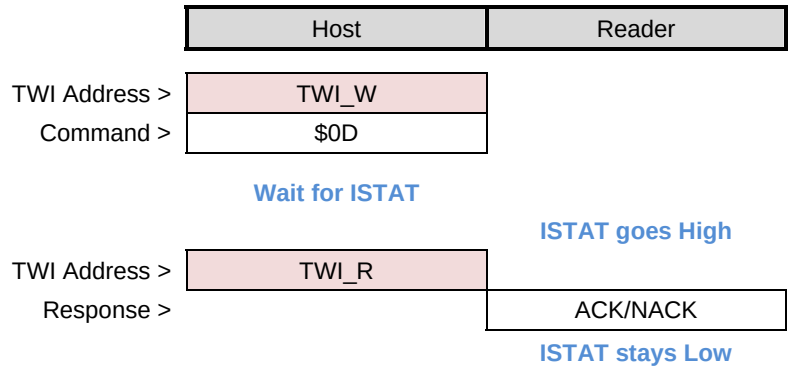
2.1 Abort Command

This command aborts a command in progress and places the reader in the idle state.

2.1.1 SPI Command Format



2.1.2 TWI Command Format



2.1.3 Operation

The Abort command stops a command operation in progress. The contents of the RAM buffer and registers are not modified by the Abort command.

2.1.4 Command Field Description

There are no field options in this command.

2.1.5 Response Field Descriptions

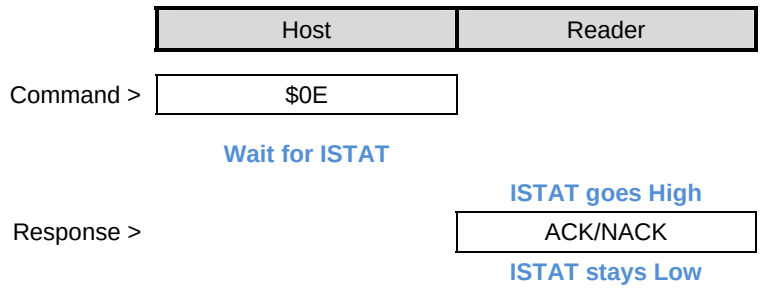
ACK: Acknowledge — the command executed correctly

NACK: Not Acknowledge — the command did not execute correctly

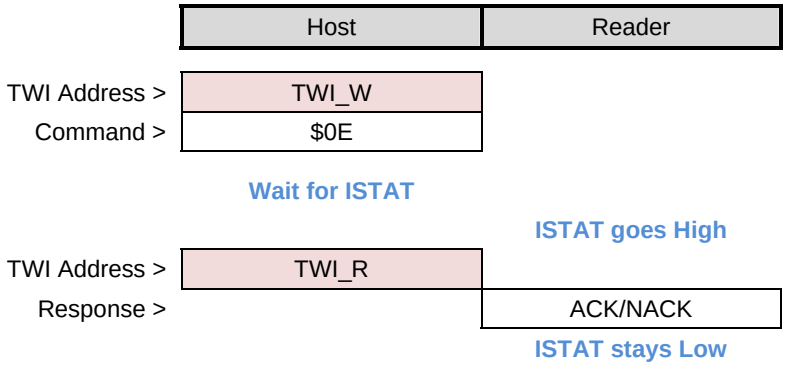
2.2 Clear Command [$0E]

This command aborts a command in progress, turns off the RF field, clears the RAM buffer, and places the reader in the idle state.

2.2.1 SPI Command Format



2.2.2 TWI Command Format



2.2.3 Operation

The Clear command stops a command in progress, turns off the RF field, and clears the RAM buffer. The contents of the error register are reset by the Clear command, the contents of the other registers are unchanged.

2.2.4 Command Field Descriptions

There are no field options in this command.

2.2.5 Response Field Descriptions

ACK: Acknowledge — the command executed correctly

NACK: Not Acknowledge — the command did not execute correctly

2.3 Poll Continuous Command [$02]

This command performs multiple Type B polling sequences to detect cards near the antenna.

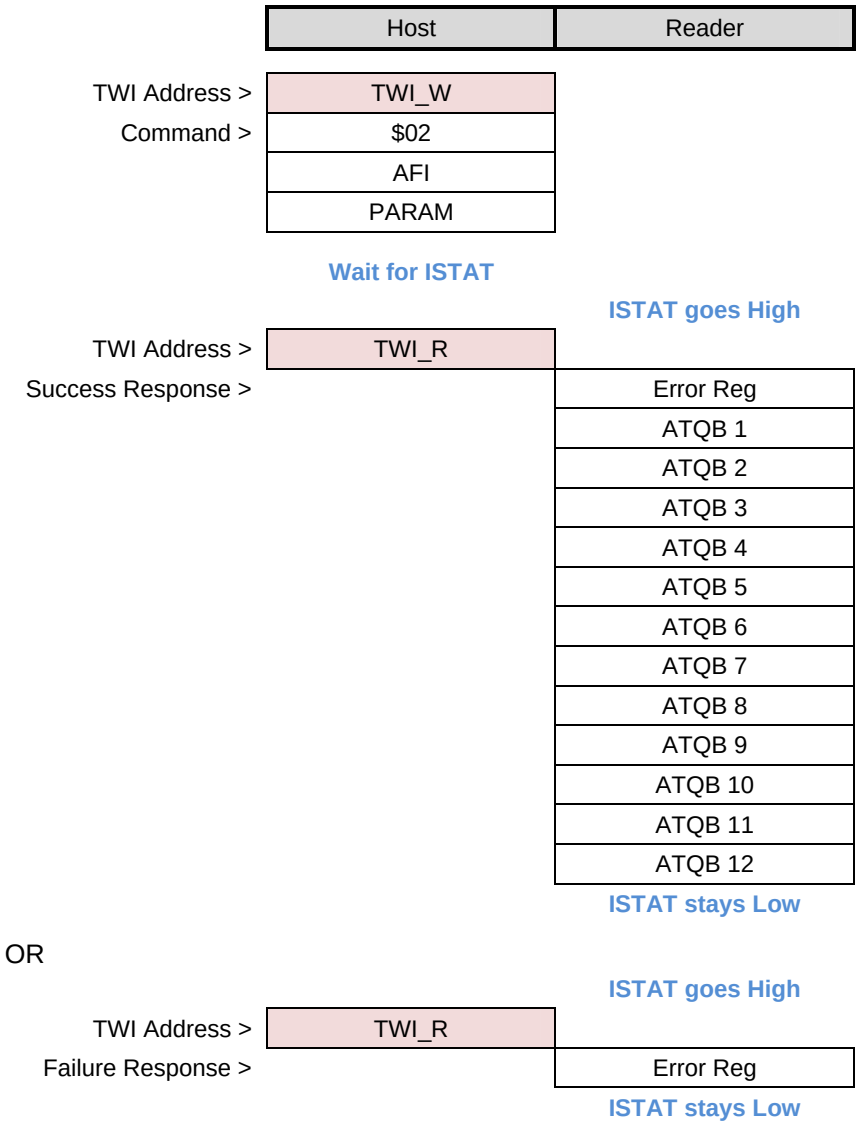
The first response is returned to the host. In the event a card response containing a communication error is received, then an error code is returned. If no response is detected, then polling continues until an Abort command is sent by the host.

The optional Smart Poll mode modifies the polling operation to include error tolerance. In Smart Poll mode polling continues until an error free card response is received.

2.3.1 SPI Command Format

	Host	Reader
Command >	$02	
	AFI	
	PARAM	
	Wait for ISTAT	
		ISTAT goes High
Success Response >		Error Reg
		ATQB 1
		ATQB 2
		ATQB 3
		ATQB 4
		ATQB 5
		ATQB 6
		ATQB 7
		ATQB 8
		ATQB 9
		ATQB 10
		ATQB 11
		ATQB 12
		ISTAT stays Low
OR		
		ISTAT goes High
Failure Response >		Error Reg
		ISTAT stays Low

2.3.2 TWI Command Format



2.3.3 Operation

The functionality of the Poll Continuous command is identical to the Poll Single command, except that after the final Slot-MARKER is sent, if no card response is received, the reader chip repeats the polling procedure. The Poll Continuous command is like an infinite loop of Poll Single commands that is broken when a card response (good or bad) is received.

This command performs multiple polling sequences with “N” slots using the ISO/IEC14443-3 Type B commands REQB, WUPB, and Slot-MARKER. The CPR0 default Communication Protocol settings are used by this command.

A polling sequence consists of either an REQB or WUPB command, followed by the number of Slot-MARKER commands indicated by “N”. When a response is received, then the polling sequence is stopped and the response is returned to the host. When a communication error is detected, then the polling sequence is stopped and an error code is returned to the host.

2.3.4 Smart Poll Mode Operation

Smart Poll mode is enabled by sending the Poll Continuous command with N = 111b. In the Smart Poll mode, the reader will continually send REQB/WUPB with N = 000b until it receives a card response. If this response is valid, it will return the response to the host. If the card response generates a communication error, the reader assumes that there was a collision. It will then send the next REQB/WUPB with N = 001b, and if there is no valid card response it will send Slot-MARKER for slot two.

If there is no response from a card in either slot, then the reader returns to polling with N = 000b. If there is an error free card response, then it will be returned to the host. If there is another collision and no valid response, however, N will again be incremented, and the reader will send the correct sequence of REQB/WUPB and Slot-MARKERs. In the case where Smart Poll mode reaches 16 slots and only collisions are detected, then polling is stopped, and a Smart Poll error code is returned to the host. If no error-free card response is detected, then polling continues until an Abort command is sent by the host.

2.3.5 Command Field Descriptions

AFI: AFI code to be sent by reader in the polling command. To search for all cards set AFI = $00.

PARAM: Contains Polling command control fields: R/W and N.

Figure 7. PARAM Byte Field Definitions. Poll Continuous Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU				R/W	N		

R/W: Polling command

Table 3. REQB/WUPB Selection Bit Coding in the PARAM Byte.

Bit 3	Command
0	REQB
1	WUPB

N: Code for number of slots to poll for cards

Table 4. Coding of N, number of slots to poll.

Bit 2	Bit 1	Bit 0	N
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	*RFU*
1	1	0	*RFU*
1	1	1	Smart

RFU: Reserved for Future Use. All RFU bits must contain 0 b.

2.3.6 Response Field Descriptions

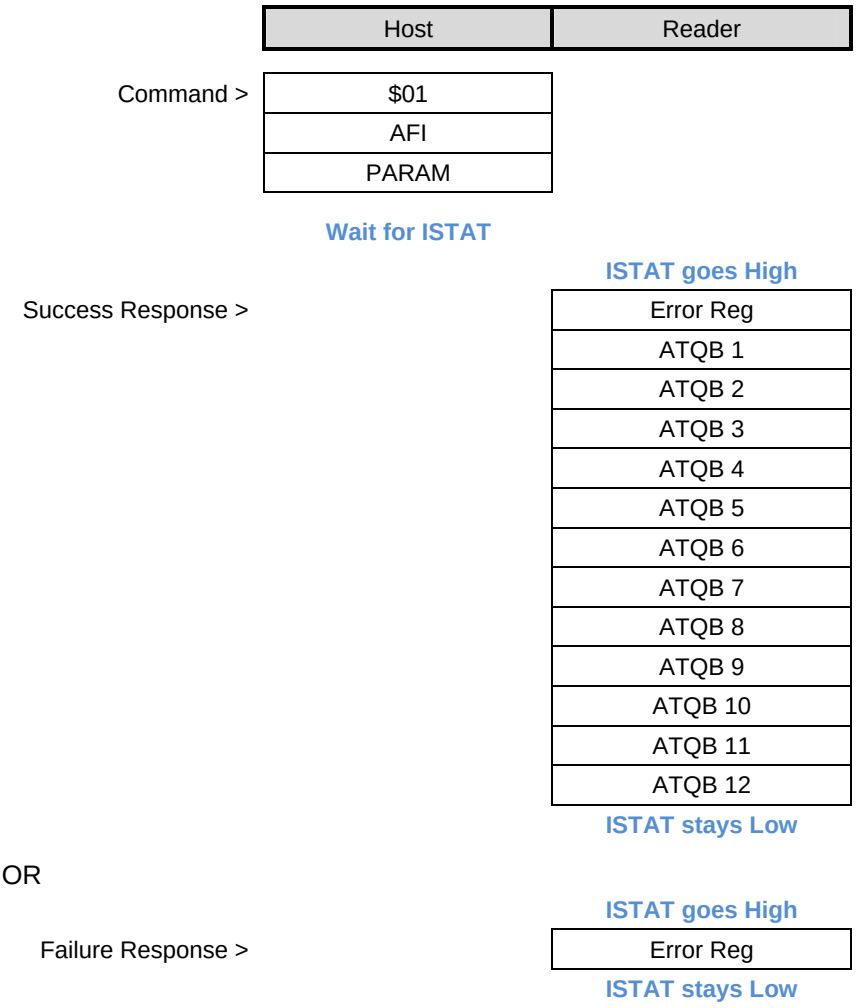
Error Register Contents: $00 indicates no errors.

ATQB: Answer to the polling command received from the PICC.

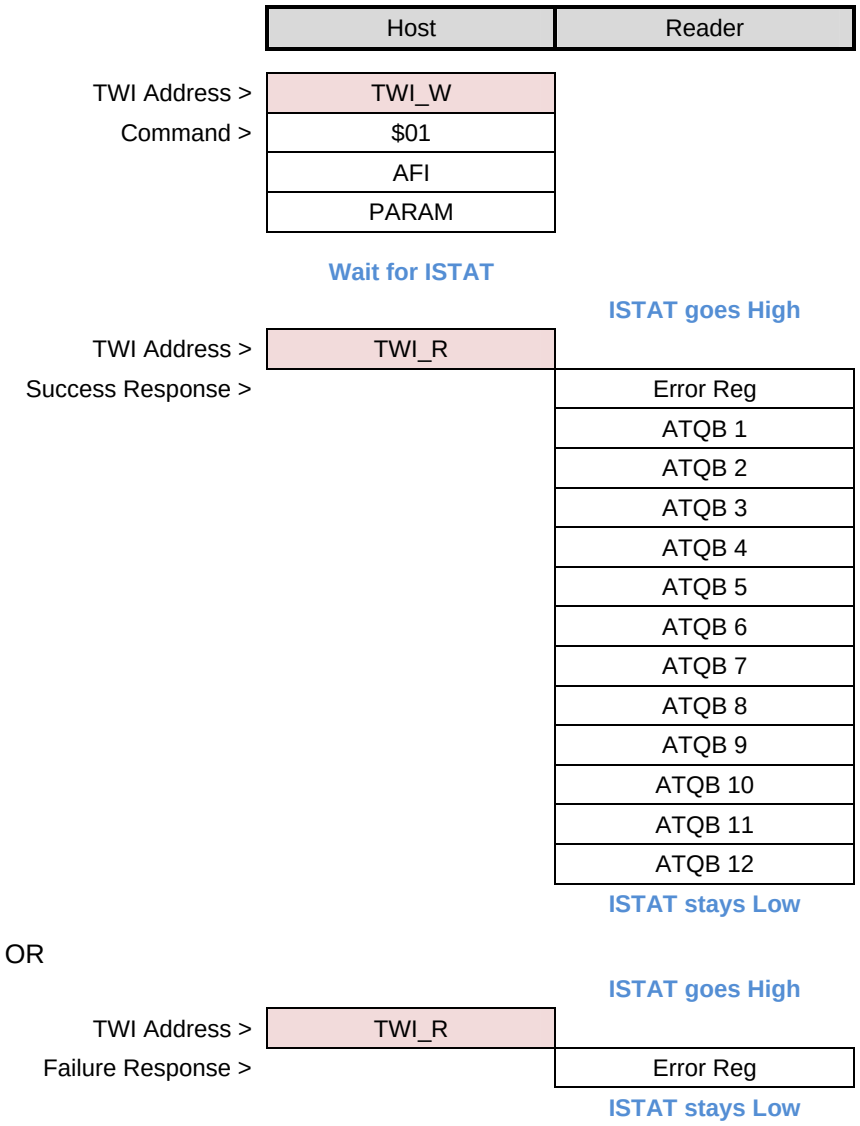
2.4 Poll Single Command [$01]

This command performs a single Type B polling sequence to detect cards near the antenna. The first response is returned to the host. In the event no error free response is detected, then an error code is returned.

2.4.1 SPI Command Format



2.4.2 TWI Command Format



2.4.3 Operation

This command performs one polling sequence with “N” slots using the ISO/IEC14443-3 Type B commands REQB, WUPB, and Slot-MARKER. The CPR0 default Communication Protocol settings are used by this command.

A polling sequence consists of either an REQB or WUPB command, followed by the number of Slot-MARKER commands indicated by “N”. When a card response not containing a CRC error is received, then the polling sequence is stopped and the response is returned to the host.

2.4.4 Command Field Descriptions

AFI: AFI code to be sent by reader in polling command. To search for all Type B cards set AFI = $00.

PARAM: Contains Polling command control fields: R/W and N.

Figure 8. PARAM Byte Field Definitions. Poll Single Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU				R/W	N		

R/W: Polling command.

Table 5. REQB/WUPB Selection Bit Coding in the PARAM Byte.

Bit 3	Command
0	REQB
1	WUPB

N: Code for number of slots to poll for cards

Table 6. Coding of N, number of slots to poll.

Bit 2	Bit 1	Bit 0	N
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	*RFU*
1	1	0	*RFU*
1	1	1	*RFU*

RFU: Reserved for Future Use. All RFU bits must contain 0 b.

2.4.5 Response Field Descriptions

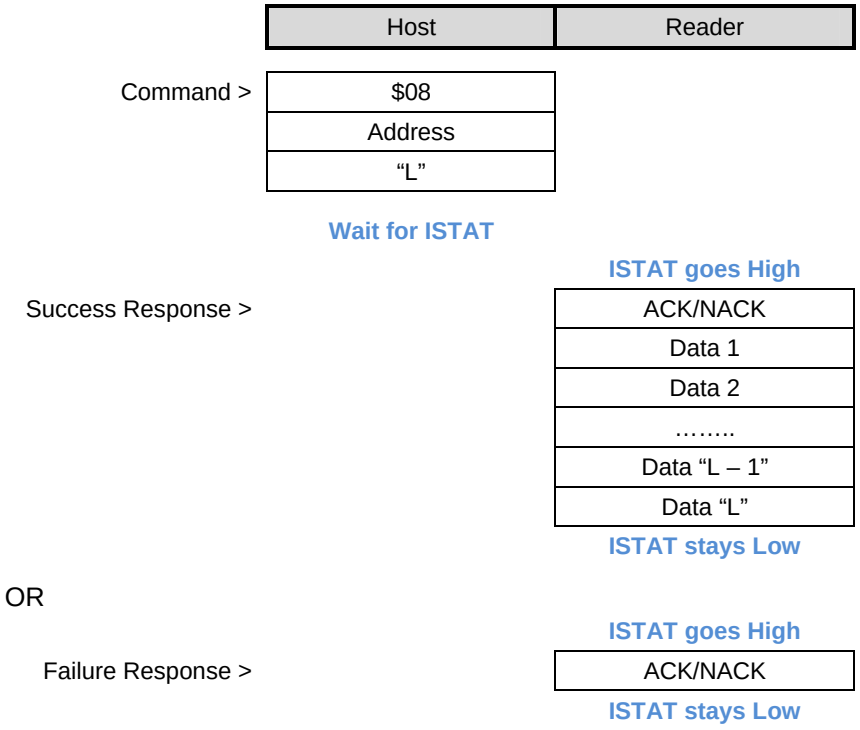
Error Register Contents: $00 indicates no errors.

ATQB: Answer to the polling command received from the PICC.

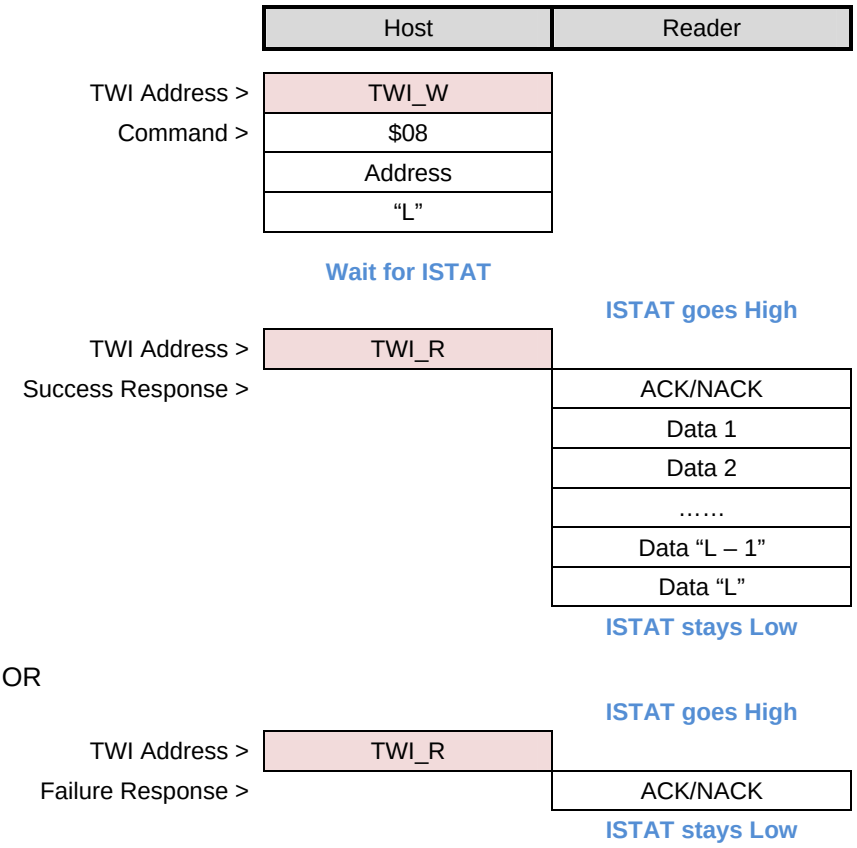
2.5 Read Buffer Command [$08]

This command reads data from the RAM Buffer of the reader.

2.5.1 SPI Command Format



2.5.2 TWI Command Format



2.5.3 Operation

Read the internal 256 byte RAM buffer starting at the Address specified.

2.5.4 Command Field Descriptions

Address: Starting Address

L: Length of Data in bytes, except $00 is 256 bytes

2.5.5 Response Field Descriptions

ACK: Acknowledge — the command executed correctly.

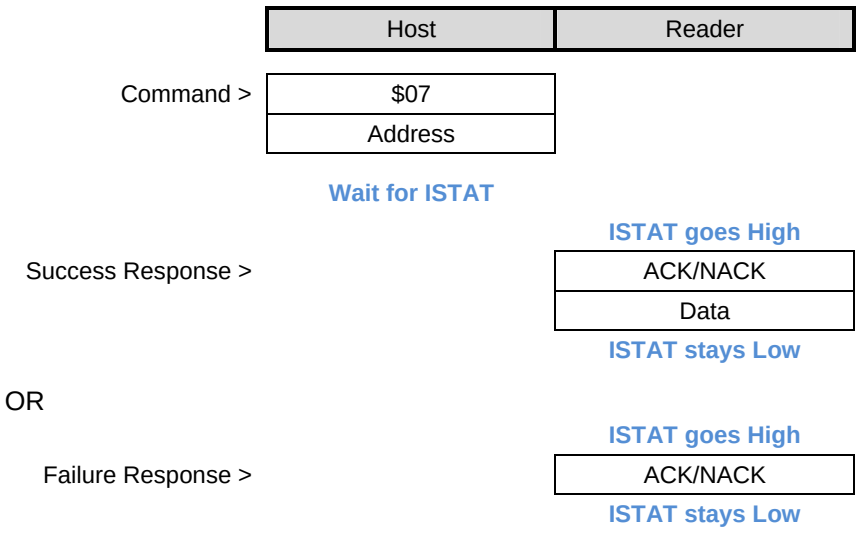
NACK: Not Acknowledge — the command did not execute correctly.

Data: Contents of buffer, lowest address first.

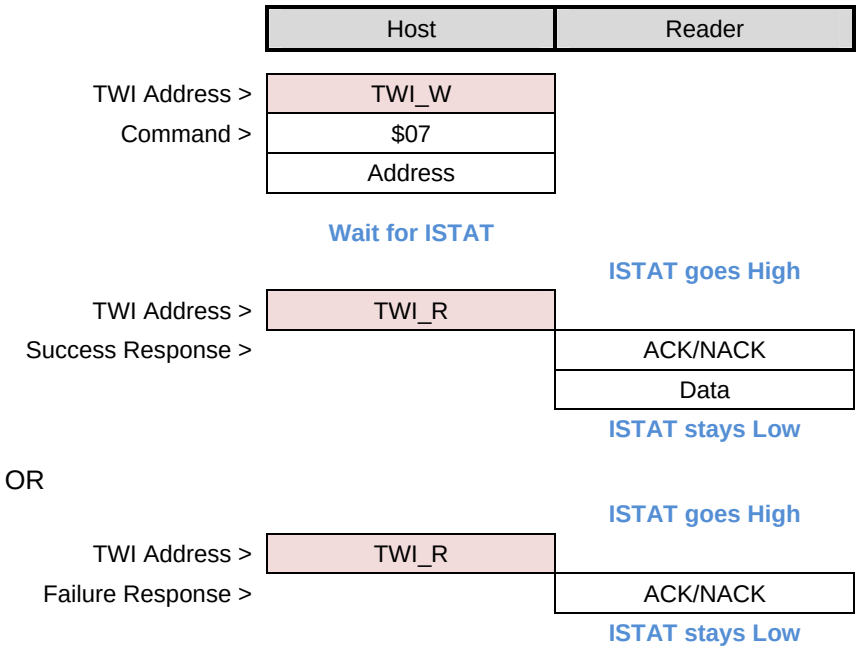
2.6 Read Register Command [$07]

This command reads the contents of the specified configuration register.

2.6.1 SPI Command Format



2.6.2 TWI Command Format



2.6.3 Operation

Read a reader configuration register.

2.6.4 Command Field Descriptions

Address: Register address

2.6.5 Response Field Descriptions

ACK: Acknowledge — the command executed correctly.

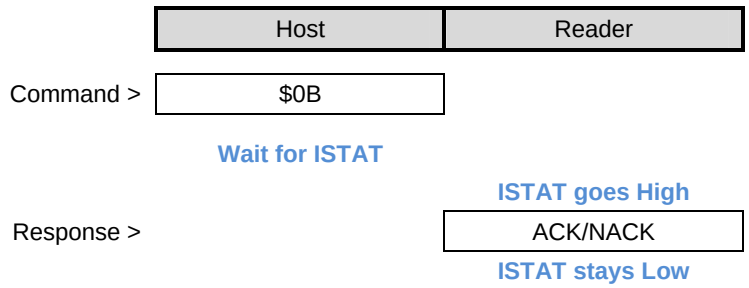
NACK: Not Acknowledge — the command did not execute correctly.

Data: Contents of the register.

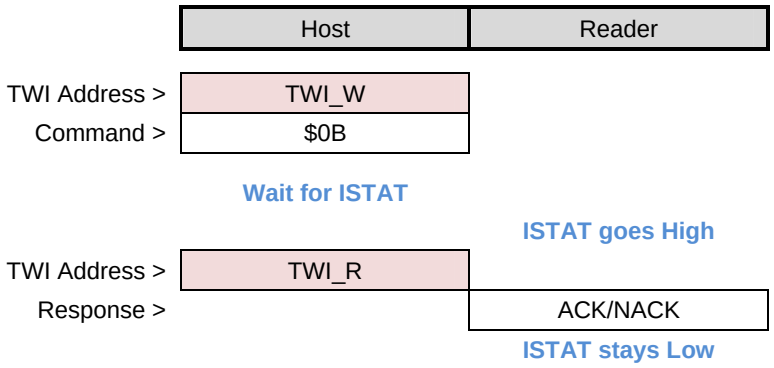
2.7 RF OFF Command [$0B]

This command turns the 13.56 MHz RF field off.

2.7.1 SPI Command Format



2.7.2 TWI Command Format



2.7.3 Operation

Turns the RF field off.

2.7.4 Command Field Descriptions

There are no field options in this command.

2.7.5 Response Field Descriptions

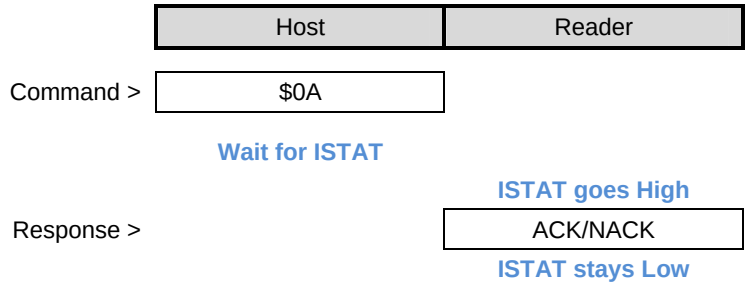
ACK: Acknowledge — the command executed correctly

NACK: Not Acknowledge — the command did not execute correctly

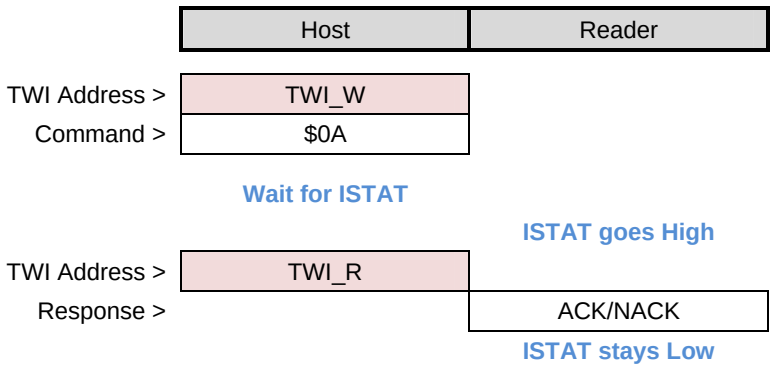
2.8 RF ON Command [$0A]

This command turns the 13.56 MHz RF field on.

2.8.1 SPI Command Format



2.8.2 TWI Command Format



2.8.3 Operation

Turns the RF field on.

2.8.4 Command Field Descriptions

There are no field options in this command.

2.8.5 Response Field Descriptions

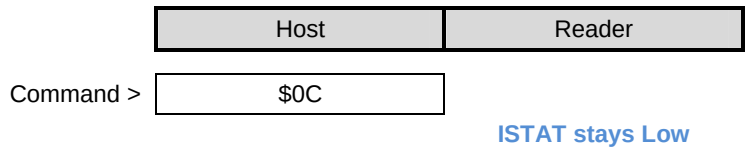
ACK: Acknowledge — the command executed correctly.

NACK: Not Acknowledge — the command did not execute correctly

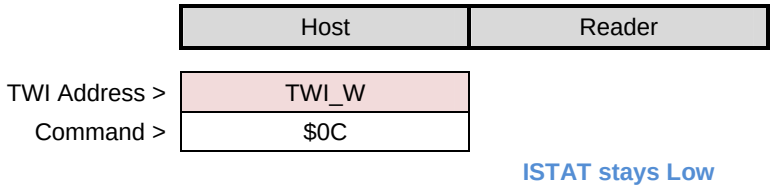
2.9 Sleep Command [$0C]

This command activates the standby mode.

2.9.1 SPI Command Format



2.9.2 TWI Command Format



2.9.3 Operation

The Sleep command places the reader into one of several standby modes. The reader will remain in this mode until the SCK serial interface input transitions from low to high. Sending any command from the host causes the reader to exit sleep mode. Any activity on the serial interface bus will cause the IC to exit sleep mode.

The Sleep command should only be sent when the 13.56 MHz RF field is off. When the Sleep command is received, the reader internal circuitry is placed in standby and all internal clocks are stopped. The PLL Configuration Register ($0D) settings determine if the PLL and crystal oscillator are disabled in standby mode.

WARNING: In TWI mode this command must be sent without a stop bit. If a stop bit is sent, the reader will immediately exit standby mode.

2.9.4 Command Field Descriptions

There are no field options in this command.

2.9.5 Response Field Descriptions

ACK: Acknowledge — the command executed correctly.

NACK: Not Acknowledge — the command did not execute correctly.

2.10 TX Data Command [$03]

This command transmits data from the reader and waits for a response.

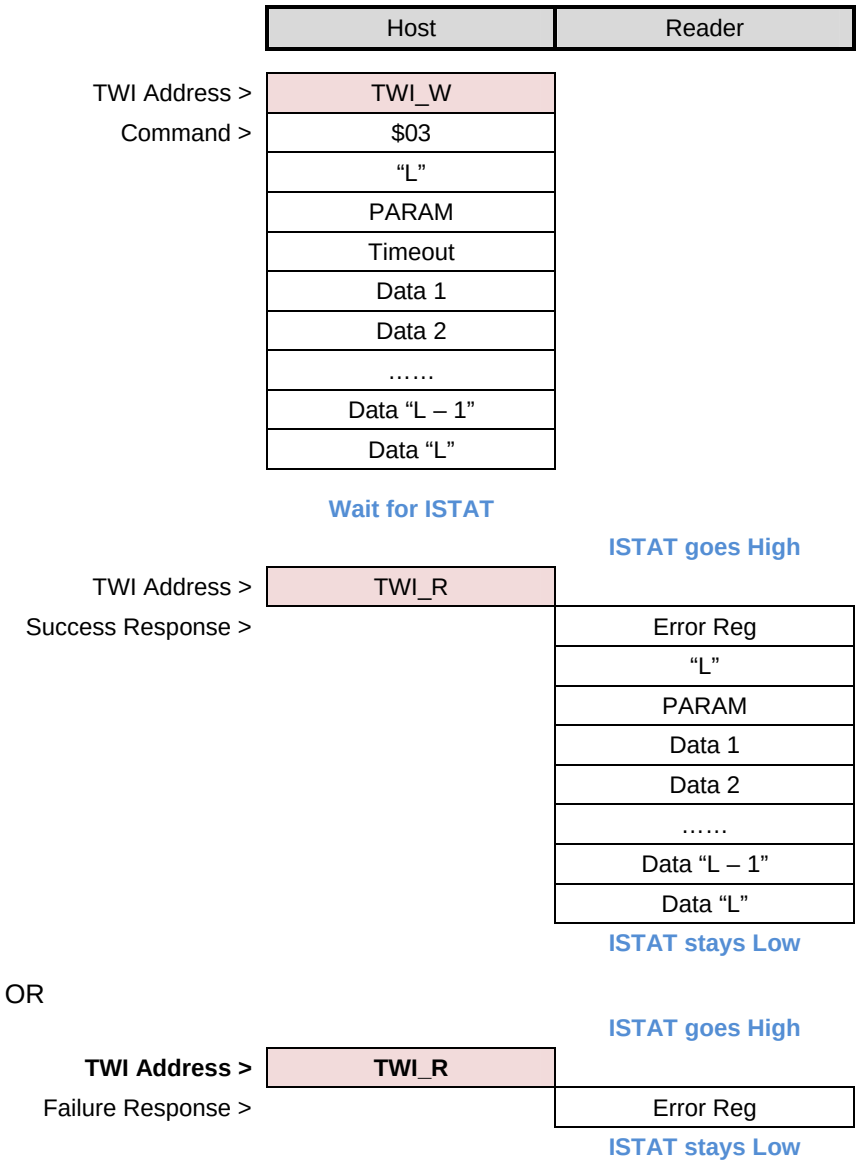
2.10.1 SPI Command Format

	Host	Reader
Command >	$03	
	"L"	
	PARAM	
	Timeout	
	Data 1	
	Data 2	
	……	
	Data "L – 1"	
	Data "L"	
	Wait for ISTAT	
		ISTAT goes High
Success Response >		Error Reg
		"L"
		PARAM
		Data 1
		Data 2
		……
		Data "L – 1"
		Data "L"
		ISTAT stays Low

OR

		ISTAT goes High
Failure Response >		Error Reg
		ISTAT stays Low

2.10.2 TWI Command Format



2.10.3 Operation

Using the communication settings in the specified Communication Protocol Register, this command transmits the data received in the data field. The reader waits for a response for the time specified. If no response is received before timeout, then a timeout error code is returned to the host.

2.10.4 Command Field Descriptions

L: Length of data in bytes, except $00 is 256 bytes.

PARAM: Contains the CPR and Length [2:0] fields.

Figure 9. PARAM Byte Field Definitions. TX Data Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Length [2:0]			0 b	0 b	CPR		

Length [2:0]: Length of additional data in bits for transmitting less than 8 bits.

CPR: Selects the Communication Protocol Register.

Table 7. Coding of CPR field in the PARAM Byte.

Command CPR			Communication Protocol Register
Bit 2	Bit 1	Bit 0	
0	0	0	CPR0
0	0	1	CPR1
0	1	0	CPR2
0	1	1	CPR3
1	0	0	CPR4
All Other Values Are NOT Supported			

Timeout: $00 selects FWI timeout using the specified CPR register. A non-zero value. In this field overrides the FWI timeout using the following formula:

Wait Time = 151 microseconds x Timeout

Data: Data transmitted to the PICC.

RFU: Reserved for Future Use. All RFU bits must contain 0 b.

2.10.5 Response Field Descriptions

Error Register: $00 indicates no errors.

PARAM: The PARAM field of the response is identical to the value received in the command.

Data: Data received from the PICC.

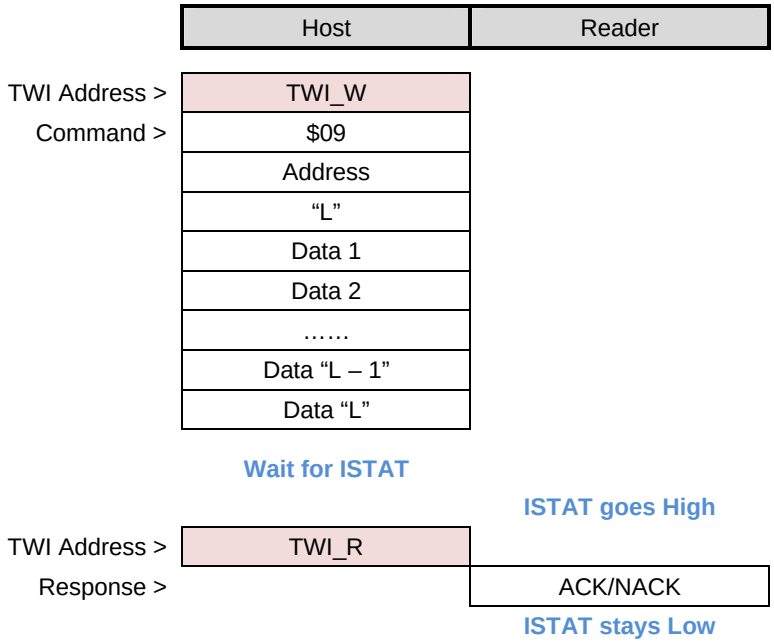
2.11 Write Buffer Command [$09]

This command writes data to the RAM buffer of the reader.

2.11.1 SPI Command Format

	Host	Reader
Command >	$09	
	Address	
	“L”	
	Data 1	
	Data 2	
	……	
	Data “L – 1”	
	Data “L”	
	Wait for ISTAT	
		ISTAT goes High
Response >		ACK/NACK
		ISTAT stays Low

2.11.2 TWI Command Format



2.11.3 Operation

Write the internal 256 byte RAM buffer starting at the Address specified.

2.11.4 Command Field Descriptions

Address: Starting Address

L: Length of Data in bytes, except $00 is 256 bytes

Data: Data to write, lowest address first.

2.11.5 Response Field Descriptions

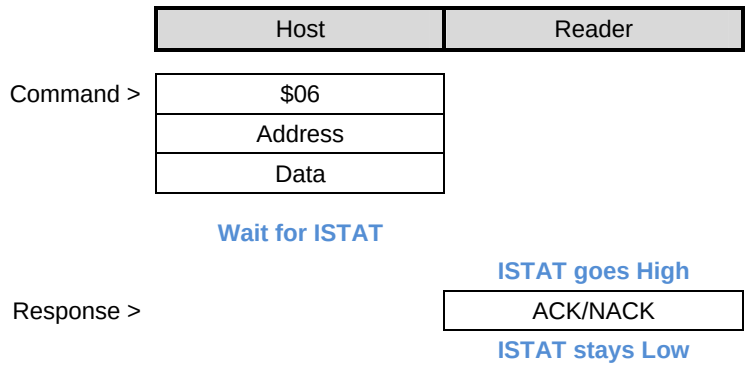
ACK: Acknowledge — the command executed correctly.

NACK: Not Acknowledge — the command did not execute correctly.

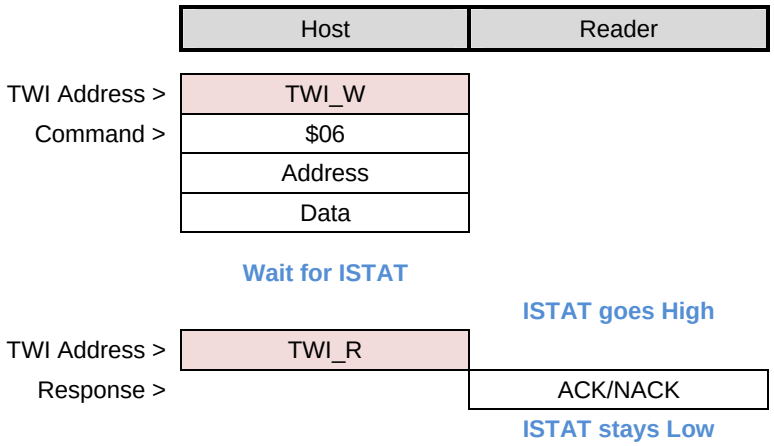
2.12 Write Register Command [$06]

This command writes a value to the specified configuration register of the reader.

2.12.1 SPI Command Format



2.12.2 TWI Command Format



2.12.3 Operation

Write a reader configuration register.

2.12.4 Command Field Descriptions

Address: Register address.

Data: Register data to write.

2.12.5 Response Field Descriptions

ACK: Acknowledge — the command executed correctly.

NACK: Not Acknowledge — the command did not execute correctly.

Section 3
Register Summary

Table 8. Register Set Sorted by Address

Register Name	Register Address	Description	Register Type
CPR0_L	$00	(Default) Communication Protocol Register 0 – Low Byte	Read—Only
CPR0_H	$01	(Default) Communication Protocol Register 0 – High Byte	Read—Only
CPR1_L	$02	Communication Protocol Register 1 – Low Byte [RFU]	Read / Write
CPR1_H	$03	Communication Protocol Register 1 – High Byte	Read / Write
CPR2_L	$04	Communication Protocol Register 2 – Low Byte [RFU]	Read / Write
CPR2_H	$05	Communication Protocol Register 2 – High Byte	Read / Write
CPR3_L	$06	Communication Protocol Register 3 – Low Byte [RFU]	Read / Write
CPR3_H	$07	Communication Protocol Register 3 – High Byte	Read / Write
CPR4_L	$08	Communication Protocol Register 4 – Low Byte [RFU]	Read / Write
CPR4_H	$09	Communication Protocol Register 4 – High Byte	Read / Write
SREG	$0A	Status Register	Read—Only
EREG	$0B	Error Register	Read—Only
IDR	$0C	Hardware ID Register	Read—Only
PLL	$0D	PLL Configuration Register	Read / Write
TXC	$0E	Transmitter Register	Read / Write
RXC	$0F	Receiver Register	Read / Write
All other register address values are NOT supported			

Registers in the following sections are listed in register address order.

Figure 10. Register Memory Map

Register Name	Register Address	Register Definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPR0_L	$00	*Reserved for future use*							
CPR0_H	$01	FWI				*RFU*			
CPR1_L	$02	*Reserved for future use*							
CPR1_H	$03	FWI				*RFU*			
CPR2_L	$04	*Reserved for future use*							
CPR2_H	$05	FWI				*RFU*			
CPR3_L	$06	*Reserved for future use*							
CPR3_H	$07	FWI				*RFU*			
CPR4_L	$08	*Reserved for future use*							
CPR4_H	$09	FWI				*RFU*			
SREG	$0A	RF	POR	CD	*RFU*				
EREG	$0B	CRC	FRAME	BYTE	TIME	COL	SPE	*RFU*	
IDR	$0C	ID							
PLL	$0D	SL1	SL0	ENB	*RFU*			RS1	RS0
TXC	$0E	TXP	ML						
RXC	$0F	G				SS			
All other register address values are NOT supported									

3.1 CPR0 Register [$00 / $01]

This read-only 16 bit register contains the standard ISO/IEC 14443 RF communication protocol settings.

3.1.1 Operation

The built-in polling functions of the reader IC utilize the settings in CPR0 to configure the transmit and receive frames. When performing communication with the ISO/IEC14443-3 standard commands the CPR field of the TX Data command should contain 000b to select CPR0.

The 16 bit CPR0 register is addressed as two 8 bit registers, CPR0_L (address $00) and CPR0_H (address $01).

3.1.2 Registers

Figure 11. CPR0_L Register Definition. All Bits are RFU.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved for future use							
Default:	0	0	0	0	0	0	0	0

Figure 12. CPR0_H Register Definition

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	FWI				*RFU*			
Default:	0	0	0	0	0	0	0	0

3.1.3 Field Descriptions

FWI: Frame Waiting Interval. Always $0 to select minimum wait time.

RFU: Reserved for Future Use. All RFU bits contain 0 b.

3.2 CPR Registers 1, 2, 3, 4

CPR1 Register [$02 / $03]

CPR2 Register [$04 / $05]

CPR3 Register [$06 / $07]

CPR4 Register [$08 / $09]

These read/write 16 bit registers are used to set the Timeout wait time for RF communications.

3.2.1 Operation

Each 16 bit command protocol register is addressed as two 8 bit registers, CPRx_L and CPRx_H. The register addresses are shown in Table 9.

Table 9. CPR Register Addresses

Communication Protocol Register	Register Address		Command CPR		
	CPRx_L	CPRx_H	Bit 2	Bit 1	Bit 0
CPR0	$00	$01	0	0	0
CPR1	$02	$03	0	0	1
CPR2	$04	$05	0	1	0
CPR3	$06	$07	0	1	1
CPR4	$08	$09	1	0	0
All other CPR values are NOT supported					

When communicating over the RF channel the CPR field of the command is used to select a CPR register set to configure the reader. By storing the timeout setting in the CPR registers it is only necessary to configure the RF protocol once. A transaction can contain a series of commands with different response times; as the reader executes each command it reconfigures the transceiver instantly to the settings in the specified CPR. Transaction time is optimized by specifying FWI no longer than necessary for each PICC operation.

3.2.2 Registers

Figure 13. CPRx_L register Definition. All Bits are RFU.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved for future use							
Default:	0	0	0	0	0	0	0	0

Figure 14. CPRx_H Register Definition

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	FWI				*RFU*			
Default:	0	0	0	0	0	0	0	0

3.2.3 Field Descriptions

FWI: Frame Waiting Interval. Used to select the time the reader waits for a response to begin after a command is transmitted. The Frame Waiting Time (FWT) is calculated from FWI using the formula in the unamended ISO/IEC14443-3 base standard.

Table 10. Coding of Frame Waiting Time in FWI Field

Bit 7	Bit 6	Bit 5	Bit 4	FWT	FWT Time
0	0	0	0	32 ETUs	302.1 uS
0	0	0	1	64 ETUs	604.1 uS
0	0	1	0	128 ETUs	1,208.3 uS
0	0	1	1	256 ETUs	2,416.5 uS
0	1	0	0	512 ETUs	4,833.0 uS
0	1	0	1	1024 ETUs	9,666.1 uS
0	1	1	0	2048 ETUs	19,332.2 uS
0	1	1	1	4096 ETUs	38,664.3 uS
1	0	0	0	8192 ETUs	77,328.6 uS
1	0	0	1	16384 ETUs	154,657.2 uS
1	0	1	0	32768 ETUs	309,314.5 uS
1	0	1	1	65536 ETUs	618,628.9 us
1	1	0	0	131072 ETUs	1,237,257.8 uS
1	1	0	1	262144 ETUs	2,474,515.6 uS
1	1	1	0	524288 ETUs	4,949,031.3 uS
1	1	1	1	*RFU*	*RFU*

RFU: Reserved for Future Use. All RFU bits must contain 0 b.

3.3 SREG Register ($0A)

This read-only register reports the status of the reader.

3.3.1 Operation

The state of the reader can be determined by reading this register.

3.3.2 Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	RF	POR	CD	*RFU*				
Default:	0	0	0	0	0	0	0	0

3.3.3 Field Descriptions

RF: RF Field Enabled. A one indicates RF field is ON.

POR: Power On Reset. A one indicates the RF Interface of the chip is in reset due to low supply voltage.

CD: Carrier Detect. A one indicates the receiver is detecting 847.5 kHz subcarrier.

RFU: Reserved for Future Use. All RFU bits contain 0 b.

3.4 EREG Register [$0B]

This read-only register reports RF communication errors. Not every bit is functional with every command.

3.4.1 Operation

The contents of this register are returned in the error register field of a response to the host.

3.4.2 Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CRC	FRAME	BYTE	TIME	COL	SPE	*RFU*	
Default:	0	0	0	0	0	0	0	0

3.4.3 Field Descriptions

CRC: CRC Error. A one indicates an error in the received data packet.

FRAME: Framing Error. A one indicates the received packet is not in a valid frame.

BYTE: Byte Error. A one indicates the received packet was incomplete.

TIME: Timeout Error. A one indicates the specified waiting time has expired with no response received.

COL: Collision Error. A one indicates a collision was detected during polling.

SPE: Smart Poll Error. A one indicates that when the maximum specified number of slots was polled, collisions were detected in all slots.

RFU: Reserved for Future Use. All RFU bits contain 0 b.

3.5 IDR Register [$0C]

This read-only register reports the hardware revision of the chip.

3.5.1 Operation

The value of this register in hex corresponds to the IC hardware revision. This register is updated when the IC design is changed.

3.5.2 Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ID							
Default:	0	0	0	1	0	0	0	1

3.5.3 3.5.3 Field Descriptions

ID: Hardware Revision ID.

ID = $10 indicates pre-production hardware.

ID = $11 indicates production hardware.

3.6 PLL Register ($0D)

This read/write register sets the configuration of the CLKO pin.

3.6.1 Operation

The CLKO pin PLL generates a programmable output frequency on the CLKO pin for use by circuits external to the reader chip. The PLL configuration has no impact on the internal functionality except in standby mode, when the SLx bits impact the standby current and wakeup delay time. By default the CLKO output is enabled and set to the lowest frequency after power-on-reset.

3.6.2 Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SL1	SL0	ENB	*RFU*			RS1	RS0
Default:	0	0	0	0	0	0	0	0

3.6.3 Field Descriptions

SL1: PLL Sleep. A one turns the PLL off in standby mode.

SL0: Oscillator Sleep. A one turns the crystal oscillator off in standby mode.

ENB: CLKO Output Enable Bar. A one disables the CLKO output.

RSx: CLKO Rate Select bit. Sets the PLL frequency for CLKO pin.

Table 11. CLKO Rate Select bit Coding

Bit 1	Bit 0	CLKO Frequency
0	0	1.978 MHz
0	1	3.955 MHz
1	0	7.910 MHz
1	1	15.82 MHz

RFU: Reserved for Future Use. All RFU bits must contain 0 b.

3.7 TXC Register [$0E]

This read/write register sets the transmit power and ASK modulation level.

3.7.1 Operation

The transmit modulation index is set with the ML bits. The TXP bit selects between two RF output power levels.

3.7.2 Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TXP	ML						
Default:	0	0	0	0	0	0	0	0

3.7.3 Field Descriptions

TXP: Transmit Power. 1 b selects low RF power. 0 b selects high RF power.

ML: Modulation Level. Adjusts the level of a zero transmitted by the reader. Typical setting is 0001000 b.

Table 12. Modulation Level Coding

ML							Modulation index
Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	0	1	8%
0	0	0	0	0	1	0	9%
0	0	0	0	1	0	0	10%
0	0	0	1	0	0	0	11%
0	0	1	0	0	0	0	12%
0	1	0	0	0	0	0	13%
1	0	0	0	0	0	0	14%
All other values are NOT supported.							

Warning: Do not set multiple bits in the ML field to 1 b. Improper configuration of this register can result in permanent damage to the device.

3.8 RXC Register [$0F]

This read/write register sets the receiver circuit gain and noise immunity.

3.8.1 Operation

This register adjusts the receiver gain and noise immunity. The gain should be adjusted to the minimum level that provides good RF performance. Excessive gain amplifies system noise, reducing overall RF communication performance.

The noise immunity field (SS) should be adjusted to the maximum level that provides good RF performance. Setting SS too low will prevent the reader from distinguishing a real RF response from system noise, reducing overall RF communication performance.

3.8.2 Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	G				SS			
Default:	0	0	0	0	0	0	0	0

3.8.3 Field Descriptions

G: Receiver Gain Adjustment. Typical Setting is $1.

Table 13. Receiver Gain Coding

G					Receiver Gain
Bit 7	Bit 6	Bit 5	Bit 4	Hex	
0	0	0	0	$0	Minimum
0	0	0	1	$1	Low
1	0	1	0	$A	Medium
1	0	1	1	$B	High
1	1	1	1	$F	Maximum
All other values are NOT supported					

SS: Receiver Squelch. Adjust the receiver noise immunity. Typical Setting is $5 to $7.

Table 14. Receiver Squelch Coding

SS					Receiver Noise Immunity
Bit 3	Bit 2	Bit 1	Bit 0	Hex	
0	0	0	0	$0	Maximum
0	0	0	1	$1	..
0	0	1	0	$2	..
0	0	1	1	$3	High
0	1	0	0	$4	..
0	1	0	1	$5	Moderate
0	1	1	0	$6	..
0	1	1	1	$7	Low
1	0	0	0	$8	..
1	0	0	1	$9	Minimum
All other values are NOT supported					

Appendix A
Initialization Procedure

The procedure for initializing the AT88RF1354 RF Reader is outlined here, starting from power up. The same general procedure applies when the IC ResetB pin is toggled (starting at step 2).

1. Turn Power On to both Vcc and Vcc_Ant.
2. Drive the ResetB pin Low for a minimum of 500 uS, then drive it high and hold it at the Vcc voltage level. Wait 1 mS for the crystal oscillator to stabilize.
3. Initialize the Configuration Registers by sending a Clear Command, followed by Write Register Commands. An ACK response must be received after each command.

Clear	(Clear all register contents)
Write PLL Register $0D to $20	(Disable CLKO Output)
Write TXC Register $0E to $08.	(High RF Power, 11% Modulation Index)
Write RXC Register $0F to $16	(Nominal Receiver Gain and Sensitivity)
Write CPR Register $03 to $20	(Set CPR1 for Timeout Wait Time of 1.2 milliseconds)
Write CPR Register $05 to $30	(Set CPR2 for Timeout Wait Time of 2.4 milliseconds)

4. Send the RF ON Command. Read SREG using the Read Register Command to verify that the RF Field is on.
5. Perform the RF Transaction. A typical RF Transaction begins with Poll Single Commands, followed by a series of TX Data Commands to select, write, and read the Card.
6. Send the RF OFF Command. Read SREG using the Read Register Command to verify that the RF Field is off.
7. The Reader is ready to be powered off or placed in standby mode using the Sleep Command.

Appendix B
The SPI Serial Interface

The SPI Interface mode is selected by shorting the ISEL pin to Vcc. Six microcontroller pins are required to operate AT88RF1354 in SPI mode. The ISTAT signal is used for handshaking between the microcontroller and RF reader.

B.1 SPI Interface

The AT88RF1354 SPI interface operates as a slave device in SPI mode 0. In SPI mode 0 the polarity and phase of the serial clock in relation to the data is as follows:

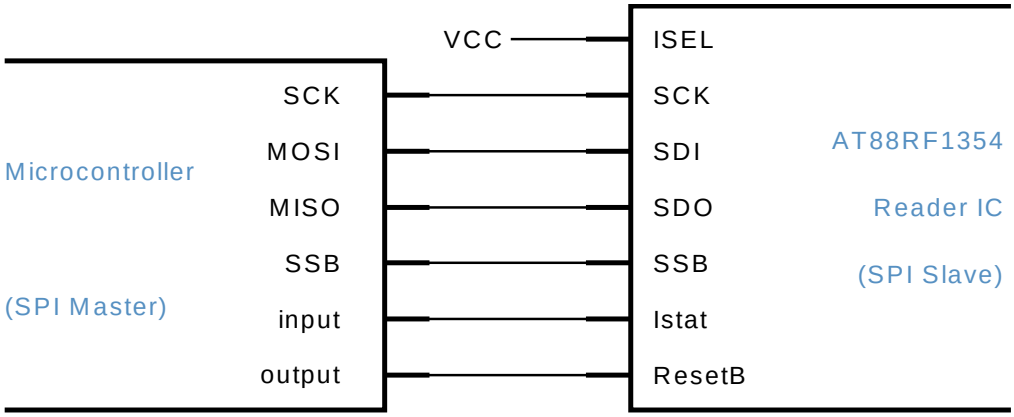
SCK is low when IDLE.

Incoming data on SDI is sampled on the positive edge of SCK.

Outgoing data on SDO is setup on the negative edge of SCK. (The host microcontroller samples SDO on the positive edge of SCK)

ISTAT reports the serial interface status to the microcontroller.

Figure 15. Serial Interface Wiring to SPI Microcontroller



A high level on the ISTAT pin signals the host microcontroller that a byte of data is ready to be read from the AT88RF1354 serial interface. If another byte is immediately available on the serial port, ISTAT will go low for 150 uS, then return high. ISTAT will remain high until the last bit of the byte is read, when it will return low. All data must be clocked out of the AT88RF1354 before it can receive a command.

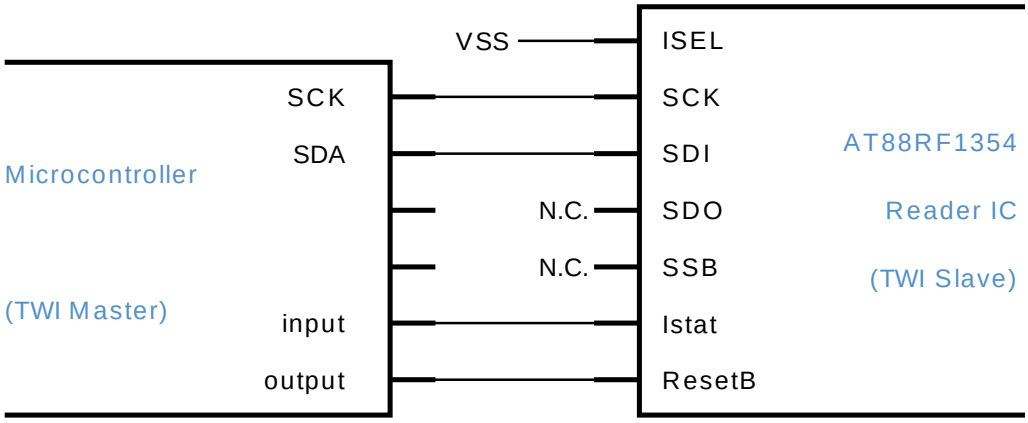
Appendix C
The TWI Serial Interface

The TWI Interface mode is selected by shorting the ISEL pin to Vss. Four microcontroller pins are required to operate AT88RF1354 in TWI mode. TWI ACK polling is not supported; the ISTAT signal is used for handshaking between the microcontroller and RF reader.

C.1 TWI Interface

The AT88RF1354 2-wire serial interface (TWI) operates as a slave device. The TWI interface allows the device to share a common 2-wire data bus with other compatible devices. The bus consists of a serial clock (SCK) and a serial data (SDA / SDI) line. The serial clock is generated by the TWI bus master. Serial data bytes are transmitted bi-directionally on the SDA / SDI line, most significant bit first, synchronized to the SCK. The ISTAT signal reports the serial interface status to the microcontroller.

Figure 16. Serial Interface Wiring to TWI Microcontroller



A high level on the ISTAT pin signals the host microcontroller that a byte of data is ready to be read from the AT88RF1354 serial interface. If another byte is immediately available on the serial port, ISTAT will go low for 150 uS, then return high. ISTAT will remain high until the last bit of the byte is read, when it will return low.

Data on the SDA / SDI line is sampled by the receiving device when the SCK clock is high. Data is allowed to be changed by the transmitting device only when the SCK clock is low. All data must be clocked out of the AT88RF1354 before it can receive a command.

C.2 TWI Device Address

The TWI device address is selected with the ADDR address select pin of the AT88RF1354.

Table 15. TWI Device Address

ADDR Pin	TWI Device Address							TWI_R	TWI_W
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Vss	0	1	0	1	0	0	0	$51	$50
Vcc	1	1	0	1	0	1	0	$D5	$D4
All other values are NOT supported									

The AT88RF1354 device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consists of a 7 bit address followed by a read/write select bit. The write bit should be set when sending command packets to AT88RF1354. The read bit should be set when retrieving response packets from AT88RF1354.

Upon a successful compare of the device address, the AT88RF1354 will pull the SDI output low for 1 bit period, sending a TWI ACK bit. If an address compare is unsuccessful, the device will return to an idle state and the SDA / SDI line will remain pulled up by the external pull-up resistor, effectively sending a TWI NACK bit.

The AT88RF1354 ignores TWI communication packets that do not begin with matching device address. This allows other TWI devices to share the bus with the AT88RF1354 Reader.

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D.3 Revision History

Doc. Rev.	Date	Comments
5150A	3/2006	Initial document release.
5150B	12/2008	Document updated.

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