APPLICATION NOTE

ATA6560 - CAN Transceiver VHDL-AMS Demonstration (Level 1)

ATAN0133

Introduction

This document contains the documentation for the simulatable demonstration file of the simulation-runtime-optimized behaviorally modeled Atmel® high-speed CAN transceiver ATA6560. This “Demo Level 1” model is intended to be used only for bus signal integrity checks and does not cover the full functionality of the real transceiver device.

Terms, Definitions and Abbreviations

Table 1. Terms, Definitions and Abbreviations

Short Name	Definition
BUS	CAN BUS
CANH	CAN BUS high channel
CANL	CAN BUS low channel
CM	Common mode = (CANH + CANL)/2
CAND	Differential mode = (CANH – CANL)
RXD	Receiver pin / receiver signal
TXD	Transceiver pin / transceiver signal
VCC	Supply pin / supply level / supply signal
GND	Ground pin / ground level / ground signal
TEMP	High level model parameter which selects one of three possible scenarios

1. Parameters

The model is parameterized regarding the high, low and typical characteristics of the device. The interface contains the model parameter “TEMP”. The following values are possible.

Table 1-1. Parameter “TEMP”, Possible Values

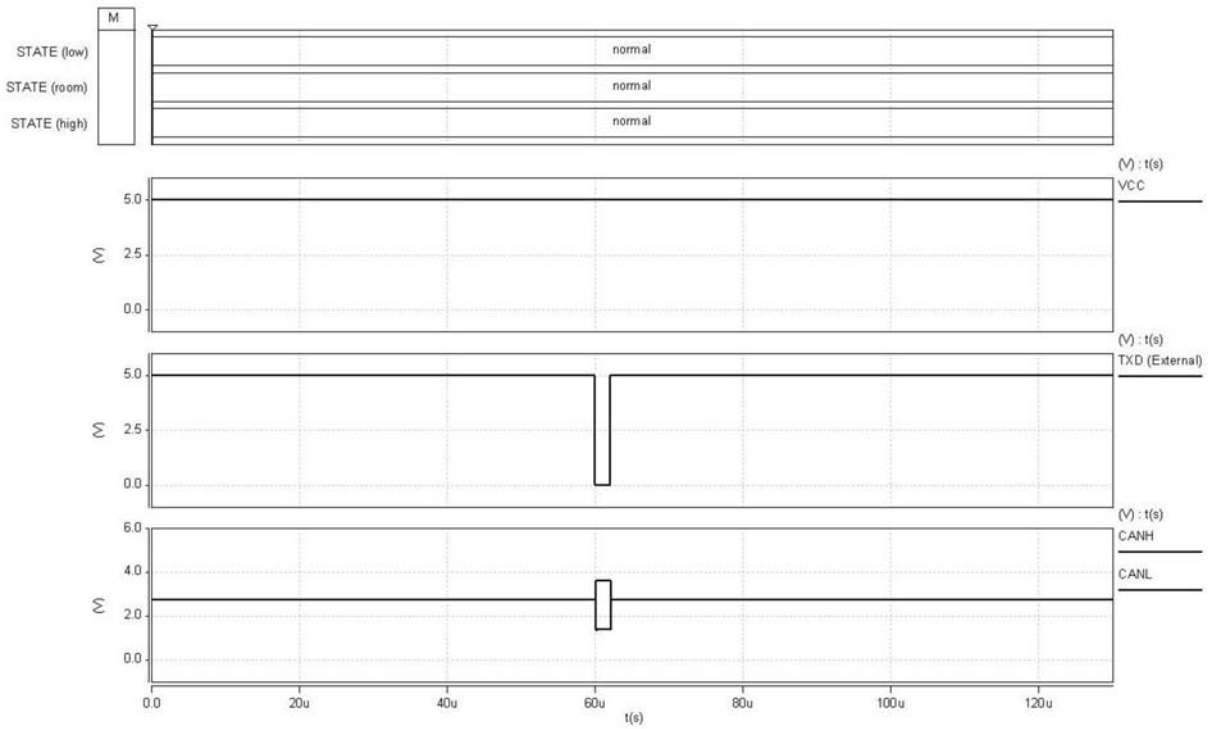
“TEMP” value	Description
–1	This setting covers the low temp behavior based on real device measurements and minimal characteristics as stated in the device datasheet
0	This setting covers the room temp behavior based on real device measurements and typical characteristics as stated in the device datasheet
1	This setting covers the high temp behavior based on real device measurements and maximal characteristics as stated in the device datasheet

2. Implementation

This demonstration file is intended to show the basic configuration / application for a Level 1 ATA6560 VHDL-AMS Model. Its characteristics are shown in Figure 2-1.

It is possible to run the demo file from a test-bench which calls this demo and make reference of all the possible parameters of interest as for example “TEMP”. The values of VCC, Load, etc. are already fixed in the demo file, but they could be shifted from the architecture area to the entity area and be called from a test-bench file too. The same applies to the signal TXD as well.

Figure 2-1. Running the Demonstration File for Level 1 Implementation



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