

General Description

Micrel's SY56xxx Ultra-low voltage CML family is designed to be used in various communications, video, and test and measurement applications. Products in this family recover data signals driven through long transmission lines. Furthermore, these products enable designers to interface to different voltage levels, and distribute data at high speeds.

Equalization (EQ)

As data signals travel through long traces of transmission medium, signal swings are attenuated and transition edges slow down. Consequently, the eye openings attenuate and bit error rates increase. The equalization control circuit amplifies the attenuated input signals to correct voltage levels.

Signal attenuation is a function of frequency, transmission length, quality of transmission medium and data pattern. Although signal attenuation depends on multiple variables, EQ ICs are designed by considering transmission length as the most significant variable. Figure 1. shows LOS tangent for various cable and FR4 lengths across frequency. Figures 2-5 show the test setup and some scope diagrams showing the affects of EQ.

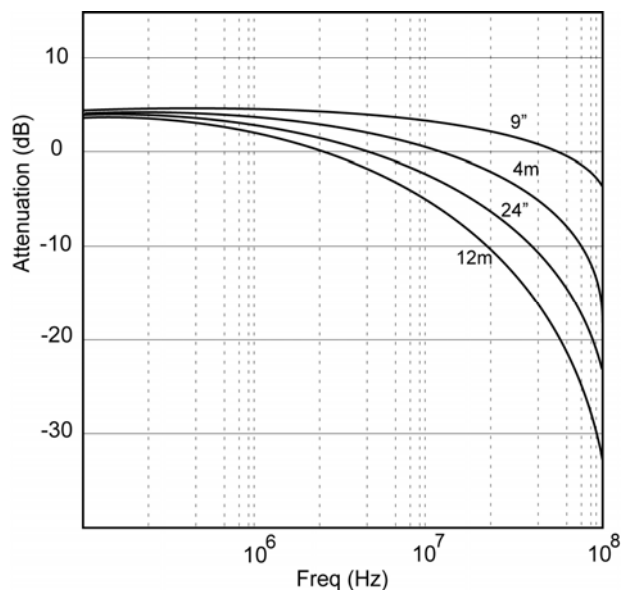


Figure 1. Signal Attenuation Curve

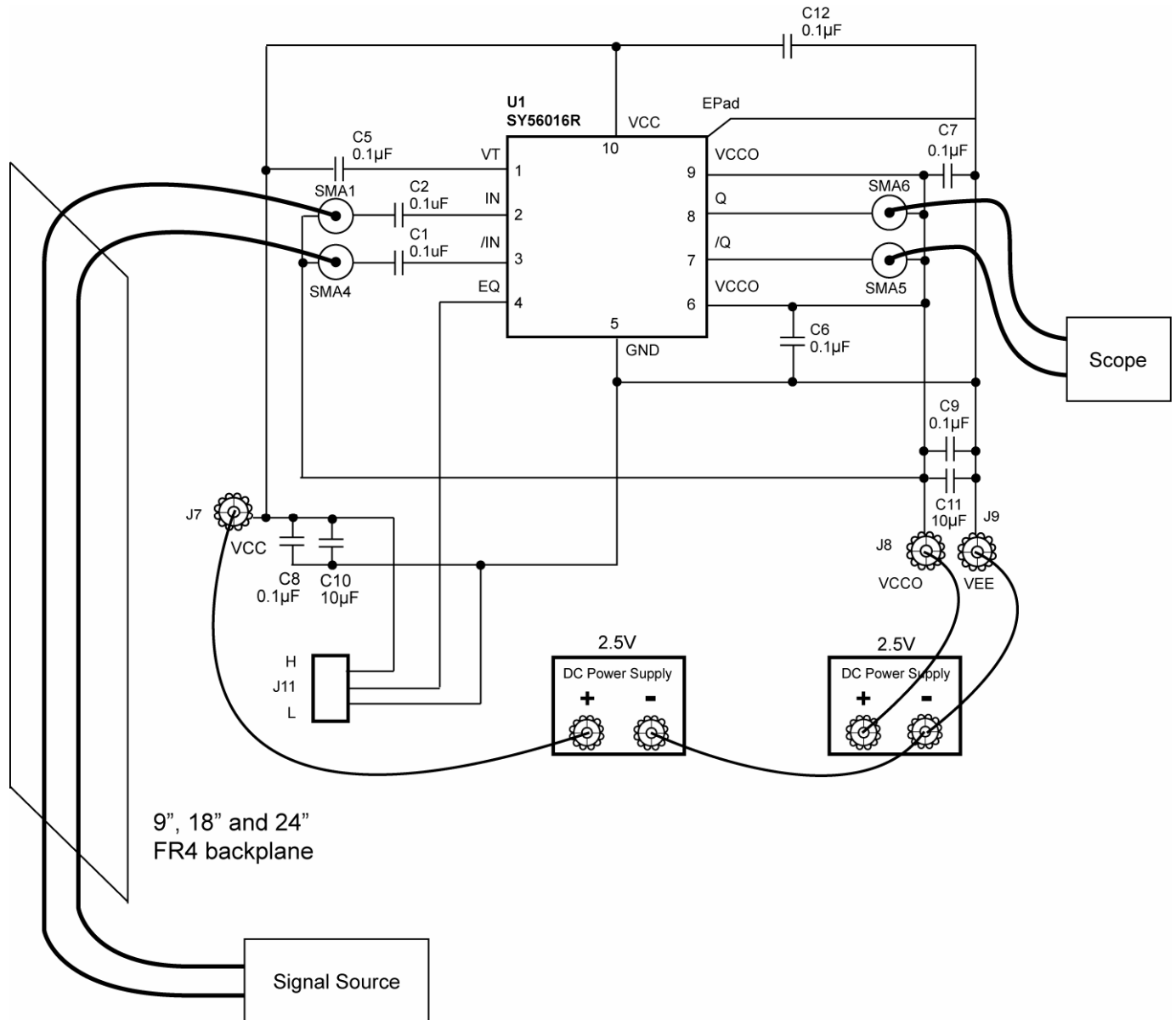


Figure 2. Test Set-Up

Test Results

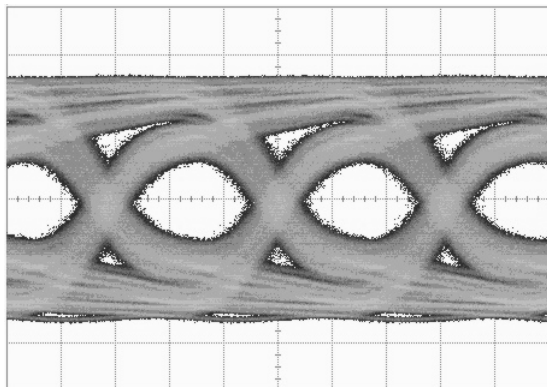


Figure 3a. Attenuation due to 9" FRA at 6.4Gbps

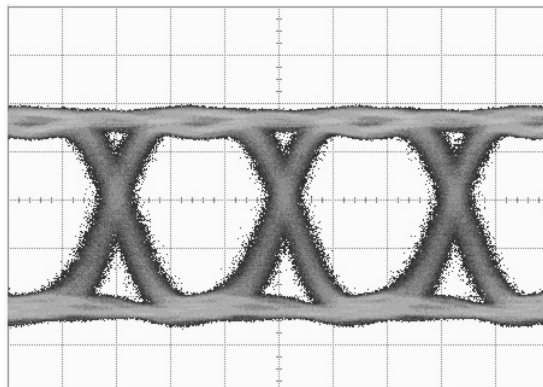


Figure 3b. Recovered Signal 6.4Gbps

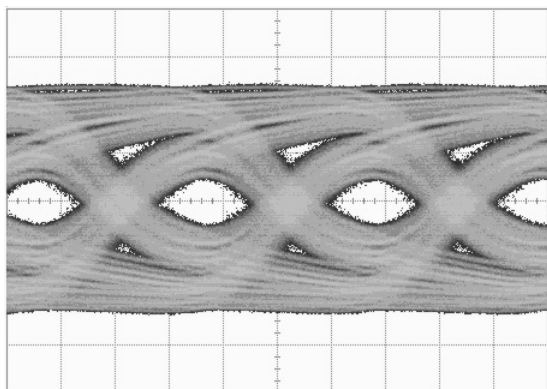


Figure 4a. Attenuation due to 18" FRA at 6.4Gbps

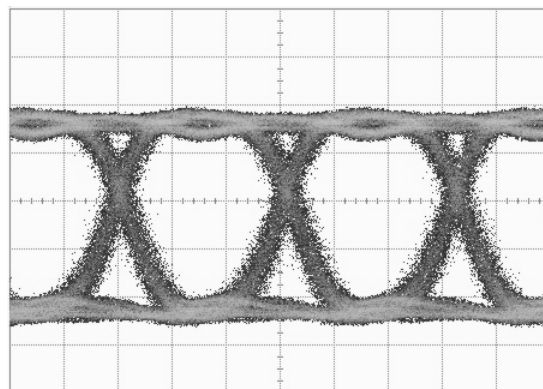


Figure 4b. Recovered Signal 6.4Gbps

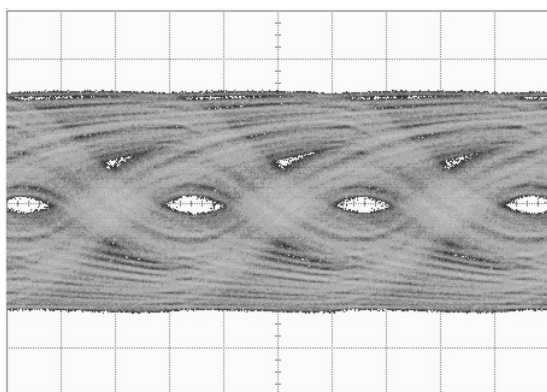


Figure 5a. Attenuation due to 24" FRA at 6.4Gbps

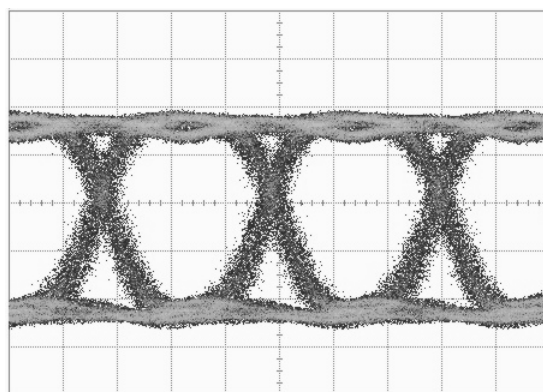


Figure 5b. Recovered Signal 6.4Gbps

Power Supply

The core circuit of the SY56xxx products is designed to operate at 2.5V while the output stage can operate at 1.2V, 1.8V, or 2.5V. A variable output stage power supply allows system designers to interface a higher voltage signal to a lower voltage receiver.

I/O Interface

Since the input structure of these products are very flexible, these products can accept various differential signals at different voltages. Thus, these products can not only be used as buffers, multiplexers, or fanouts, but also as translators to interface to different logic signals. Furthermore, these products lower cost and simplify designs.

SY56xxx products are ideal for driving 50Ω (or 100Ω differential) transmission lines, either AC- or DC-coupled. AC-coupling is used when the common mode voltage level needs to be shifted. For instance, AC-coupling is useful while interfacing PECL or LVDS drivers to SY56xxx. On the other hand, DC-coupling allows a straightforward interface between 1.8/2.5V CML driver and SY56xxx.

Since AC-coupling requires re-biasing the common mode, any differential signal can be interfaced to SY56xxx products. SY56xxx can accept AC-coupling from any driver with voltage swing between 0.2V and 1.0V. To lower noise, bypass VT pin with a 0.1μF low ESR capacitor to V_{CC}. To provide a bias voltage for AC-coupling, the input stage has an internal high impedance resistor network. Below are various input AC-coupled interfacing schemes. See individual datasheet for more details.

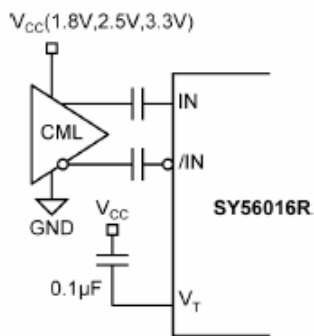


Figure 6a. CML Interface

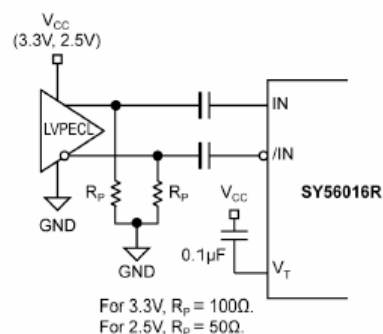


Figure 6b. LVPECL Interface

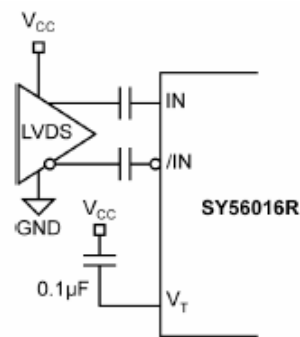


Figure 6c. LVDS Interface

While interfacing the CML driver to the SY56xxx using DC-coupling, it is important to consider the common mode voltage. VT pin allows proper termination based on input signal levels. Terminate 1.8V CML driver 50Ω-to-VT pin. 2.5V CML driver can be terminated either 50Ω-to-VT pin or 100Ω differential. The input cannot be DC-coupled from a 1.2V CML driver. Below are the two DC-coupled interfacing schemes. See individual datasheet for more details.

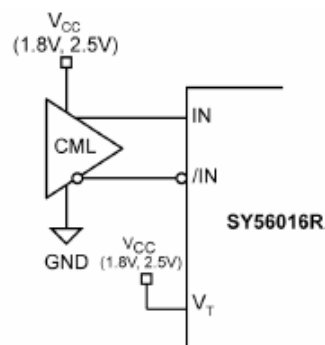


Figure 7a. 1.8/2.5V CML Interface

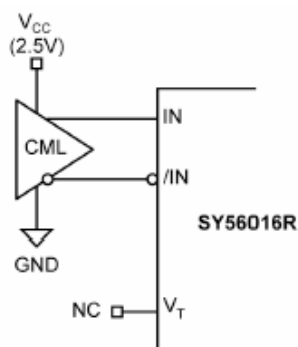


Figure 7b. 2.5V CML Interface

Proper termination is crucial while operating parts at high speeds as improper terminations lead to mismatched impedance. Consequently, jitter increases. It is also important to terminate the transmission line as close to the receiver as possible to lower the effects of reflections. A separate power supply for the output stage allows the output signal to interface to various CML receivers. The output of SY56xxx can be either AC- or DC-coupled to the receiver. Below are various output-interfacing schemes based on coupling and V_{CCO} :

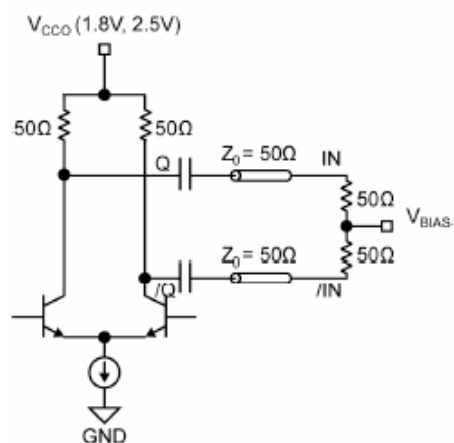


Figure 8a. 1.8/2.5V AC-coupled CML Interface

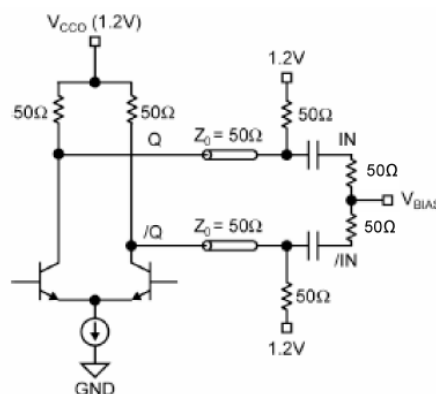


Figure 8b. 1.2V AC-coupled CML Interface

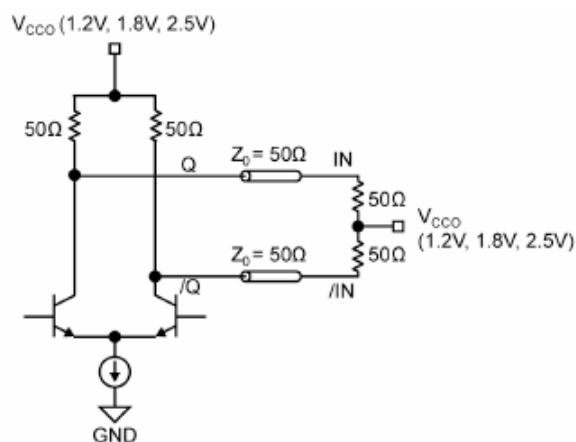


Figure 8c. 1.2/1.8/2.5V DC-coupled CML Interface

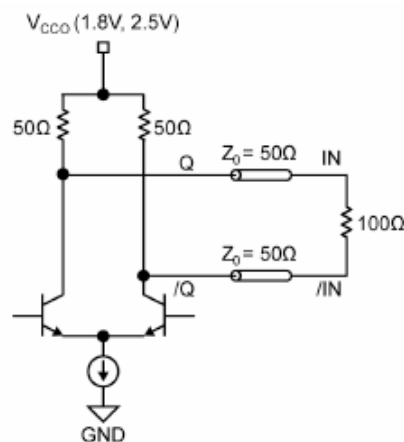


Figure 8d. 1.8/2.5V DC-coupled CML Interface

For further information, email hbwhelp@micrel.com or call 408-955-1690.

Part Number	Function	EQ	Freq (Gbps)	Freq (GHz)	Package
SY56016R	1:1 Buffer	Yes	6.4	4.5	10-Pin MLF [®] (2mm x 2mm)
SY56216R	Dual 1:1 Buffer	Yes	6.4	4.5	16-Pin MLF [®] (3mm x 3mm)
SY56011R	1:2 Fanout	Yes	6.4	4.5	16-Pin MLF [®] (3mm x 3mm)
SY56017R	2:1 MUX	Yes	6.4	4.5	16-Pin MLF [®] (3mm x 3mm)
SY56020R	1:4 Fanout	Yes	6.4	4.5	16-Pin MLF [®] (3mm x 3mm)
SY56020XR	1:4 Fanout	Yes	6.4	4.5	16-Pin MLF [®] (3mm x 3mm)
SY56572XR	1:4 Fanout	Yes	6.4	4.5	16-Pin MLF [®] (3mm x 3mm)
SY56023R	2x2 Crosspoint	Yes	6.4	4.5	16-Pin MLF [®] (3mm x 3mm)
SY56034AR	2:6 Crosspoint	No	6.4	5.0	32-Pin MLF [®] (5mm x 5mm)
SY56040AR	4x4 Crosspoint	No	6.4	5.0	44-Pin MLF [®] (7mm x 7mm)

Table 1. SY56xxx Ultra Low Voltage CML Products

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