



Design Guidelines for Connecting the ARCNET Product Family, COM20019/20/22, with Renesas Technology's SH Series Microcontrollers

1 Introduction

SMSC's COM20019, COM20020 and COM20022 ARCNET controllers are designed to be easily connected to all types of microcontrollers. However, special attention to bus timing is recommended for designs using Renesas Technology's SH Series RISC microcontrollers and SMSC's ARCNET devices. Using SH-1, 2, 3 and 4 SOCs, critical design information and practices connection are summarized and explained.

Note that COM20020 is used as the example to represent ARCNET controller; the design guidelines also can be applied to COM20019/22.

1.1 SH1 and COM20019/20/22 Connection

The following 2 points with respect to connection between SH-1 and the COM20020 should be handled with special care.

1.1.1 Read/Write Cycle AC Timing Specification

Based on the bus timing for RISC type CPUs, beginning with SH-1, setup/hold time for address and chip select is very tight. In particular, the following 2 points are issues during a read cycle.

A0 - A2 and nCS setup time to the falling edge of nRD

A0 - A2 and nCS hold time from the rising edge of nRD

If these setup/hold time are violated, it usually can't be resolved even if the bus cycle is extended using a wait cycle. Also, the faster the bus clock, the worse the problem.

For the COM20020, using a bit setup, two types of setup/hold time can be set for only a read cycle. If the setup 2 register RBUSTMG bit =1 is set, a setting for compatibility with a high speed CPU (high speed read operation) is established and the setup/hold time requirement is relaxed and there are cases where the above issue is resolved. However, on the other hand, there is also the disadvantage that data access time and nRD specification pulse width are lengthened. Please insert a wait cycle to extend the bus cycle as a countermeasure.

To prevent misunderstanding, while this is termed high speed read operation mode, it is not that access time and cycle time become high speed. It is a mode that enables connection to a RISC type high speed CPU without external logic. In fact, data access time is lengthened and through insertion of wait cycles the nRD pulse width is extended, therefore it is not high speed. The actual timing specifications are noted on pages 57, 58 of the COM20020 datasheet (Rev 04-15-05); therefore, if you review both of these pages you will understand the differences. Note that even if the RBUSTMG bit is set to 1, the write cycle timing specification is not relaxed.

1.1.2 Dummy Write Addresses when Connecting to a 16 Bit CPU

For COM20020 CPU interface mode settings, after the hardware reset cancellation, prior to accessing the COM20020, dummy writing to odd number addresses (nCS=H write operation) needs to be performed.

However, care must be taken for dummy writing when connected to a 16 bit CPU. Odd number addresses are the addresses for the COM20020. In other words, the addresses which cause the COM20020 A0 pin to be set to high are called odd number addresses. When connecting a 16 bit CPU, the A1 pin on the CPU side is shifted to the COM20020 A0 pin for connection, in this case odd number addresses means something different. In this case, dummy write to the addresses causes the CPU A1 pin to go high. For example, the hexadecimal addresses xxx2h, 6h, Ah, and Eh. The CPU bus type is determined by this dummy write and afterwards the COM20020 registers can be accessed.

1.2 SH2 and COM20019/20/22 Connection

The following 2 points with respect to the connection between SH-2 and the COM20020 should be handled with special care

1. Read/Write cycle AC timing specification
 - a. Enable extension of nCS assert period
 - b. Extend the bus cycle by inserting a wait
2. Dummy write addresses when connecting to a 16 bit CPU

1.2.1 Read/Write Cycle AC Timing Specification

1.2.1.1 Enable Extension of nCS Assert Period

In general, the bus timing for RISC type CPUs setup/hold time for address and chip select is very tight. In particular, the following 2 points are the potential issues during a read cycle.

A0 - A2 and nCS setup time to the falling edge of nRD

A0 - A2 and nCS hold time from the rising edge of nRD

If these setup/hold time are violated, it usually can't be resolved even if the bus cycle is extended using a wait cycle. Also, the faster the bus clock, the worse the problem.

However, for the SH-2, there is a mode prepared to secure this setup/hold time. This mode is called "nCS assert period extension". This "nCS assert period extension" function automatically inserts idle cycles before and after the bus cycle for SH-2 and gains more than sufficient time for the above setup/hold time.

(SH-1 and SH-3 do not have this function)

The "nCS assert period extension" is enable through setting the SH-2 BCR2 register SW3~0 bits. (SH-2 datasheet P. 180, P. 197)

1.2.1.2 Extend the Bus Cycle by Inserting a Wait

There are timing specifications concerning cycle time (interval time) that are 4 TARB (5 TARB) for continuous access to the COM20020.

5 TARB and 4 TARB 5 are cycle time (interval time) specifications. Specifically, they are the specifications of the AC timing chart after page 53 of the "COM20020 datasheet Rev. 04-15-05".

The CPU interface mode when connecting SH-2 is a non-multiplex bus as well as 80xx system (nWR, nRD type) mode. This specification is written on pages 70 (read cycle) and 74 (write cycle). Both read cycles and write cycles are controlled by the timing specification noted in t5:Cycle Time of the table

and the 4 TARB and 5 TARB values included in the notes under the table. (For case where nBUSTMG pin = high, RBUSTMG bit = 0).

A wait must be inserted in order for there to be a sufficient interval for continuous access to the COM20022 as well as to extend the active width of the read/write nRD or nWR for the COM20020.

Combinations for continuous access to the COM20020 are the following 4 items.

- A. Write → Write (nWR↑ ~ next nWR↑;)
- B. Read → Read (nRD↓ ~ next nRD↓)
- C. Write → Read (nWR↑ ~ next nRD↓)
- D. Read → Write (nRD↓; ~ next nWR↑)

(Note ↑:rising edge, ↓:falling edge)

The reference for a "Write" is the rising edge of nWR and the reference for a "Read" is the falling edge of nRD

For the above A ~ D, greater than a maximum 5 TARB (250 nS @ 2.5 mbps, SLOWARB bit = 0) is necessary. Therefore, if the bus cycle becomes greater than 5 TARB through insertion of a wait, the above A, B, and D can be cleared. However, for C, an intentional wait in the program is needed. After performing a write to the COM20020, set the program so that it waits for at least 5 TARB and then perform a Read of the COM20020.

Set the SH-2 WCR1 register W33 ~ 0 bit to insert a wait (SH-2 datasheet P. 181).

TARB expresses the clock signal period being supplied to the dual port RAM inside the COM20020. Also, TARB is determined by the period of the maximum internal operating clock.

XTAL1 FREQUENCY	CKUP1,0-BIT	TOPR	MAXIMUM TRANSFER RATE	SLOWARB-BIT	TARB
20 MHz	0,0	50 ns	2.5 Mbps	,O	50 ns
20 MHz	0,1	25 ns	5 Mbps	,O	25 ns
20 MHz	1,1	12.5 ns	10 Mbps	,P	25 ns

The CKUP 1, 0 bits are in the setup 2 register and set the "multiplication factor" of the clock multiplication circuit (PLL circuit). (00: x1, 01: x2, 11: x4) The SLOWARB bit is in the setup 1 register and sets whether the clock signal supplied to the dual port RAM is divided in half or not.

For Topr = 50 ns/25 ns, there is no problem with leaving SLOWARB = 0 (0: full speed, 1: half speed).

1.2.2 Dummy Write Addresses when Connecting to a 16 Bit CPU

For COM20020 CPU interface mode settings, after the hardware reset cancellation, prior to accessing the COM20020, dummy writing to odd number addresses (nCS=H write operation) needs to be performed.

However, special care must be taken for dummy writing when connected to a 16 bit CPU. Odd number addresses are the addresses for the COM20020. In other words, the addresses which cause the COM20020 A0 pin to be set to high are called odd number addresses. When connecting a 16 bit CPU, the A1 pin on the CPU side is shifted to the COM20020 A0 pin for connection, in this case odd number addresses mean something different. In this case, dummy write to the addresses causes the CPU A1 pin to go high. For example, the hexadecimal addresses xxx2h, 6h, Ah, and Eh. The CPU bus type is determined by this dummy write and afterwards the COM20020 registers can be accessed.

1.3 SH3 and COM20019/20/22 Connection

The following 2 points with respect to connection between SH-3 and the COM20020 should be handled with special care:

1. Read/Write cycle AC timing specification
2. Dummy write addresses when connecting to a 16 bit CPU

1.3.1 Read/Write Cycle AC Timing Specification

After investigating the AC timing specification of the SH-3 datasheet, the timing is different from SH-1. This is shown below.

- Setup time for the chip select (nCS) to the falling edge of a Read (nRD)
- Hold time for the chip select (nCS) from the rising edge of a Read (nRD)
- Hold time for the chip select (nCS) from the rising edge of a write (nWE)

Through these timing changes, while there was only one issue with the read cycle side set up time for SH1, there are other issues with especially hold time for both a read cycle and a write cycle for SH-3.

In addition, for SH-3 as nWE and nRD have the same timing, if a setup/hold time countermeasure for only the read cycle is taken as this does not provide a setup/hold time countermeasure for the write cycle, the countermeasure is insufficient for a high speed CPU read operation mode (RBUSTMG bit = 1). The high speed CPU read operation mode for the COM20020D is effective for the read cycle but is not effective with respect to the write cycle. The problems of not using the high speed CPU read operation mode are explained below.

Problem 1: nCS hold time from the rising edge of nRD can not be specified

The transition timing for the rising edge of nRD and nCS from the falling edge of CKIO (bus clock) in the T2 cycle is the same time. Compare tCSD2 and tRSD in Fig 16.18 on P.16-23 of the SH-3 datasheet. As tCSD2 and tRSD are only the maximum specifications, the rising edge of nRD may be delayed with respect to the rising edge of nCS. With the COM20020 this is not allowable. (Simultaneous is ok)

Problem 2: nCS hold time from the rising edge of nWE can not be specified

The transition timing for the rising edge of nWE and nCS from the falling edge of CKIO (bus clock) in the T2 cycle is the same time. (Same as for Read), Compare tCSD2 and tWED in Fig 16.18 on P.16-23 of the SH-3 datasheet. As tCSD2 and tWED are only the maximum specifications, the rising edge of nWE may be delayed with respect to the rising edge of nCS. With the COM20020 this is not allowable. (Simultaneous is ok.)

An external circuit used to delay only the rising edge of nCS as a countermeasure for problems 1 and 2 above is required. (If delay is too long, set up timing becomes tight.)

1.3.2 Dummy Write Addresses when Connecting to a 16 Bit CPU

For COM20020 CPU interface mode settings, after the hardware reset cancellation, prior to accessing the COM20020, dummy writing to odd number addresses (nCS=H write operation) needs to be performed. However, special care must be taken for dummy writing when connected to a 16 bit CPU. Odd number addresses are the addresses for the COM20020. In other words, the addresses which cause the COM20020 A0 pin to be set high are called odd number addresses. When connecting a 16 bit CPU, the A1 pin on the CPU side is shifted to the COM20020 A0 pin for connection, in this case odd number addresses means something different. In this case, dummy write to the addresses causes the CPU A1 pin to go high. For example, the hexadecimal addresses xxx2h, 6h, Ah, and Eh. The CPU bus type is determined by this dummy write and afterwards the COM20020 registers can be accessed.

1.4 SH4 and COM20019/20/22 Connection

CPU model	SH4-167 MHz product (SH7750:HD6417750F167)
Bus Clock	33 MHz (CKIO output frequency)
COM20020@_XTAL1	20MHz
Transfer rate	5 Mbps
SH4 bus timing settings:	Address setup insertion (AnS=1) Hold time insertion (AnH = 1)

Insert 2 waits (2WAIT) when accessing the COM20020D

COM20020D SLOWARB bit = 0

COM20020D RBUSTMG bit = 1

COM20020D CKUP bit = 1

COM20020D internal operations 40 MHz & SLOWARB = 0

→Tarb = 125 nS → 5nS

1.4.1 Prerequisites

The bus clock output is specified as the standard for delay time for SH4 AC timing but there are those do not have a minimum delay time specification. In this case, the minimum is determined to be 0 nS. For example, with tRSD within the SH4 AC timing specification, the RD signal transitions at the falling edge of CKIO; however, the RD signal transition can not occur prior to the falling edge of CKIO. (This is because tRSD has a maximum specification of 8 nS and no minimum specification timing.)

1. Write timing (when CKIO = 33 MHz)

With respect to the nWE signal, the address, chip select, and data setup/hold time is satisfied by insertion of 2 waits.

2. Read timing (when CKIO = 33 MHz)

With respect to the rising edge of nRD signal, both the address and chip select/hold timing are in violation. Even if the RBUSTMG is set to 1, the hold for both of these needs to be set to greater than 0 nS. However, the rising edge of nRD and the address, chip select to transition at the same time and their relative positioning can not be guaranteed. Therefore a hold time of greater than 0 nS is not guaranteed. Otherwise, the specified value is satisfied through insertion of 2 waits.

3. Reference [SH433-20.pdf](#) Countermeasures for Read timing violations ([Figure 1.1 Reference Circuit Diagram on page 6](#)).

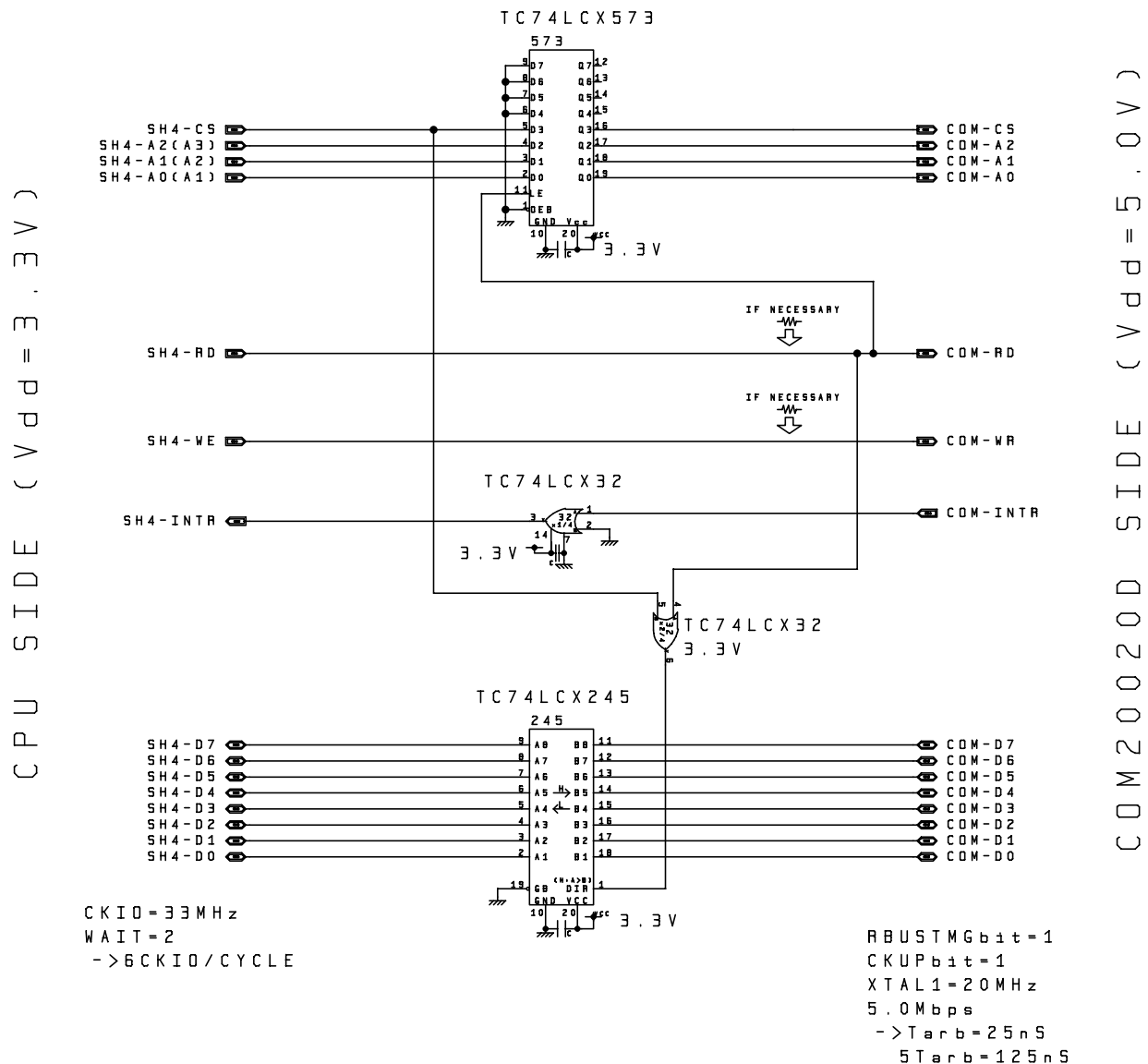


Figure 1.1 Reference Circuit Diagram

Set the RBUSTMG bit = 1 and implement the countermeasures for the address and chip select hold times. In order to resolve the hold time violations, a latch IC is inserted for the address and chip select and maintained during the period that nRD = L. This enables satisfying with a hold time of greater than 0 nS.

However, the D→Q transmission delay time (maximum 8 nS) of the latch IC (TC74LCX573) makes the setup time for the read and write cycles tight. However, the setup time when reading prior to insertion of the latch IC is 52.6 nS and therefore even if this is reduced by 8 nS, there is still a more than sufficient margin. The setup time for writing prior to insertion of the latch IC is 23.3 nS and this reduced by 8 nS is 15.3 nS and barely satisfies the less than 15 nS specification of the COM20020D.

4. Interval time for continuous access

For the access cycle with respect to the COM20020, when 2 waits are inserted, 1 bus cycle becomes 6 clocks. As the CKIO is 33 MHz (roughly 30.3 nS), after insertion of 2 wait cycles, the length of 1 bus cycle is 181 nS. Both the interval for nRD → nRD and nWR → nWR are roughly 181 nS and satisfy 5



Tarb (125 nS @ 5 Mbps). (The reference for a write is the rising edge of nWR and the reference for a Read is the falling edge of nRD.)

Also, the nRD →nWR interval becomes roughly 175 nS and satisfies 5 Tarb.

$(6 \times \text{cyc} + \text{CKOHmin} - \text{RSDmax}) = 6 \times 30.3 + 1 - 8 = 144.5 \text{ nS}$

As the remaining nWR →nRD interval becomes roughly 84 nS, it does not satisfy 5 Tarb.
 $(3 \times \text{cyc} + \text{CKOLmin} - \text{WEDFmax}) = 3 \times 30.3 + 1 - 8 = 83.9 \text{ nS}$

Therefore, a roughly 42 nS ($125 - 83.9 = 41.1 \text{ nS}$) wait using software becomes necessary.

As is shown below, a min. 42 nS software wait is required between completing a write to COM20020 and the start of the read from COM20020.

- Write to COM20020 →wait for 42 nS or more →Read from COM20020.

Tarb expresses the clock signal period being supplied to the dual port RAM inside the COM20020. Also, Tarb is determined by the period of the maximum internal operating clock.

XTAL1 FREQUENCY	CKUP-BIT	TOPR	MAXIMUM TRANSFER RATE	SLOWARB-BIT	TARB
20 MHz	0	50 ns	2.5 Mbps	0	50 ns
20 MHz	1	25 ns	5.0 Mbps	0	25 ns

The CKUP 1, 0 bits are in the setup 2 register and set the "multiplication factor" of the clock multiplication circuit (PLL circuit). (0: x1, 1: x2) The SLOWARB bit is in the setup 1 register and sets whether the clock signal supplied to the dual port RAM is divided in half or not. (0: full speed, 1: half speed) however, for the COM20020, it is fine to leave SLOWARB = 0.

Therefore, for the case Topr = 25

nS, Tarb = 25 nS, 5 Tarb = 5 x 25 nS = 125 nS

5. 5V system and 3.3 V system level conversions

This describes the general precautions for connecting of the COM20020 (5V system) and the SH4 (3.3 V system).

A level conversion buffer is not needed for input of the SH4 output to the COM20020. (However, a pullup internal pin needs a buffer: A1, D0 ~ D7 pins.)

On the other hand, a 5 V to 3.3 V level converter buffer IC must be inserted to input the COM20020 output to the SH4. The nINTR, D0 ~ D7 pins on the COM20020 fulfill this function.

6. Damping resistor

If there is ringing noise that occurs during the falling edge of the COM20020 nRD, nWR signals, insertion of a damping resistor (near 50 Ω) is needed to suppress the ringing. If the ringing voltage appears to exceed 0.5V, then a damping resistor is needed.

7. Dummy write addresses when connecting to a greater than 16 bit width CPU.

For COM20020 CPU interface mode settings, after the hardware reset cancellation, prior to accessing the COM20020, dummy writing to odd number addresses (nCS=H write operation) needs to be performed.

However, special care must be taken for dummy writing when connected to a 16 bit CPU. Odd number addresses are the addresses for the COM20020. In other words, the addresses which cause the COM20020 A0 pin to be set to high are called odd number addresses. When connecting a 16 bit CPU, the A1 pin on the CPU side is shifted to the COM20020D A0 pin for connection, in this case odd number addresses means something different. In this case, dummy write to the addresses causes the CPU A1 pin to go high. For example, the hexadecimal addresses xxx2h, 6h, Ah, and Eh. The CPU

bus type is determined by this dummy write and afterwards the COM20020D registers can be accessed.

Dummy write addresses are the same when connected to a 32 bit CPU. In this case, as the COM20020D A0 pin is connected to the A2 pin on the CPU, the dummy write addresses are hexadecimal xxx4h, Ch.

8. Consideration for the upper limit of the bus clock (CKIO)

The upper limit of the bus clock for this 167 MHz product is roughly 37 MHz. If a higher speed is used, the timing specification for nRD↑ to nWE↓ in the case of write timing is insufficient. This is due to the bus clock CKIO output high level pulse width. In the SH4 specification, the minimum is 1 nS. Here, as there is only 1 nS from CKIO↑ to CKIO↓ the interval specification for the transition edge of a different nRD signal and nWE signal is a disadvantage.

For example, if the CKIO output high level pulse is further extended by 7 nS (width 8 nS), it is possible to set the upper limit of the bus clock to 50 MHz. However, as the CKIO output high level pulse width minimum specification is a specification for the SH4 and therefore we can not make any guarantees and you will need to ensure that the CKIO output high level pulse width is 8 nS or greater.

As another method for providing a bus lock, through using CPLD/FPGA bus timing can be generated and fixed. As SH4 has a synchronized bus, it does not have very good compatibility with the non-synchronized bus of the COM20020. Therefore, use with a CPLD etc. and the most reliable method is to perform synchronized →non-synchronized conversion. On the evaluation board that we have built, a CPLD manufactured by Altec is being used to adjust timing for the "ARC - SH4".

2 Precaution

We have not confirmed operation of the enclosed circuit. Therefore, the customer will need to perform sufficient operation verification.



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