AT91-AN02: Signal Integrity and AT91 Products
(Basic Relationships Between IBIS Data and your PCB)

AT91 ARM Thumb Microcontrollers

Application Note

1. Scope

The purpose of this document is to heighten the customer's awareness of Signal Integrity (SI) issues before the start of a design using an Atmel AT91 ARM® Thumb® microcontroller. All digital device users are potentially impacted by this issue.

The AT91 microcontroller (and all related hardware applications as well) is at once a potential source of perturbation and a potential victim. **Source**, because it is the source of digital activity, but a **Victim** because an embedded PLL, oscillator or ADC all have very small noise margins (for example). The user must pay attention to this last point. The successful cohabitation of the source and victim in the same embedded system (respectively, the digital and the analogical parts) is as critical as electromagnetic compatibility (EMC) certification. To not think of taking steps with SI in mind from the beginning of a design can be expensive at the end of the project.

In the description of the process that follows, the state of the art concerning all the relevant domains is not given. It is assumed that the main rules--such as GND, power supply and decoupling, for example--are known and will be applied to your design. We are dealing with the point-to-point wiring and not with multi-line issues.

This Application Note provides the means to find information, to compute the necessary criteria in order to distinguish critical trace and, subsequently, the remedy and selection strategy.

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2. Terminology

SI: Signal **I**ntegrity, denotes correct timing and quality of the signal.

EMC: Electro **M**agnetic **C**ompatibility, refers to the ability of an electrical device to work satisfactorily in its electromagnetic environment without adversely influencing the surrounding devices, or being influenced by them.

IBIS: Input/output **B**uffer **I**nformation **S**pecification is a behavioral-modeling specification. It is a standard for describing the analog behavior of the buffers of a digital device using plain ASCII-text formatted data. The data in an IBIS file is used to perform **S**ignal **I**ntegrity (SI) simulations of printed circuit boards. The information needed to perform this simulation is buffer voltage-current (V-I) characteristics and switching (output voltage versus time) characteristics.

ADC: Analog-to-**D**igital **C**onverter.

GND: Grou**ND** in electrical circuits

IO: Input and **O**utput words

FR4: is an abbreviation for **F**lame **R**esistant **4**, is a type of material used for making a Printed Circuit Board (PCB). It describes the board itself with no copper covering. FR-4 meets the requirements of Underwriters Laboratories UL94-V0.

PLL: Phase-**L**ocked **L**oop or **P**hase **L**ock Loop.

SDRAM: Synchronous **D**ynamic **R**andom **A**ccess **M**emory.

3. Extracting the Critical Parameters

3.1 Starting the Analysis: The AT91 IBIS Model

The starting point is the electrical specification of the AT91 device output buffers. Atmel provides this specification through a standard IBIS Model file for each device. The IBIS Model file associated with your AT91 product or that of the targeted AT91 microcontroller, can be downloaded from the Atmel web site at; http://www.atmel.com/products/AT91/ then choose the desired device. Next, from the “Tools and Software” section, look up the IBIS file.

Once this file is downloaded, for a knowledgeable person, it is easy to edit the IO electrical specification. Otherwise, you need to download a free IBIS editor available on the internet (just for example, take a look at “Visual IBIS Editor” tool by Mentor Graphics).

3.2 From the IBIS Model: The Interesting Electrical Parameters

Now, with the IBIS file you will extract the rising and falling time pertaining to all Input/Output drivers inside your AT91 microcontroller. This is the only information you need from Atmel to evaluate whether an intrinsic characteristic of a trace will maintain full signal integrity or not.

3.3 Let’s go into Practice

I have downloaded the IBIS Model file for the AT91SAM9260 ARM9-based microcontroller and I am designing the SDRAM clock trace on my PCB. I open this file with an IBIS editor tool and select electrical characteristics of the “SDCK” signal. Now, I am looking at the Rising and Falling Waveforms, and from these curves, I deduce the time delay of the “SDCK” signal slope, between the 10% and 90% points of the final voltage step. I select the nominal curve (for an IO rail supplied at 3.3V) the results are the following:

- The found rising time is equal to 742 ps
- The found falling time is equal to 627 ps

These two physical events are the source of **all** signal integrity problems. It is normal to start from here and take the most critical event, the **falling** edge time, which is shorter than the other.

4. Signal and Trace Behavior

At this level and continuing through this document, Atmel can only give general methods because the bulk of technical information and constraints are known to the user.

In order to be assured signal integrity is sufficient, the following must be respected in descending order of importance:

- First have a fine-tuned working of the whole application
- Have no undesirable effects from the digital parts (the main source) on the on-board low-noise electronic parts (the victim)
- Have no undesirable conducted or transmitted noise originating outside the application (external EMC issue)

4.1 Signal Slope and Critical Trace Length Criteria

As stated in the introduction, it is assumed that the user knows the primary rules of GND, power distribution, decoupling method, static and dynamical noise margins, etc. The working application and PCB design of the digital traces will have a preponderant effect on digital signal integrity. This is why, under some conditions, the trace is considered as a localized or distributed system:

- Localized system, when all the trace points have equal voltage level at any time.
- Distributed system, when the physical size of the trace is greater than the faster electrical event (rising or falling time).

The relationship between the rising (or falling) time and the digital signal imperfection is due to the ratio between the trace propagation time and this rising (or falling) time. Or, by knowing the propagation speed on the trace, this becomes the ratio between the trace length and the rising (T_R) or falling (T_F) time (in our example, the falling time):

- A propagation delay on digital trace < 16% of the T_F provides a “clean” digital signal trace in terms of being without reflection. But we cannot say there will not be overshoot and ringing when that trace is connected to a capacitive load (it is usually the case). We will examine this case when we present the Series Termination method.
- A propagation delay on digital trace equal to 30% of the T_F causes some small ringing on the digital signal trace.
- A propagation delay on digital trace equal to 40% of the T_F causes some ringing on the digital signal trace.
- A propagation delay on the digital trace up to 50% of the T_F can be acceptable.

You must not forget that the 50% criteria can be acceptable for the intrinsic digital signal but not for the whole application, nor to be successful for EMC certification. And inversely, 16% will be the best but that is going to compel you to add termination resistors on a lot of traces. This choice is fully arbitrary.

Note: Often this 50% is assumed to be the limit, over which a trace becomes a distributed system.

Now, we have a time value, T_{PMAX} that will be the maximum allowed propagation time for a trace.

4.2 The Propagation Speed V_P

I have rising/falling time, I have just chosen the maximum propagation delay for a trace: The Propagation Speed V_P. Now, the other needed information is dependent upon the board characteristics. You have to calculate the propagation time (T_P) for each trace and compare this with the previous T_{PMAX} parameter.

In case you do not have a specific software design tool to help the designer in computing this number (T_P) automatically while the board is being designed, the following parameter will be required for a manual computing:

- Physical Composition (FR4: generally glass + resin),
- Trace Layout in term of layers (position of the trace and type of layout: microstrip, stripline, dual stripline),
- Trace geometry (width, thickness) and its come back wire (GND).

Table 4-1 gives standard numbers in terms of propagation delay vs. the material:.

Table 4-1. Example of Propagation Speed

Material	Dielectric Constant	VP (mm/ns)
Air	1	300 (light speed)
Teflon	2.1	212
FR4 (external layer	2.8 to 4.7	141 to 179
FR4 (internal layer)	4.7	141
Aluminium oxide	10	95
Water	80	34

The propagation speed of an electromagnetic wave is inversely proportional to the dielectric constant and is equal to:

$$V_P = \frac{c}{\sqrt{\varepsilon_r}} \quad \textbf{(1)}$$

With:
c as the light speed into space equal to 3.10^8 m/s,

ε_r as the dielectric constant of the material.

Remark:

The external layers always have one side where the dielectric constant is the Air and the other is FR4 (true for both external sides). This is why external layers are used for critical lines, the propagation speed is higher on external layers than on inner layers.

Normal FR4 PCB material has a nominal relative dielectric constant (ε_r) of approximately 4.7 at 1 MHz falling roughly in a linear fashion with increasing frequency to 4.2 at 1 GHz. Actual values of ε_r can vary by ±25%. Controlled ε_r grades of FR4 are available at little or no extra cost, but PCB manufacturers may not use these grades unless specifically requested.

From equation (1), we can deduce the T_P delay which is going to be compared with our previous time criteria T_{PMAX}:

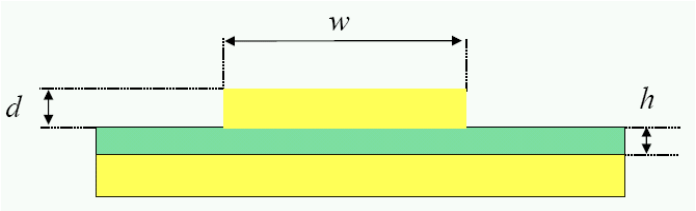
$$T_P = \frac{L_{track}}{V_P} \quad \textbf{(2)}$$

with:
L_{track} as the trace length.

For a trace, if the resulting T_P time is greater than T_{PMAX} then we have to add a termination component on the line.

Below is the microstrip line geometrical representation and the formula for the calculation of its propagation delay:

Figure 4-1. Microstrip Line Parameter



$$T_p \cong 3.35 \times \sqrt{0.475 \times \varepsilon_r + 0.67} \quad \textbf{(3)}$$

- We have the electrical critical timing on the AT91 side and we take into account the falling edge time equal to 627 ps from the AT91SAM9260 IBIS Model,
- Our need, in terms of generated digital noise, compels us to have a low noise level and we have to take 30% ratio according to T_F as criterion for the maximum propagation time (T_{PMAX}). Therefore, with this constraint, the delay limit will be equal to 0.3 x 627 = 188ps.
- The designed trace is on the upper side and the ground plane is immediately below (it is a PCB type microstrip). This trace length is around 56 mm.
- We know the PCB material and its dielectric constant is (FR4) 4.5.

Application: From equation (1), the propagation speed on our board is equal to:

$$V_p = \frac{3.10^8}{\sqrt{4.5}} \cong 141{,}421356 m/s \text{ or } V_p = 141 \text{ mm/ns}$$

The propagation delay on this trace will be equal to: $T_P = \frac{56}{141} = 397 ps$

And the maximum propagation time T_{PMAX}, has been calculated at 188 ps. $T_P = 397 ps > 188 ps$

This propagation delay of the trace is too large. This line should have a specific termination component.

Below Table 4-2, Table 4-3 and Table 4-4 provide three graphs which show maximum trace length with a T_{PMAX} equal to, respectively, 16%, 30% and 50% ratio of the falling time. The x-axis is given in ns and the y-axis in mm. The FR4 outer trace is given with $_r$ equal to 4.5 and the FR4 Inner trace is given with epsilon equal to 4.7.

Table 4-2. T_{PMAX} Equal to 16%

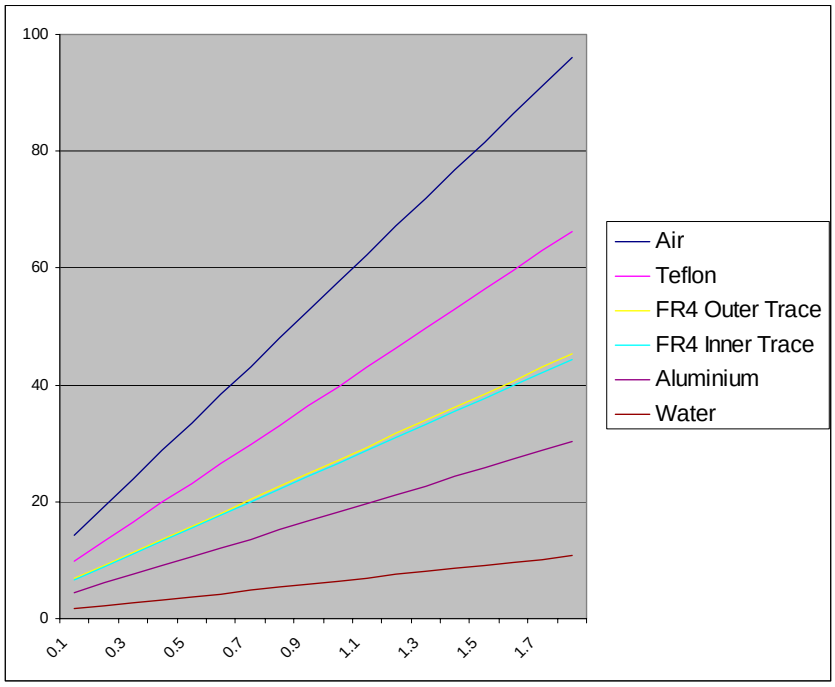


Table 4-3. T_{PMAX} Equal to 30%

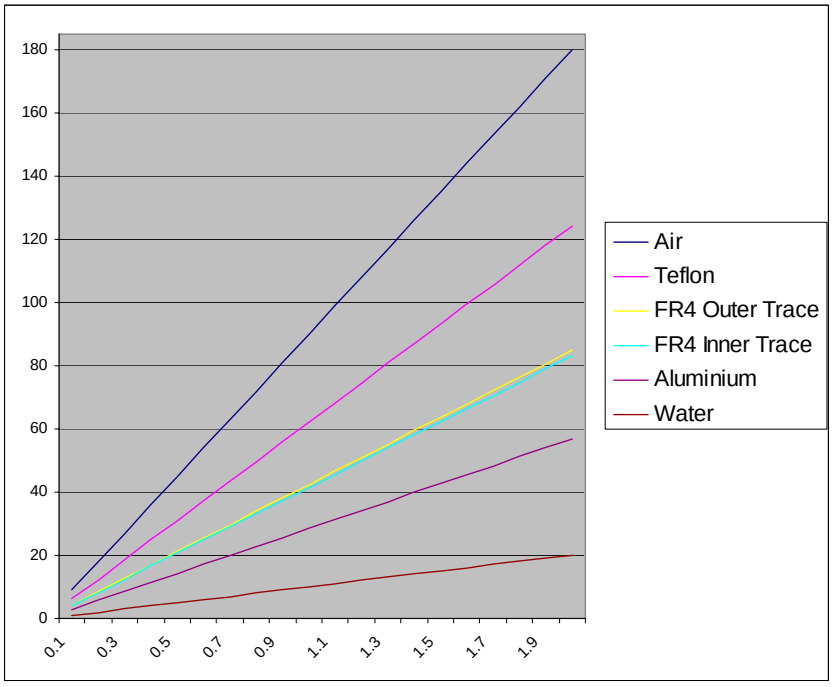
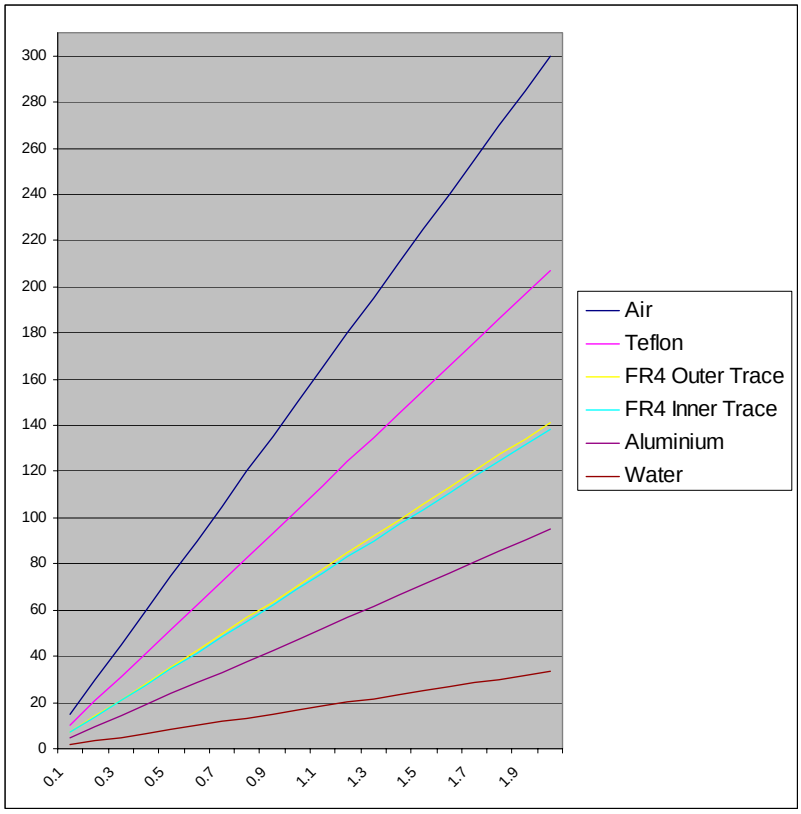


Table 4-4. Worst Case T_{PMAX} Equal to 50%



5. Ending the Line

The paragraphs that follow give some basic rules to determine the different termination methods and how to specify the added component value in order to end the line.

5.1 Impedance of the AT91 Output Buffer

As previously stated we start from the IBIS Model. In this model, the rising and falling behavior are fully specified with an external 50 ohms load resistor. From these curves, it is very easy to calculate the output impedance of a specific driver. For example, as done previously, we calculate the “SDCK” output driver impedance at 3.3 Volts. I take the voltage data on the IBIS curve of the SDCK pad and I have directly residual voltage on the pad when it is supplied at 3.3V and loaded by a 50 Ohms resistor. It is easy to deduce the intrinsic impedance:

$$r_{SDCK} = \frac{3.3-2.82}{2.82} \times 50 = 8.5\Omega$$

5.2 Transmission Line and its Characteristic Impedance

At this step, like the propagation speed, it is the board makeup (layout, material, trace geometry) which define the characteristic impedance of a trace (we call it Z_0). The characteristic impedance of the trace is defined by the following formula:

$$Z_0 = \sqrt{L_n / C_n} \quad \textbf{(4)}$$

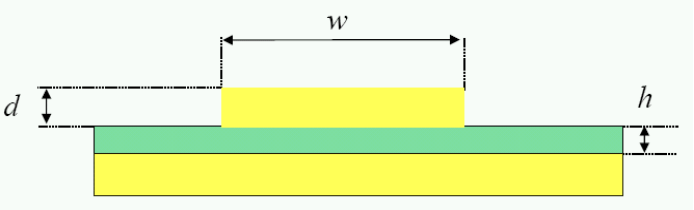
With Z_0 being the characteristic impedance of the trace,

L_n being the Henries per length unit,

C_n being the Farad per length unit.

As you can see, the length of the trace has no effect on this parameter. This characteristic impedance depends only of geometrical trace parameters. Figure 5-1 below is an example of the Microstrip line type and the relationship between the characteristic impedance and the trace parameters:

Figure 5-1. Microstrip Line Parameters



$$Z_0 \cong \frac{87}{\sqrt{\varepsilon_r + 1.41}} . \ln\left(\frac{5.98 \times h}{0.8 \times w + d}\right) \quad \textbf{(5)}$$

We do not expatiate on this subject (like the V_P computing methods) as there are many papers which give relationships, or free tools, to calculate this impedance. But we can give a scale of size about these characteristic impedances which vary, mainly from 50 Ohms to 100 Ohms.

5.3 Termination Strategy

The starting point is based on theory and the study of the reflection factor when an electromagnetic wave propagates and comes across another environment with a different impedance characteristic. In this condition (without giving a detailed account of this domain), a Γ_0 reflection coefficient can be defined by the following formula:

$$\Gamma_1 = \frac{Z_1 - Z_2}{Z_1 + Z_2} \quad \textbf{(6)}$$

Note: This equation gives the reflection coefficient for a voltage edge coming from *Z1* source and going to *Z2* load. *Z1* and *Z2* are both impedances.

As stated previously about the impedance characteristics, we are not going to develop this subject but only give the five termination methods. The goal is to terminate the line with an impedance as close as possible to the characteristic impedance value. In this case, the numerator of the previous equation is zero.

5.3.1 Termination Methods

The five termination methods are listed below and described in the sections that follow:

- Series termination
- Parallel termination
- AC or RC termination

- Thevenin termination
- Diode termination

Each of the five termination methods is defined by:

- A specific topology
- A relative implementation cost
- Bad or good characteristics in terms of timing, consumption

The first termination method described is ideal, for point-to-point connection between two devices, and not only to fix the reflection effect. But in a multi-point connection domain, the user will have to privilege the four other methods.

5.4 Series Termination (A good choice for a point-to-point connection)

To implement this termination method it is enough to fit a serial resistor (R_s) at source level equal to the line characteristic impedance (Z_0). The source termination resistor, R_S, is added to achieve impedance matching between the source (Z_S) and the distributed trace, Z_0. It can also absorb reflection from the load. R_S must be placed as close as possible to the source driver. The value of R_S is the real part in the equation:

$$R_S = (Z_0 - Z_S) \quad \textbf{(7)}$$

The user has to keep this method in mind when obliged to terminate a point-to-point connection between an AT91device pin to another input device pin. As stated previously in Section 4.1 “Signal Slope and Critical Trace Length Criteria” on page 3, having the short trace (with a propagation delay on digital trace < 16% of the T_R or T_F) does not allow us to say there will not be overshoot and ringing on the trace.

In this case, overshoot and ringing occur when the IO output impedance is very small and drives a capacitive load through the trace. In this case, we have a circuitry of the same kind of RLC where:

- R is due (principally) to the driver output impedance
- L is due to the trace characteristic
- C as function of C_{trace} and C_{load}

The trace behavior will depend of quality factor defined by the following formula:

$$Q = \frac{Z_0}{R} \quad \textbf{(8)}$$

Taking a look at the previous example of “SDCK” signal on AT91SAM9260: (Refer to “Section 5.1 “Impedance of the AT91 Output Buffer” on page 7.)

By looking at the scale of sizes, it is easy to understand with the following data:

- An IO output impedance value down to 8.5 Ohms,
- A trace resistance value no more than 0.1 Ohm,
- A trace impedance value 5 times higher than the previous added resistances.

The trace can have a high quality factor and will be the cause of overshoots and the ringing response of the system.

In this case, it is more interesting to use this method (or just forecast footprints on the PCB and fitting a 0 ohm resistor in waiting).

The series termination method is favorable for another intrinsic critical device behavior, it limits the driver current and avoids the ground bounce (or, power rail undershoot) inside the device. Without going into all the details, this is a problem source linked to the simultaneous switching output effect.

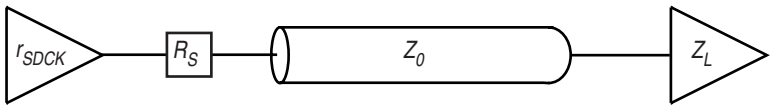
Typically, R_S is equal to approximately 15 to 75. A usual value is a 33 Ohms resistor because it is enough to have a damped system without making the signal timing worse.

An example of the theoretic series termination value:

Previously, we found the “SDCK” output impedance equal to r_{SDCK} = 8.5 Ohms.

By example, after calculating the characteristic impedance of the “sdck” trace, we found 82 Ohms. In order to correctly terminate the line, we have to add, close to the AT91 device SDCK pin, an R_S resistor equal to: $R_S = 82 - 8.5 = 73.5$ Ohms.

Figure 5-2. Schematic



Usually, this value will be too high, because:

– Primarily, because the effect on the timing will be too high.

– The real impedance of the trace is lower than the theoretic impedance due to the ended load.

But, in case there is no constraint at timing level (because IO is used in low frequency domain), then it is necessary to fit a series termination value equal to the theoretic or with a higher value.

Table 5-1. Series Termination Characteristics

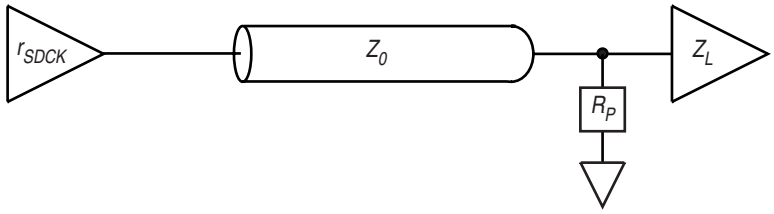
Relative Cost	Delay Added	Power Required	Parameters	Characteristics
Low	Yes	Low	$R_S = Z_0 = R$	Good DC noise margin, however **added delay**

5.5 Parallel Termination

The parallel termination resistor (R_P) is added, so that $R_P // Z_L$ is matched with Z_0 and placed as close as possible to the load termination.

$$R_P = \frac{Z_L \times Z_0}{Z_L - Z_0} \quad \textbf{(9)}$$

Figure 5-3. Schematic



This method is used for a high speed bus because it does not degrade the timing. But this method is not suitable for low power applications, because of the low value of R_P (around 50Ω), and will consume high power (in dynamic and worse in static domain) and requires the source driver to drive a high current.

This method also adds a small delay by $Z_{equi} \times Cl_{oad}$, where $Z_{equi} = R_P // Z_L$ and C_{load} is the input shunt capacitance of the load.

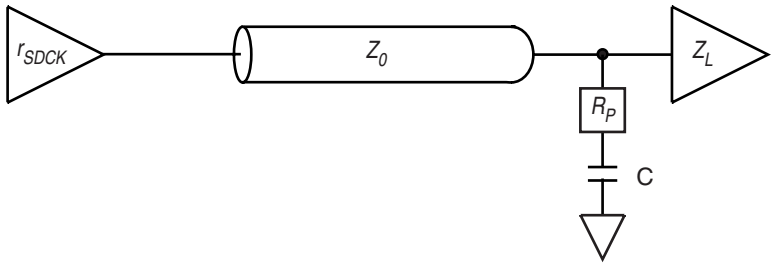
Table 5-2. Parallel Termination Characteristics

Relative Cost	Delay Added	Power Required	Parameters	Characteristics
Low	Small	High	$Z_0 = R_p//Z_L$	Power consumption is a problem

5.6 AC or RC Termination

This is very similar to parallel termination, but with a serial C capacitor added to R_P. This termination method fixes the DC current consumption issue. The R_P value is the same as the parallel termination to provide impedance matching with Z_0, and C provides the drive current to drive the R_P. Therefore, the R_PC termination needs less source-driver current than the parallel termination. The C_P value selection depends on the digital frequency domain on the line: the R_P C_P time constant must be higher than the period of the signal. Of course, it is easy to understand that the introduced Z_C impedance, in serial with R_P, must be smaller than R_P so that, in all frequency domains of the digital signal, $[R_P+Z_C]$ termination network can be approximated to $R_P = Z_0$.

Figure 5-4. Schematic



The power dissipation stays very high.

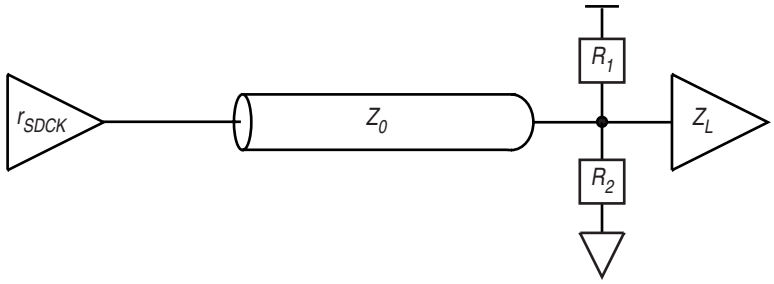
Table 5-3. AC or RC Termination Characteristics

Relative Cost	Delay Added	Power Required	Parameters	Characteristics
Medium	Small	Medium	$R_1 = Z_0$	Check bandwidth and added capacitance

5.7 Thevenin Termination

A closely related variation of the parallel termination strategy is the Thevenin termination. It is formed by the *R1* pull-up and *R2* pull-down resistors, so that the logic high and low can meet the requirement of the destination load.

Figure 5-5. Schematic



The advantages of Thevenin termination are that, in this scheme, the termination resistors also serve as pull-up and pull-down resistors and thereby improve the noise margin of the system. Thevenin termination also reduces the burden on the driver by supplying additional current to the load. This additional current helps the driver, especially in a large voltage-swing system such as 3.3V CMOS based systems. Also, this type of termination provides good overshoot suppression.

One disadvantage of Thevenin termination is that a constant flow of DC from V_{DD} to ground, regardless of the logic state, results in static power dissipation in the termination resistors.

On the one hand, it would appear that the selection of resistor values would be relatively straightforward. The parallel combination of the two resistors must simply be equal to Z_0:

$$Z_0 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \quad \textbf{(10)}$$

By careful observation, it can be inferred that during logic-high state, the Thevenin resistor, R_1, performs pull-up action by supplying current to the load. This current added with the driver's sourcing current is just enough to maintain the voltage at the output of the driver at the minimum threshold-logic voltage, $V_{OH(MIN)}$. Designing V_{TH} in this way minimizes power dissipation in R_1 and R_2.

Table 5-4. Thevenin Termination Characteristics

Relative Cost	Delay Added	Power Required	Parameters	Characteristics
Medium	Small	Medium	$R_1//R_1 = Z_0$	Power consumption is a problem

5.8 Diode Termination

Diode termination is similar to the Thevenin termination, except that the resistors are replaced by diodes, which has a lower power consumption. The D1 and D2 configuration is used to limit overshoots of the reflected signal from the load. The diodes do not affect the line impedance, unlike the Thevenin termination. Schottky and fast switching diodes are good choices to use for this type of termination.

Figure 5-6. Schematic

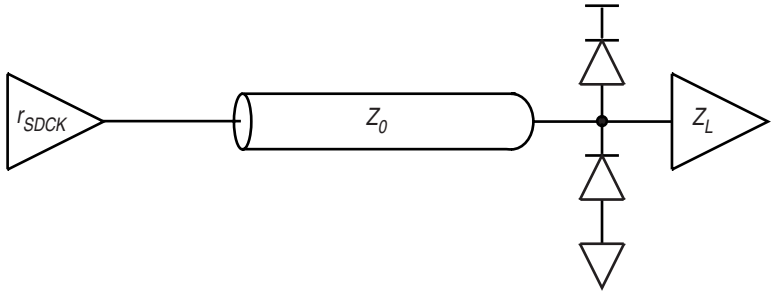


Table 5-5. Thevenin Termination Characteristics

Relative Cost	Delay Added	Power Required	Parameters	Characteristics
High	Small	Low	None	Limits overshoot, some ringing

6. Conclusion

With the evolution of technology on the one hand and the strong constraints in terms of external timing and SI on the other, the customer should not consider a printed circuit board to be perfect and passive equipment but more like a component which might affect the application. With this perspective in view, the IBIS file contains all required data to design a printed circuit board in accordance with the AT91 Input/Output behavior and connected devices through each trace. The IBIS files and PCB electrical data are the starting point to calculate PCB limits and design constraints. But, in case those constraints are too strong, there are corrective actions to take such as correctly ending traces in order to achieve the design.

This application note has shown a means to tackle the SI question around the I/O behavior vs. the PCB criteria.However, this document cannot substitute for dedicated tools such as Hyper-Lynx® by Mentor Graphics or Allegro® PCB SI Foundations by Cadence.

Revision History

Doc. Rev	Comments	Change Request Ref.
6349A	First issue	

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