

Microchip KSZ9131RNX to LAN8830 Migration Guide

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INTRODUCTION

This document is for customers with an existing KSZ9131RNX board design migrating to the LAN8830 for their board design. This features a comparison of hardware and software register specifications between the two products. Details on the hardware and software of each device can be found on each product's Microchip web page.

[Table 1](#) summarizes the hardware attribute differences between the KSZ9131RNX and the LAN8830. [Table 2](#) summarizes the register differences between the KSZ9131RNX and the LAN8830.

TABLE 1: HARDWARE DIFFERENCES BETWEEN KSZ9131RNX AND LAN8830

Device Attribute	KSZ9131RNX	LAN8830
Analog Low Voltage	AVDDL – 1.2V	VDDAL – 1.1V
Digital Low Voltage	DVDDL –1.2V	VDD – 1.1V
MODE Strapping Pins	<p>MODE[3:0]</p> <ul style="list-style-type: none"> – 0100: NAND Tree – 0111: Chip Power Down – 1000: RGMII mode – Advertise 1000BASE-T Full-duplex and 10/100 Half-/Full-duplex. PME on PME_N1. – 1010: RGMII mode – Advertise 1000BASE-T Full-Duplex and 10/100 Half-/Full-duplex). PME on PME_N2. – 1100: RGMII mode – Advertise 1000BASE-T Full-duplex only – 1110: RGMII mode – Advertise 1000BASE-T Full-duplex and 10/100 Half-/Full-duplex 	<p>MODE[4:0]</p> <ul style="list-style-type: none"> – 00100: NAND Tree – 00111: Device Power Down mode – 01000: Chip Power Down – PLL Enabled – 01001: Chip Power Down – PLL Disabled – 10010: RGMII mode – Advertise 1000BASE-T Full-duplex and Half-duplex only, EEE Disabled – 11010: RGMII mode – Advertise 1000BASE-T Full-duplex and Half-duplex only, EEE Enabled – 10000: RGMII mode – Advertise all capabilities (10/100/1000 speed Half/Full-duplex), except 1000BASE-T Half-duplex, EEE Disabled – 11000: RGMII mode – Advertise all capabilities (10/100/1000 speed Half-/Full-duplex), except 1000BASE-T Half-duplex, EEE Disabled <p>Note that PME can map to any GPIO.</p>
PME	Needs mode setting to set LED1/LED2 as PME signal	No mode setting needed to set PME. Registers set the GPIO pin to set as PME signal.
ALL-PHYAD	Pin 38 can be set to respond to the KSZ9131RNX PHY Address (from PHYAD[2:0]) and PHY Address 0.	Pin 13 can be set to respond to the LAN8830 PHY Address (from PHYAD[2:0]) and PHY Address 0.
Fast Link Failure	None	Can indicate link failure in 1 ms when enabled at 100/1000

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TABLE 1: HARDWARE DIFFERENCES BETWEEN KSZ9131RNX AND LAN8830

Device Attribute	KSZ9131RNX	LAN8830
PHYAD Strap Range	PHYAD[2:0]	PHYAD[4:0]
LED Modes	No straps for LED modes	LED mode strap for Individual (PU) and Tricolor (PD)
LED Polarity Control	None	LEDPOL[5:1] available
LEDs	2 LEDs (LED1, LED2)	5 LEDs (LED1, LED2, LED3, LED4, LED5)
GPIOs	None	10 GPIOs (GPIO0-GPIO10)
Shorted-center Tap Magnetic Support	None	MAGJACK Strap
Quiet-WIRE	Supported	No Functionality

TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9131RNX AND LAN8830

Register	KSZ9131RNX	LAN8830
16h	Bits[15:8] – Reserved Bits[7:4] – LED2 Configuration Bits[3:0] – LED1 Configuration	Bits[15:12] – LED4 Configuration Bits[11:8] – LED3 Configuration Bits[7:4] – LED2 Configuration Bits[3:0] – LED1 Configuration
17h	Bits 15, 13, [9:7], [4:2] – Reserved Bits[6:5] – LED Pulse Stretch Enables Bits[1:0] – LED Combination Disables	Bits 15, 13, 9, 4 – Reserved Bits[8:5] – LED Pulse Stretch Enables Bits[3:0] – LED Combination Disables
19h	Bit 15 – Reserved Bit 1 – MDIO Drive Bit 0 – Reserved	Bit 15 – MDIO Buffer Type Bit 14 – INT Buffer Type Bits[13:8] – LED Buffer Type Bit[7] – PME Polarity Bits[5:0] – LED Polarity
1Bh	Bit 15 – Jabber Interrupt Enable Bit 14 – Receive Error Interrupt Bit 13 – Page Receive Interrupt Bit 12 – Parallel Detect Fault Interrupt Bit 11 – Link Partner Acknowledgment Interrupt Bit 10 – Link Down Interrupt Bit 9 – Remote Fault Interrupt Bit 1 – Remote Fault Interrupt	Bits[15:12], 9 – Reserved Bit 11 – Energy Not Detected Interrupt Bit 10 – Energy Detected Interrupt Bit 1 – ADC FIFO Error Interrupt
Address 2, Reg. 1h	Bits[13:8] = Reserved	Bits[13:8] = LED Polarity
Address 2, Reg. 2h	Bits 14, 8, 0 – Reserved Bit 11 – GMII mode with PME_N2 mapped to INT_N Bit 9 – GMII mode with PME_N1 mapped to LED1 Bit 7 – Chip Power-Down Strap Override Bit 4 – NAND Tree Strap Override Bit 1 – GMII/MII Strap Override	Bits 11, 7, 0 – Reserved Bit 14 – MagJack Strap Bit 9 – Software Power Down w/ PLL Disabled Bit 8 – Software Power Down w/ PLL Enabled Bit 4 – NAND Tree Strap Override Bit 1 – GMII/MII Strap Override Bit 0 – RGMII mode

TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9131RNX AND LAN8830

Register	KSZ9131RNX	LAN8830
Address 2, Reg. 3h	Bits 14, 8, 0 – Reserved Bit 11 – GMII mode with PME_N2 mapped to INT_N Status Bit 9 – GMII mode with PME_N1 mapped to LED1 Status Bit 7 – Chip Power-Down Strap Override Status Bit 4 – NAND Tree Strap Override Bit 1 – GMII/MII Strap Status	Bits 11, 7, 0 – Reserved Bit 14 – MagJack Strap Status Bit 9 – Software Power Down w/ PLL Disabled Status Bit 8 – Software Power Down w/ PLL Enabled Status Bit 4 – NAND Tree Strap Override Status Bit 1 – GMII/MII Strap Status Bit 0 – RGMII Strap Status
Address 2, Reg. 40h	Bits[15:0] – Bad SFD Count Lo	Reserved (Not shown)
Address 2, Reg. 41h	Bits[15:0] – Bad SFD Count Hi	Reserved (Not shown)
Address 1C, 0Dh	Bit 15 – LDO Enabled	Bit 15 – LDO Enabled Bits 14:12 – LDO Reference Tune
Address 1F, Reg. 13h	Bit 10 – Quiet-WIRE Enable	Reserved (Not shown)

Additional features, such as EEE, MSE/SQI and self-test for frame generation or checking, are accessible in the Indirect Address Registers.

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APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004742A (09-19-22)	Initial release.	

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