
Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8564 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8564 in a new design. A summary of these items is provided in [Section 10.0, "Hardware Checklist Summary"](#). Detailed information on these subjects can be found in the corresponding sections:

- [Section 2.0, "General Considerations"](#)
- [Section 3.0, "Power"](#)
- [Section 4.0, "Twisted Pair Media Interface"](#)
- [Section 5.0, "SerDes Media Interface"](#)
- [Section 6.0, "QSGMII/SGMII/SerDes MAC Interface"](#)
- [Section 7.0, "Device Clocks"](#)
- [Section 8.0, "Digital Interface and I/O"](#)
- [Section 9.0, "Miscellaneous"](#)

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8564 implementor should have the following documents on hand:

- *VSC8564-11 Data Sheet*
- VSC8564 Evaluation Design Files

These documents can be found at www.microchip.com/VSC8564.

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and RJ45 connector at line side for better EMI and ESD.

VSC8564

3.0 POWER

Table 3-1 shows the power supply pins for VSC8564.

TABLE 3-1: POWER SUPPLY PINS

Name	Pin	Description	Comments
VDD_MDIO	P3	1.2 V or 2.5 V power for SMI pins	Digital, no ferrite bead
VDD1_[1:18]	E5, E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5, M12, N5, N12	1.0V digital core power supply	Digital, no ferrite bead
VDD1A_[1:10]	C7, C8, C9, C13, P6, P7, P8, P9, P10, P11	1.0V analog core power supply. Associated with the QSGMII/SGMII MAC receiver output pins.	Analog, use ferrite bead
VDD25_[1:4]	H13, M4, M13	2.5V general digital power supply. Associated with the LED, GPIO, JTAG, and recovered clock pins.	Digital, no ferrite bead
VDD25A_[1:10]	C2, C4, C6, C11, C14, E4, E13, P5, P12, P13	2.5V general analog power supply	Analog, use ferrite bead
VSS_[1:4]	B1, B16, C5, C12	Ground	—
VSS_[6:68]	D5, D6, D7, D8, D9, D10, D11, D12, E6, E7, E8, E9, E10, E11, F4, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11, M6, M7, M8, M9, M10, M11, N6, N7, N8, N9, N10, N11	Ground	—
VSS_70	R16	Ground	—

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. (See [Table 3-2](#) for different system configuration.) Note that the current values in the table need an additional margin of 25-30%.

TABLE 3-2: MAXIMUM RAIL CURRENTS

Maximum Current Consumption		1V Digital		1V	2.5V	2.5V	Unit
Mode	Interface	Base	w/ MACsec	Analog	Digital	Analog	
Reset	N/A	910	N/A	190	11	4	mA
Power down	N/A	1015	N/A	260	11	23	
1000BASE-T	4-port SGMII	1890	+160	270	15	500	
100BASE-TX	4-port SGMII	1525	+120	245	15	310	
10BASE-T	4-port SGMII	1420	+120	240	15	245	
10BASE-Te	4-port SGMII	1420	+120	240	15	210	
1000BASE-X	4-port SGMII	1430	+160	300	15	25	
100BASE-FX	4-port SGMII	1400	+120	290	15	25	
1000BASE-T	4-port QSGMII	1885	+160	225	15	515	
100BASE-TX	4-port QSGMII	1520	+120	200	15	325	
10BASE-T	4-port QSGMII	1415	+120	195	15	260	
10BASE-Te	4-port QSGMII	1415	+120	195	15	225	
1000BASE-X	4-port QSGMII	1425	+160	255	15	40	
100BASE-FX	4-port QSGMII	1395	+120	245	15	40	

3.2 Power Supply Planes

- The VSC8564 requires two power rails: 2.5V and 1.0V. The filtered analog 1.0V and 2.5V supplies should not be shorted to any other digital supply at the package or PCB level. See [Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"](#).
- The most important PCB design and layout considerations are as follows:
 - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
 - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
 - Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly positioned local decoupling. For more information, see [Section 3.4, "Bulk Decoupling Capacitors"](#).
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Power Circuit Connection and Analog Power Plane Filtering

- The analog power supplies are: VDD25A and VDD1A.
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite

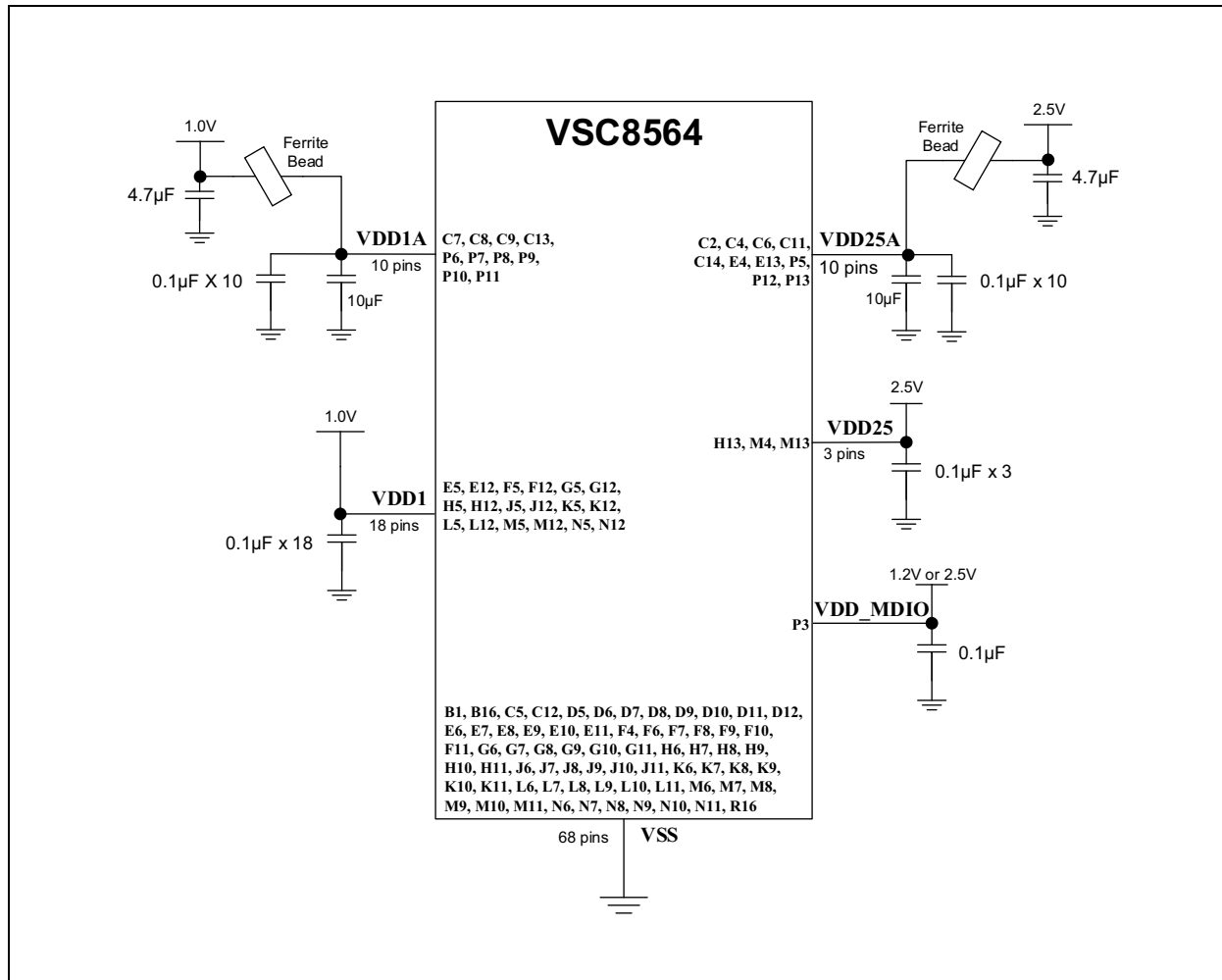
VSC8564

beads with 0Ω resistors once a thorough evaluation of system performance is completed.

- Ferrite beads are not recommended on digital supplies VDD1, VDD25, and VDDMDIO.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Bulk Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8564's power pins for every pin.
- Make sure that bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail of power supply.
- If the VSC8564 device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 TWISTED PAIR MEDIA INTERFACE

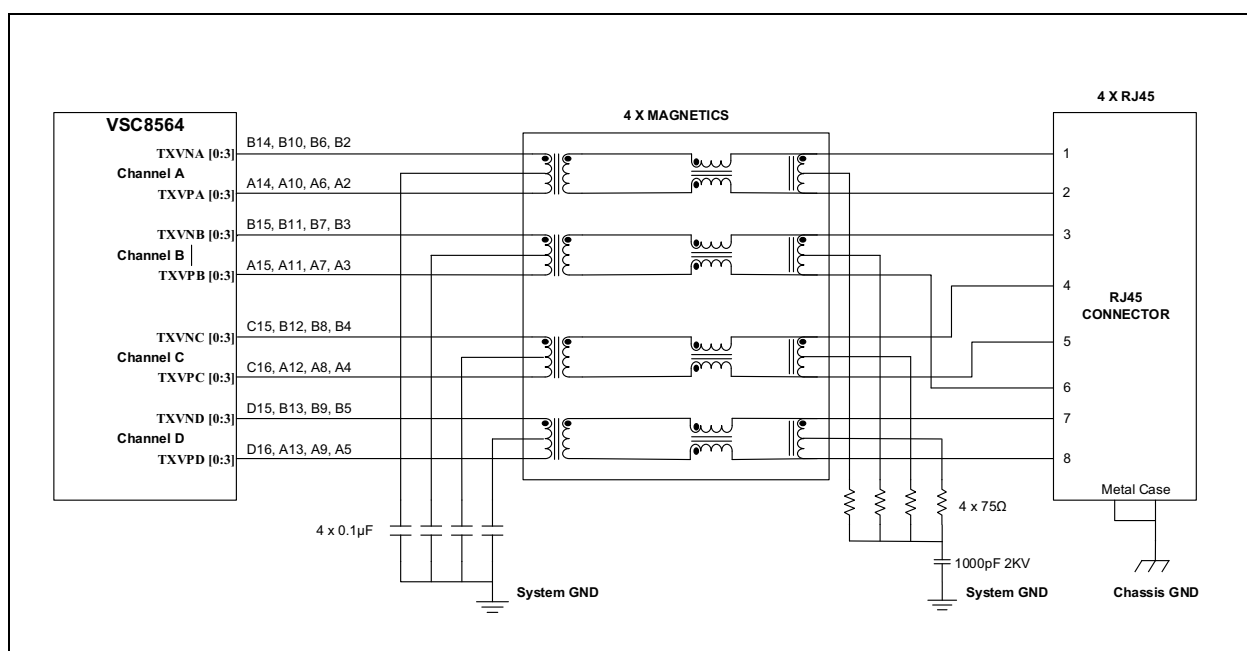
4.1 10/100/1000 Mbps Interface Connection

The VSC8564 has four GPHY ports from PHY 0 to PHY 3 for port 1, port 2, port 3, and port 4. Detailed pin numbers from PHY 0 to PHY 3 sequence and descriptions are as follows:

- **TXVNA [0:3]** (pins B14, B10, B6, and B2): These pins are the transmit/receive negative (–) connection from pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPA [0:3]** (pins A14, A10, A6, and A2): These pins are the transmit/receive positive (+) connection from pair A of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNB [0:3]** (pins B15, B11, B7, and B3): These pins are the transmit/receive negative (–) connection from pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPB [0:3]** (pins A15, A11, A7, and A3): These pins are the transmit/receive positive (+) connection from pair B of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVNC [0:3]** (pins C15, B12, B8, and B4): These pins are the transmit/receive negative (–) connection from pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPC [0:3]** (pins C16, A12, A8, and A4): These pins are the transmit/receive positive (+) connection from pair C of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVND [0:3]** (pins D15, B13, B9, and B5): These pins are the transmit/receive negative (–) connection from pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXVPD [0:3]** (pins D16, A13, A9, and A5): These pins are the transmit/receive positive (+) connection from pair D of the internal PHY 0 to PHY 3. These pins connect to the 10/100/1000 magnetics. No external terminator and bias are needed.

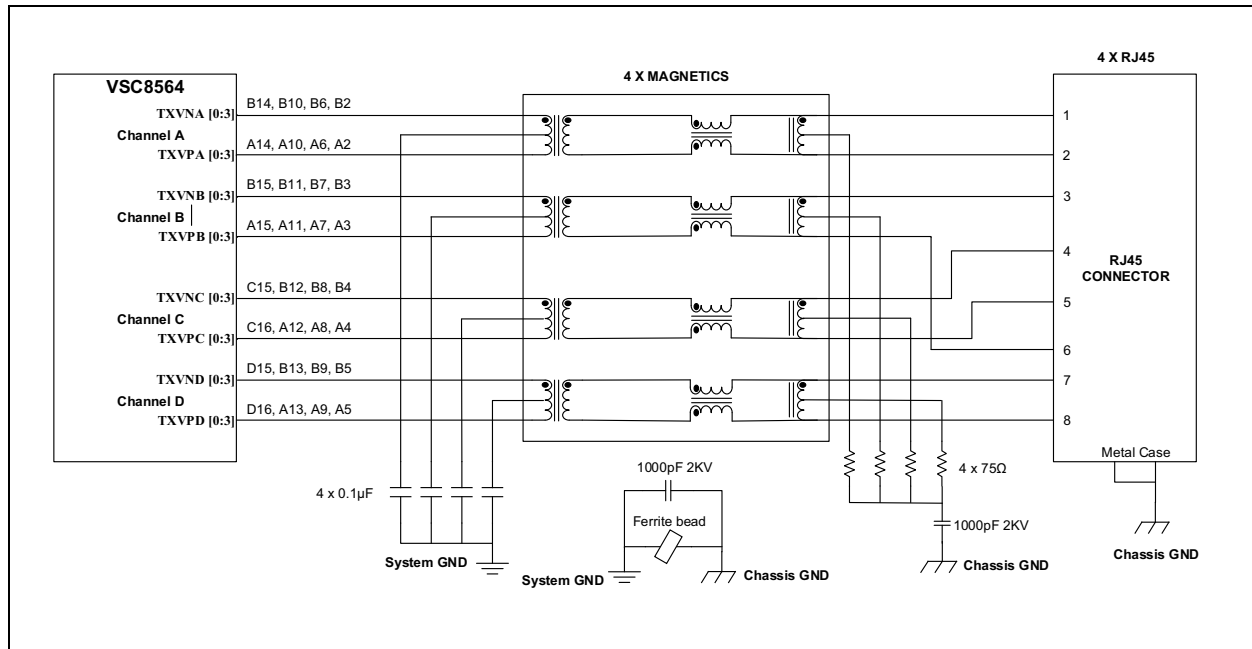
There are two 10/100/1000 Mbps channel connection solutions: (1) Solution #1 is for an external environment with no electrical noise and no ESD to be considered (see [Figure 4-1](#)), and (2) Solution #2 is for an external environment with electrical noise and with ESD to be considered (see [Figure 4-2](#)).

FIGURE 4-1: SOLUTION #1 FOR 10/100/1000 MBPS CHANNEL CONNECTIONS



VSC8564

FIGURE 4-2: SOLUTION #2 FOR 10/100/1000 MBPS CHANNEL CONNECTIONS



4.2 10/100/1000 Magnetics Connection and RJ45 Connection

- The center tap connection on the VSC8564 side for Pair A channel only connects a 0.1 μ F capacitor to GND. No bias is needed.
- The center tap connection on the VSC8564 side for Pair B channel only connects a 0.1 μ F capacitor to GND. No bias is needed.
- The center tap connection on the VSC8564 side for Pair C channel only connects a 0.1 μ F capacitor to GND. No bias is needed.
- The center tap connection on the VSC8564 side for Pair D channel only connects a 0.1 μ F capacitor to GND. No bias is needed.
- The center taps of the magnetics of all four pairs should not be connected together without the 0.1 μ F capacitors to ground. The reason is the Common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75 Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required for each PHY. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground, it is shared by PHY 0, PHY 1, PHY 2, and PHY 3 for port 1, port 2, port 3, and port 4.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See [Section 4.3, "PCB Layout Considerations"](#) for guidance on how chassis ground should be created from system ground.
- For the magnetics selection, please refer to magnetics suggested guidelines (*ENT-AN0098 Magnetics Guide* on Microchip Technology product page) for reference.

4.3 PCB Layout Considerations

- All differential pairs of the MDI interface traces should have a characteristic impedance of 100 Ω to the GND plane. This is a strict requirement to minimize return loss requiring the PCB designer and FAB house.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI and crosstalk. Each port of pairs A, B, C, and D should match in length to prevent delay mismatch that would cause common-mode noise.
- Ideally, there should be no crossover or via on the signal paths.
- Incorporate a 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor or ferrite bead far away from the VSC8564 device or other sensitive devices in the PCB layout placement for better ESD.

5.0 SERDES MEDIA INTERFACE

5.1 Fiber and Copper SFP Interface Pins and Descriptions

- The VSC8564 device SerDes media interface supports 1000BASE-X fiber ports with 1000BASE-X family SFPs, or 100BASE-FX fiber ports with 100BASE-FX SFPs, or 10/100/1000BASE-T copper ports with 10/100/1000BASE-T copper SFPs.
- For the details of SFP-related pin numbers and descriptions of the SerDes media interface, see [Table 5-1](#). For SerDes media SFP interface connections, see [Figure 5-1](#) and [Figure 5-2](#).

TABLE 5-1: SFP-RELATED PIN NUMBERS AND DESCRIPTIONS FOR SERDES MEDIA INTERFACE

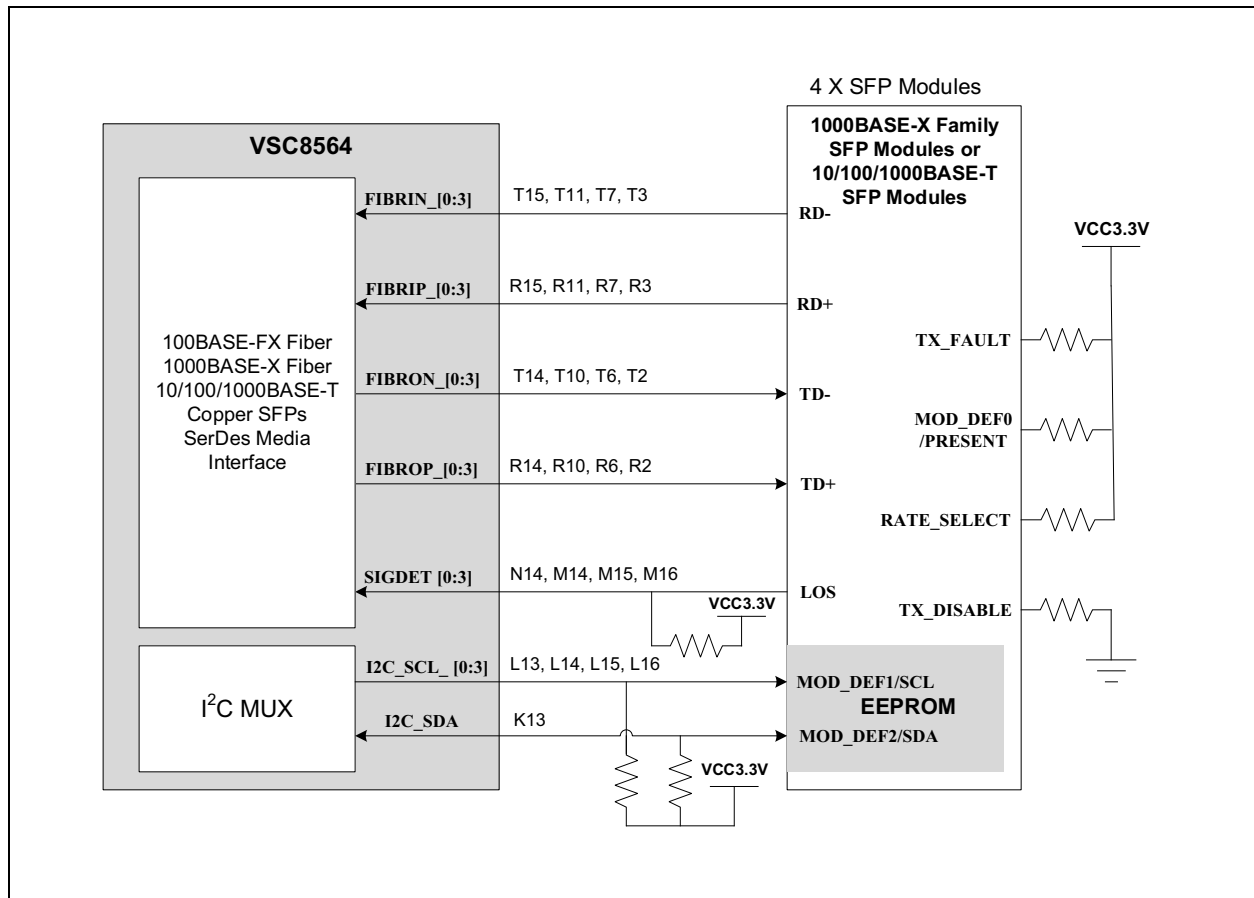
Pin Name	Pin Number	Type	Description
SerDes Media Interface Pins			
FIBRIN_[0:3]	T15, T11, T7, T3	Input	SerDes media interface receiver input pairs
FIBRIP_[0:3]	R15, R11, R7, R3	Input	
FIBRON_[0:3]	T14, T10, T6, T2	Output	SerDes media interface transmitter output pairs
FIBROP_[0:3]	R14, R10, R6, R2	Output	
SIGDET [0:3]	N14, M14, M15, M16	Input	If SIGDET is used as signal detect for SFP
I²C Two-Wire Serial Controller Pins			
I2C_SCL_[0:3]	L13, L14, L15, L16	Output	I ² C two-wire serial controller clock pins
I2C_SDA	K13	I/O	I ² C two-wire serial controller data pin

5.2 SerDes Media Interface Connecting to 1000BASE-X Fiber or 1000BASE-T Copper SFPs

To connect the VSC8564 device to a 1000BASE-X fiber SFP or 10/100/1000BASE-T copper SFP, use the following guidelines and reference schematic:

- The RD+/- and TD+/- differential pairs must be able to perform 100Ω impedance control in the PCB layout and FAB.
- The SIGDET input pin of the PHY should be connected to the LOS output pin of the SFP connector.
- The MII register should be set to 19E.0 = 1 in order to set the SIGDET pin to active-low. This will set the pin to properly receive the LOS behavior without additional glue logic.
- The SFP's Present, SCL, SDA, TX_DIS, TX_FAULT, and RX_LOS signals may be connected to the Switch/MAC/ASIC or the GPIO pins of the VSC8564. If using multiple SFPs, it may be best to implement an I²C controller as all SFP devices have an I²C address = 00000.
- One of the port LED pins should be used and LINK/ACTIVITY be selected and connected to the CATHODE pin of an LED. This can be used to indicate when the SFP is linked and has data activity present.
- If there is no 0.1 μF AC coupling capacitors in SFP, then four external 0.1 μF AC coupling capacitors must be added for RD+/- and TD+/- differential pairs. Usually, almost all SFPs have internal termination resistors and AC coupling capacitors.
- All pull-up resistors should have a value between 4.7 kΩ to 10 kΩ.

FIGURE 5-1: SERDES MEDIA INTERFACE TO 1000BASE-X FAMILY FIBER SFP OR 10/100/1000BASE-T COPPER SFP REFERENCE CONNECTION

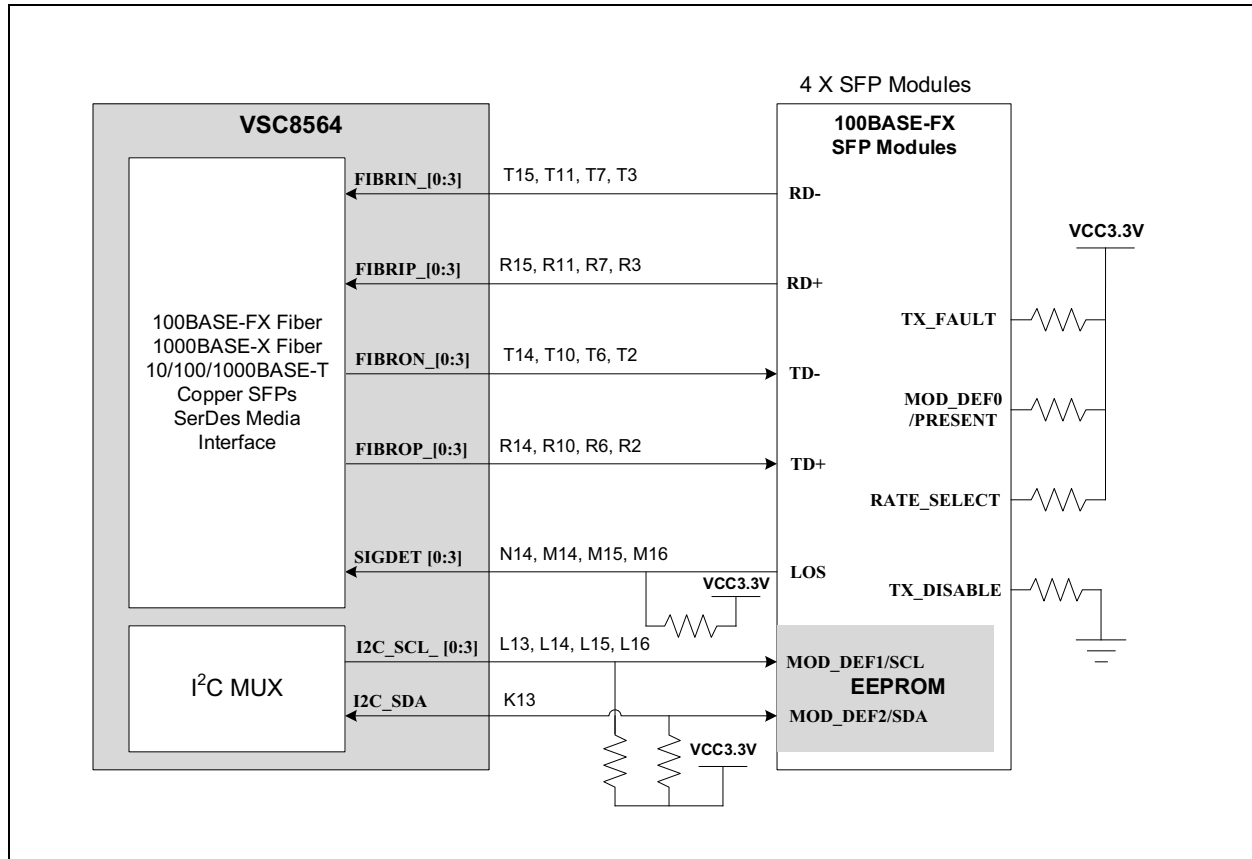


5.3 SerDes Media Interface Connecting to 100BASE-FX Fiber SFPs

To connect VSC8564 device to a 100BASE-FX fiber SFP, use the following guidelines and reference schematic:

- The RD+/- and TD+/- differential pairs must be able to perform 100Ω impedance control in the PCB layout and FAB.
- The **SIGDET** input pin of the PHY should be connected to the **LOS** output pin of the SFP connector.
- The MII register should be set to 19E.0 = 1 in order to set the **SIGDET** pin to active-low. This will set the pin to properly receive the LOS behavior without additional glue logic.
- The SFP's Present, SCL, SDA, TX_DIS, TX_FAULT, and RX_LOS signals may be connected to the Switch/MAC/ASIC or the GPIO pins of the VSC8564. If using multiple SFPs, it may be best to implement an I²C controller as all SFP devices have an I²C address = 00000.
- If there are no **TX_FAULT** and **RATE_SELECT** pins on some of 100BASE-FX SFPs or they are invalid pins, they should be left not connected.
- One of the port LED pins should be used and LINK/ACTIVITY be selected and connected to the CATHODE pin of an LED. This can be used to indicate when the SFP is linked and has data activity present.
- If there is no 0.1 μF AC coupling capacitors in SFP, four external 0.1 μF AC coupling capacitors must be added for RD+/- and TD+/- differential pairs. Usually, almost all SFPs have internal termination resistors and AC coupling capacitors.
- All pull-up resistors should have a value between 4.7K kΩ to 10 kΩ.

FIGURE 5-2: SERDES MEDIA INTERFACE WITH FOUR 100BASE-FX FIBER SFP MODULES



6.0 QSGMII/SGMII/SERDES MAC INTERFACE

6.1 QSGMII/SGMII/SerDes MAC Pins and Connection

- The VSC8564 device supports one QSGMII MAC, four SGMII MACs, or four SerDes MACs.
- For detailed pin numbers and description and connection of QSGMII/SGMII/SerDes MAC interface, see [Table 6-1](#) and [Figure 6-1](#) to [Figure 6-3](#).

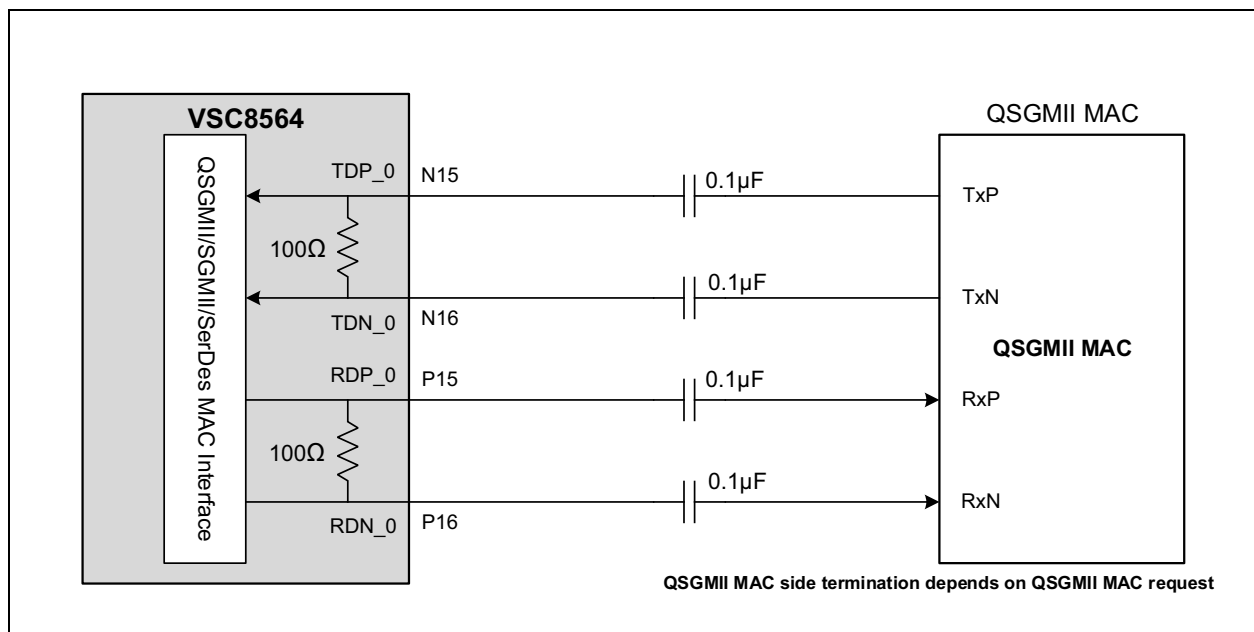
TABLE 6-1: QSGMII/SGMII/SERDES INTERFACE PINS

Pin Name	Pin Number	Type	Description
RDN_[0:3]	P16, T12, T8, T4	Output	QSGMII/SGMII/SerDes MAC receiver output pairs
RDP_[0:3]	P15, R12, R8, R4	Output	
TDN_[0:3]	N16, T13, T9, T5	Input	QSGMII/SGMII/SerDes MAC transmitter input pairs
TDP_[0:3]	N15, R13, R9, R5	Input	

6.2 QSGMII MAC

- The VSC8564 device supports a QSGMII MAC to convey four ports of network data and port speed from 10/100/1000 Mbps.

FIGURE 6-1: QSGMII MAC INTERFACE CONNECTIONS

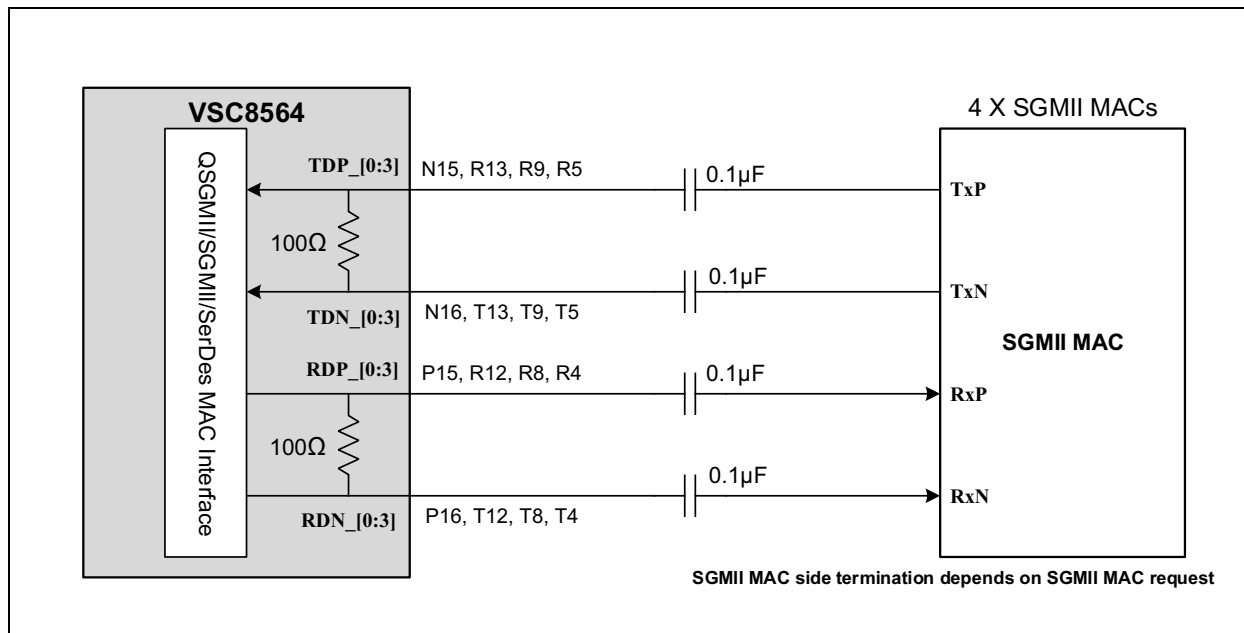


6.3 SGMII MAC

- When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8564 device can be connected to an SGMII-compatible MAC.

VSC8564

FIGURE 6-2: SGMII MAC INTERFACE CONNECTIONS



6.4 SerDes MAC

- When connected to a SerDes MAC compliant to 1000BASE-X, the VSC8564 device provides data throughput at a rate of 1000 Mbps only; 10 Mbps and 100 Mbps rates are not supported.
- [Figure 6-3](#) shows the SerDes MAC interface connection. [Figure 6-4](#) shows the SerDes MAC interface connection to 1000BASE-X SFP or 1000BASE-T SFP.

FIGURE 6-3: SERDES MAC INTERFACE CONNECTIONS

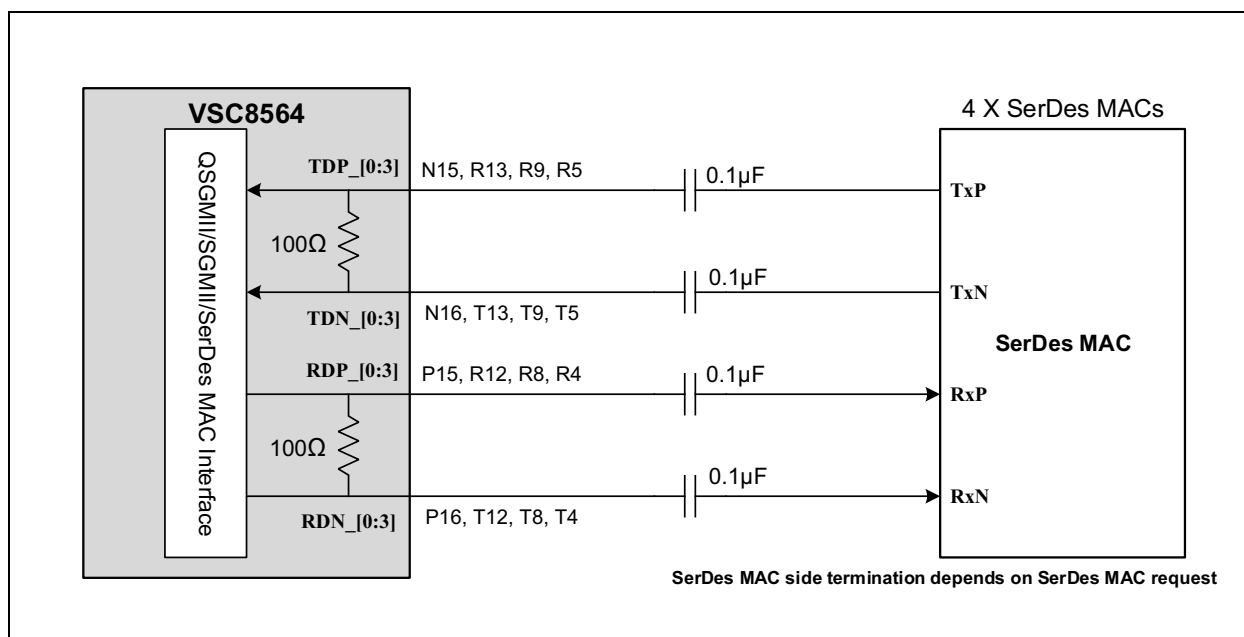
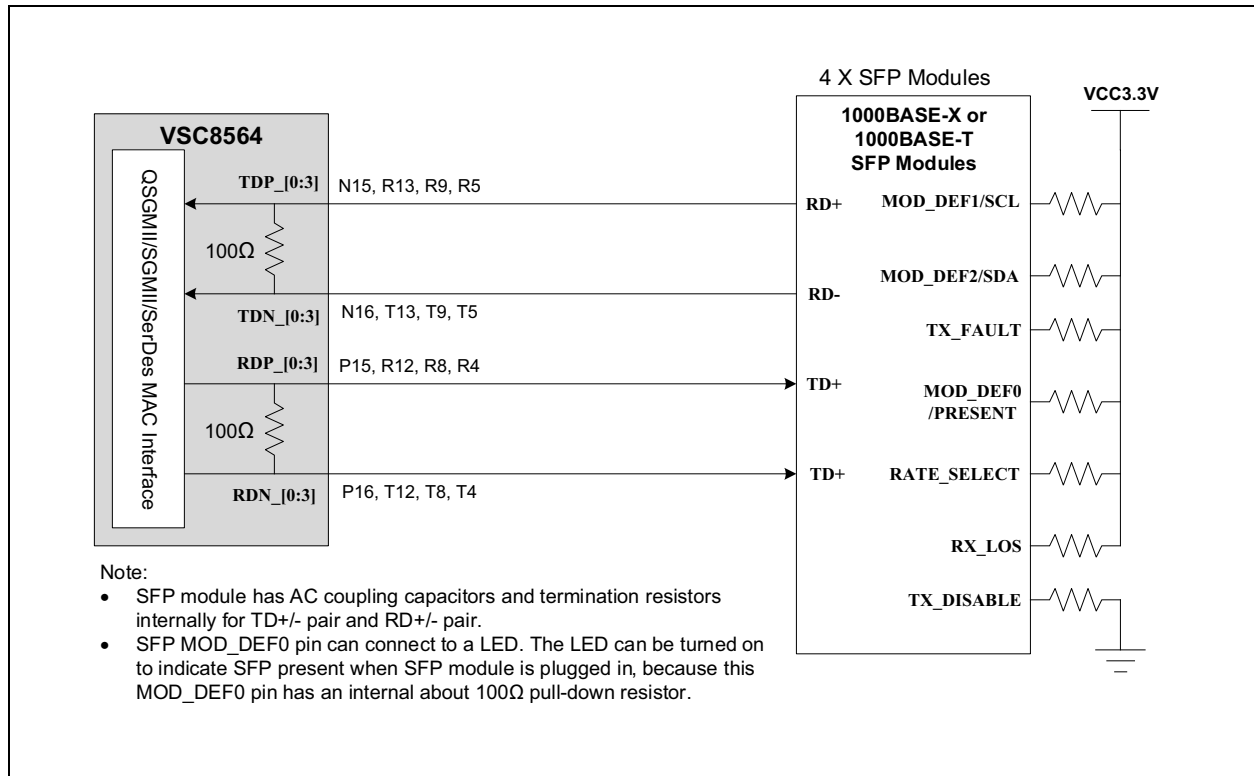


FIGURE 6-4: SERDES MAC INTERFACE TO 1000BASE-X SFP OR 1000BASE-T SFP CONNECTION



6.5 QSGMII/SGMII/SerDes MAC Design Rules

- Use AC coupling with 0.1 μF capacitors for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or strip-line).
- Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
- Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
- Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce crosstalk between differential pairs. Minimum spacing of three times the ground plane gap is required.
- Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
- Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
- If the SGMII/SerDes port is unused, both the RD_x pair and TD_x pair pins can be left floating (No Connect).

VSC8564

7.0 DEVICE CLOCKS

7.1 Reference Clock

- The device reference clock supports both 25 MHz and 125 MHz clock signals. The reference clocks can be either differential or single-ended. If differential, they must be capacitively coupled and LVDS-compatible.
- Refer to [Table 7-1](#) for the reference clock pins and system clock frequency selection.

TABLE 7-1: REFERENCE CLOCK PINS

Pin Name	Pin Number	Type	Description
REFCLK_P	D1	ADIFF	Differential reference clock input pair
REFCLK_N	C1	ADIFF	
REFCLK_SEL2	E1	I, PU	Selects the reference clock speed: 0: 25 MHz (Pull down to VSS) 1: 125 MHz (Default or pull up to 2.5V) Use 125 MHz for typical applications.

When reference clocks are used, ensure that:

- The jitter requirements in the data sheet are met.
- The amplitude specifications in the data sheet are met.
- The traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- AC coupling with 0.1 μF capacitors is used. Capacitors are best placed close to the reference clock input pins.
- For some clock drivers, the termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the VSC8564 side of the capacitors.
- All reference clocks must be free from glitches or must be hitless.
- For QSGMII operation of the PHY, 25 MHz reference clock is not recommended.

7.2 Single-Ended REFCLK Input

To use a single-ended reference clock, an external resistor network is required. The purpose of the network is to limit the amplitude and to adjust the center of the swing. The configurations for a single-ended REFCLK, with the clock centered at 1V and a 500 mV peak-to-peak swing, are shown in [Figure 7-1](#).

FIGURE 7-1: SINGLE-ENDED REFCLK INPUT RESISTOR DIVIDER

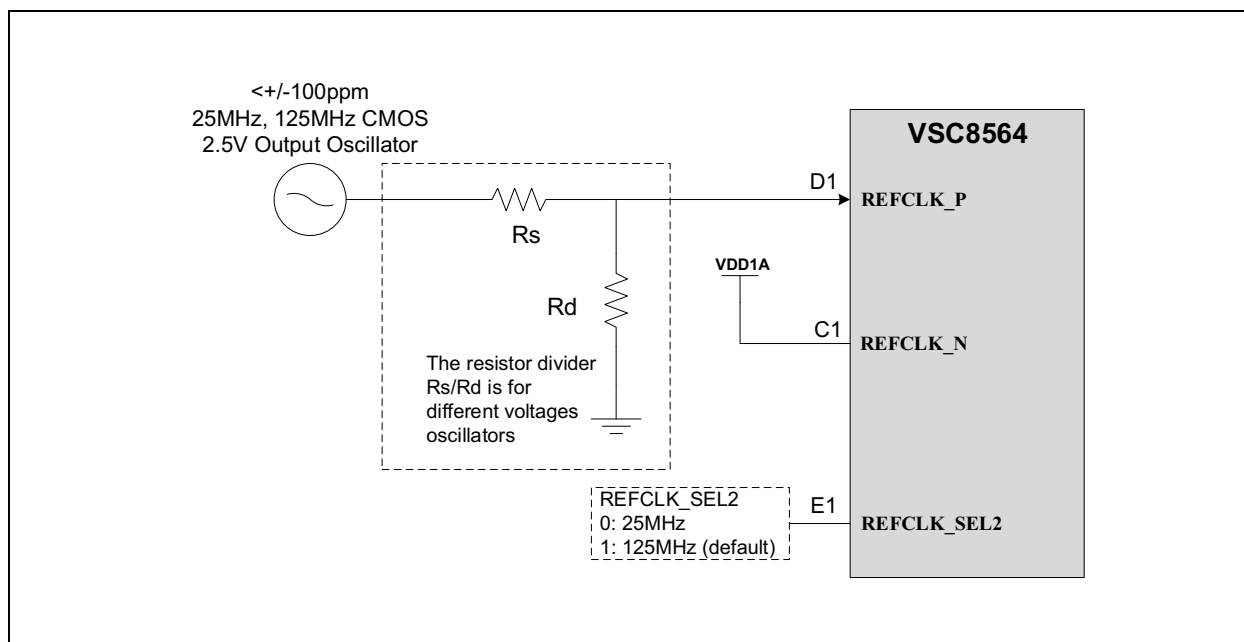


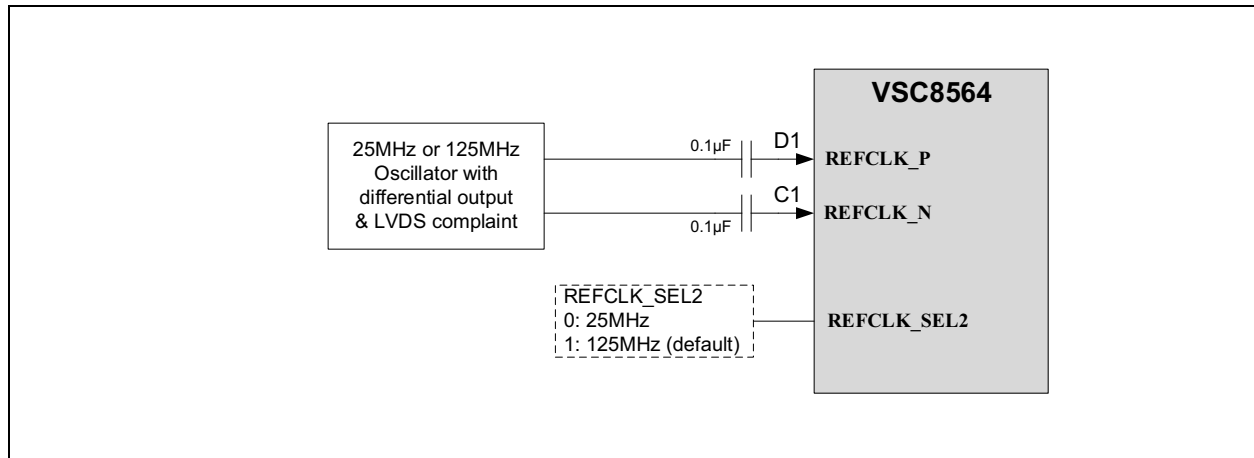
TABLE 7-2: SINGLE-ENDED REFCLK INPUT RESISTOR DIVIDER

Oscillator CMOS Output Voltage	Resistor Divider Rs Value (Ω)	Resistor Divider Rd Value (Ω)
2.5V	220	910
3.3V	270	430
5V	430	300

7.3 Differential REFCLK Input

AC coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS compatible. [Figure 7-2](#) shows the configuration.

FIGURE 7-2: AC COUPLING FOR REFCLK DIFFERENTIAL INPUT

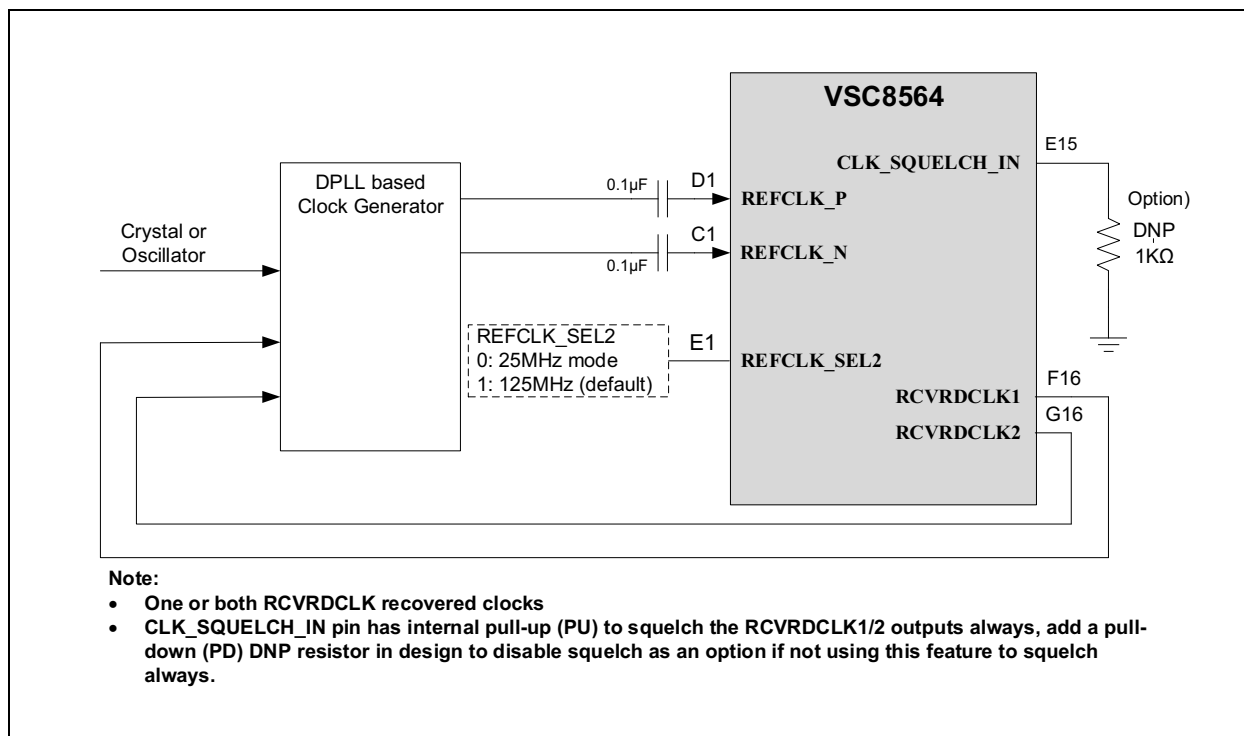


7.4 Media Recovered Clock Output

For Synchronous Ethernet applications, the VSC8564 includes two recovered clock output pins.

- **RCVRDCLK1** (pin F16) is controlled by register 23G. The clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz. The recovered clock pins are synchronized to the clock of the active media link. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
- **RCVRDCLK2** (pin G16) is controlled by register 24G. The clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz. The recovered clock pins are synchronized to the clock of the active media link. This pin is not active when NRESET is asserted. When disabled, the pin is held low.
 - To enable recovered clock output, set register 23G or 24G, bit 15 to 1. By default, the recovered clock output pins are disabled and held low, including when NRESET is asserted. Registers 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz or 125 MHz), and squelch conditions.
- **CLK_SQUELCH_IN** (pin E15) is the input control to squelch the recovered clock. Use registers 23G or 24G, bits 5:4 to configure the clock squelch criteria. These registers can also disable the squelch feature. The **CLK_SQUELCH_IN** pin controls the squelching of the clock. Both **RCVRDCLK1** and **RCVRDCLK2** are squelched when the **CLK_SQUELCH_IN** pin is high. This pin should not be left floating when using Synchronous Ethernet applications.
- For using Synchronous Ethernet applications, see [Figure 7-3](#) for reference.

FIGURE 7-3: TYPICAL SYNCHRONOUS ETHERNET CLOCK CONFIGURATION



8.0 DIGITAL INTERFACE AND I/O

8.1 Serial Management Interface (SMI) Pins

- The VSC8564 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its **MDC** and **MDIO** pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.
- Energy Efficient Ethernet (EEE) control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For information, see the *VSC8564 Data Sheet*.
- The SMI is a synchronous serial interface with input data to the VSC8564 on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2 kΩ pull-up resistor is required on the MDIO pin. See [Table 8-1](#) for SMI interface pin numbers and more information.

TABLE 8-1: SMI INTERFACE PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
MDC	P2	I, PD	A maximum of 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
MDIO	N2	I/O, TS	Management data input/output pin (TS, Tri-State). Serial data is written or read from this pin bidirectionally between the PHY and Station Manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the Station Manager, and its value depends on the MDC clock frequency and the total sum of the capacitive loads from the MDIO pins.
MDINT	M2	I/O, OD, OS	Management interrupt signal. Upon reset the device will configure these pins as active-low (OD, open drain) or active-high (OS, open source) based on the polarity of an external 10 kΩ resistor connection. These pins can be tied together in a wired-OR configuration with only a single pull-up or pull-down resistor.

8.2 GPIO Pins

- VSC8564 provides 15 multiplexed general-purpose input/output (GPIO) pins. All device GPIO pins and their behavior are controlled using registers. [Table 8-2](#) shows an overview of the register controls for GPIO pins.
- These GPIO pins have internal pull-up (PU). Any unused GPIO pins can be left floating (No Connect).

TABLE 8-2: GPIO PINS AND REGISTER BITS FOR GPIO CONTROL

Pin Name	Pin Number	GPIO_Control	GPIO Input	GPIO Output	GPIO Output Enable	Alternative Use
GPIO0	N14	13G [1:0]	15G.0	16G.0	17G.0	SIGDET0
GPIO1	M14	13G [3:2]	15G.1	16G.1	17G.1	SIGDET1
GPIO2	M15	13G [5:4]	15G.2	16G.2	17G.2	SIGDET2
GPIO3	M16	13G [7:6]	15G.3	16G.3	17G.3	SIGDET3
GPIO4	L13	13G [9:8]	15G.4	16G.4	17G.4	I2C_SCL_0
GPIO5	L14	13G [11:10]	15G.5	16G.5	17G.5	I2C_SCL_1
GPIO6	L15	13G [13:12]	15G.6	16G.6	17G.6	I2C_SCL_2
GPIO7	L16	13G [15:14]	15G.7	16G.7	17G.7	I2C_SCL_3
GPIO8	K13	14G [1:0]	15G.8	16G.8	17G.8	I2C_SDA

Note 1: For all GPIO-related register bits in the table, defaults are '0' or '00', and write '1' or '11' is valid.

VSC8564

TABLE 8-2: GPIO PINS AND REGISTER BITS FOR GPIO CONTROL (CONTINUED)

Pin Name	Pin Number	GPIO_Control	GPIO Input	GPIO Output	GPIO Output Enable	Alternative Use
GPIO9	K14	14G [3:2]	15G.9	16G.9	17G.9	FASTLINK_FAIL
GPIO10	K15	14G [5:4]	15G.10	16G.10	17G.10	—
GPIO11	K16	14G [7:6]	15G.11	16G.11	17G.11	—
GPIO12	J14	14G [15:14]	15G.12	16G.12	17G.12	—
GPIO13	H14	14G [15:14]	15G.13	16G.13	17G.13	—
GPIO14	E16	N/A	N/A	N/A	N/A	—

Note 1: For all GPIO-related register bits in the table, defaults are '0' or '00', and write '1' or '11' is valid.

8.3 JTAG Pins

- If JTAG is not used, **TRST** should be pulled low. The other pins may be left floating (No Connect). See [Table 8-3](#) for JTAG pin information.

TABLE 8-3: JTAG PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
TCK	F3	I, PU	Boundary scan, test clock input. Internally pulled high.
TDI	F2	I, PU	Boundary scan, test data input. Internally pulled high.
TDO	F1	O	Boundary scan, test data output
TMS	E2	I, PU	Boundary scan, test mode selection. Internally pulled high.
TRST	E3	I, PU	Boundary scan, test Reset input. Internally pulled high. Note: When JTAG is not in use, this pin must be tied to ground with a pull-down resistor for normal operation.

9.0 MISCELLANEOUS

9.1 Reset

- The VSC8564 must be reset at power-up. One option is to hold **NRESET** low for a minimum 2 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **NRESET** low for a minimum 100 ns after power-up. **NRESET** is typically driven by a voltage monitor device or by the management processor or FPGA. See [Table 9-1](#) for more information on this pin.

TABLE 9-1: RESET PIN DESCRIPTION

Pin Name	Pin Number	Type	Description
NRESET	M3	I, PD	Device reset. Active low input that powers down the device and sets all register bits to their default state.

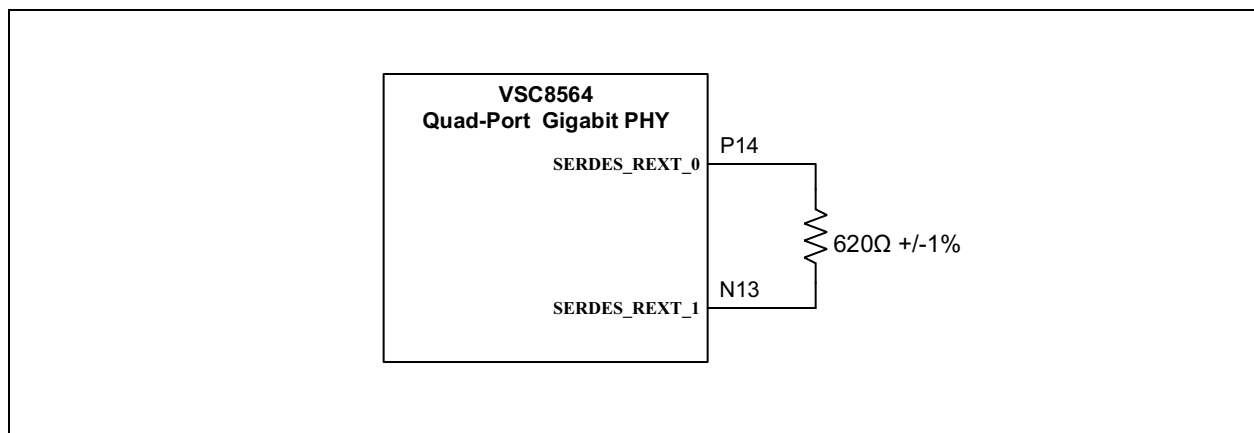
9.2 Reference Resistor

- Connect a $620\Omega \pm 1\%$ resistor between **SERDES_REXT_0** and **SERDES_REXT_1** as shown in [Figure 9-1](#). See [Table 9-2](#) for additional details on the pins.

TABLE 9-2: REFERENCE RESISTORS DESCRIPTIONS

Pin Name	Pin Number	Type	Description
SERDES_REXT_0	P14	ABIAS	SerDes bias pins. Connect to a 620Ω 1% resistor.
SERDES_REXT_1	N13	ABIAS	

FIGURE 9-1: SERDES BIAS RESISTOR



VSC8564

9.3 LED Pins

- The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed using register 17E2, bits [13:10]. The default polarity is active low. The register 25G, register 29 and 30 can be configured for different LED modes.
- The VSC8564 LED pins are for quad-port status; refer to [Table 9-3](#) for all indicator LED pins.
- Using 330Ω to 510Ω current limit resistor is recommended and VDD25 for LED power.

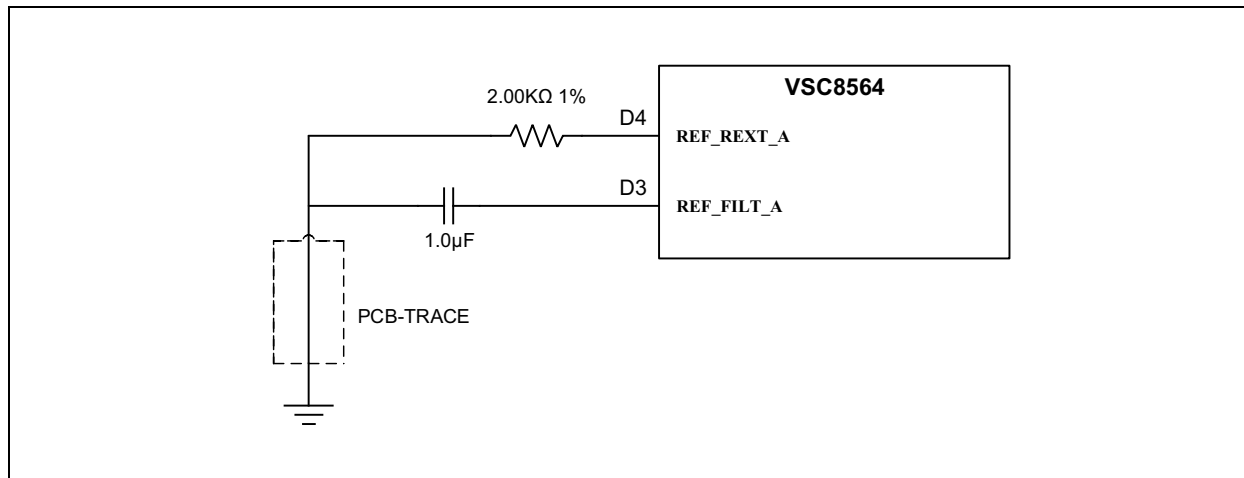
TABLE 9-3: LED PINS AND BASIC DEFAULT FUNCTION

Pin Name	Pin Number	Type	Description
LED0_[0:3]	G1, H1, J1, K1	O	LED0 is for PHY [0:3]. LED0 default is LED mode 1 for link 1000/Activity and can be changed by register 29 bits [3:0].
LED1_[0:3]	G2, H2, J2, K2	O	LED1 is for PHY [0:3]. LED1 default is LED mode 2 for link 100/Activity and can be changed by register 29 bits [7:4].
LED2_[0:3]	G3, H3, J3, K3	O	LED2 is for PHY [0:3]. LED2 default is LED mode 0 for link/Activity and can be changed by register 29 bits [11:8].
LED3_[0:3]	G4, H4, J4, K4	O	LED3 is for PHY [0:3]. LED3 default is LED mode 8 for Duplex/Collision and can be changed by register 29 bits [15:12].

9.4 Analog Bias Pins for Voltage Reference

- The **REF_REXT_A** pin (pin D4) on the VSC8564 device should connect to the system ground through a 2 kΩ resistor with a tolerance of 1.0% and minimum 1/16W. This pin is used to set up critical bias currents for the Ethernet physical device.
- The **REF_FILT_A** pin (pin D3) on the VSC8564 device should connect to the system ground through a 1 μF capacitor with 10% tolerance; NPO, X7R, or X5R ceramic materials are all acceptable.
- For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (rather than being connected individually to a common ground plane), as shown in [Figure 9-2](#). This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8564.
- Refer to [Figure 9-2](#) for the analog bias pins connection.

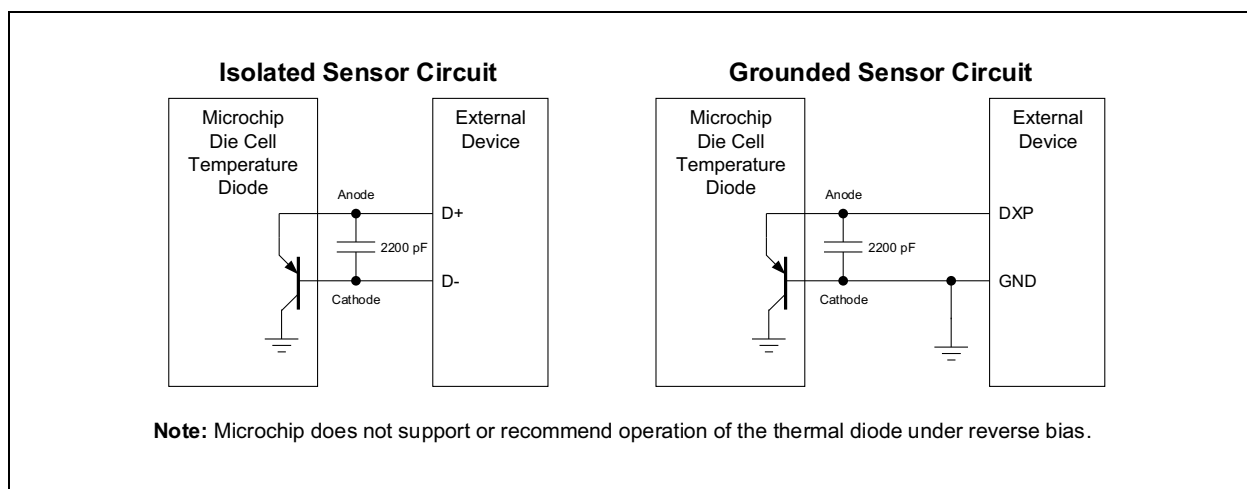
FIGURE 9-2: VOLTAGE REFERENCE SCHEMATIC



9.5 Temperature Sensor Diode

- The temperature sensor diode pins provide access to an on-die diode and internal circuitry for monitoring die temperature. To use it, connect an external thermal sensor located on the board or in a stand-alone measurement kit. The feature can be as an option in application.
- The **THERMDA** pin (pin C3) is the Thermal Diode Anode pin, which needs to be pulled down by a pull-down resistor if not used.
- The **THERMDC_VSS** pin (pin D2) is the Thermal Diode Cathode pin connected to system ground. The temperature sensor must be chosen accordingly. This pin needs to be pulled down by a pull-down resistor if not used.
- Temperature measurement using a thermal diode is very sensitive to noise. [Figure 9-3](#) illustrates a generic application design.

FIGURE 9-3: THERMAL DIODE CONNECTIONS



9.6 PHY Address Pins

- The VSC8564 device includes three external PHY address pins, **PHYADD [4:2]**, to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 3) and the setting of the PHY address reversal bit in register 20E1, bit 9. See [Table 9-4](#) for more information on the PHY address.

TABLE 9-4: PHY ADDRESS PIN DESCRIPTIONS

Pin Name	Pin Number	Type	Description
PHYADD1	F13	I, PU	Device SMI Address Bit 1. Normally tied to VSS unless an address offset of 0x2 is used by the system's station manager.
PHYADD2	G13	I, PD	PHYADD [4:2] for access each PHY's registers through SMI interface.
PHYADD3	G14	I, PD	
PHYADD4	F14	I, PD	

9.7 SPI Slave (Optional Use)

Use slave SPI I/O for MACsec register access.

Note: Highly recommended for MACsec applications.

TABLE 9-5: SPI SLAVE INTERFACE PINS

Pin Name	Pin Number	Type	Description
SPI_IO_CLK	H15	I/O, PU, 3V	Serial peripheral interface clock input from external device
SPI_IO_CS	J13	I/O, PU, 3V	Serial peripheral interface chip select
SPI_IO_DI	G15	I/O, PU, 3V	Serial peripheral interface data input
SPI_IO_DO	F15	I/O, PU, 3V	Serial peripheral interface data output

9.8 Other Pins

- The **COMA_MODE** (pin L3) provides an optional feature that may be used to control when the PHYs become active. The typical usage is to keep the PHYs from becoming active before they have been fully initialized. Alternatively, the **COMA_MODE** pin may be connected low (ground) by a pull-down resistor and the PHYs will be fully active once out of reset. Hence, this pin should be pulled down by a pull-down resistor. When this pin is asserted high, all PHYs are held in a powered down state. When deasserted low, all PHYs are powered up and resume normal operation.
- The **FASTLINK_FAIL** (pin K14) provides a Fast Link Failure indication signal. The register 17G bit [9] can enable this feature, and the register 19G bits [3:0] can select the source PHY for fast link failure indication. If this feature is not used, this pin **FASTLINK_FAIL/GPIO_9** can be floating.

9.9 Unused and No Connection Pins

- The **RESERVED_[1:14]** pins (pins C10, D13, L4, P4, L1, M1, N1, P1, J15, J16, N3, N4, L2, and E14) are reserved signals. Leave them unconnected (floating).
- The **NC_[1:4]** pins (pins A1, A16, T1, and T16) are unconnected pins. Leave them floating.

9.10 General External Pull-Up and Pull-Down Resistors

- If there is no pull-up resistor value specified, a 4.7 k Ω resistor is recommended to use.
- If there is no pull-down resistor value specified, a 1 k Ω or 4.7 k Ω resistor is recommended to use.

NOTES:

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if a single ground reference as a system ground is used for all ground pins. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.1, "Current Requirements"	Refer to Table 3-1 to ensure that the power pins are correct. Select the correct power supply components with at least about 25-30% margin based on Table 3-2 for the system power design.		
	Section 3.2, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"	Refer to Figure 3-1 to check the power circuit connection, decoupling capacitors, and filtering.		
	Section 3.4, "Bulk Decoupling Capacitors"	If doing PCB layout, see this section for the bulk decoupling capacitor required.		
Section 4.0, "Twisted Pair Media Interface"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify all analog I/O pins connection for quad-port circuit design based on product design requirement to select the design of Figure 4-1 or Figure 4-2 .		
	Section 4.2, "10/100/1000 Magnetics Connection and RJ45 Connection"	Verify the magnetics and the common-mode capacitors connection based on Figure 4-1 or Figure 4-2 .		
	Section 4.3, "PCB Layout Considerations"	Refer to this section for PCB layout design reference to check if the Gigabit copper port PCB layout request is met.		
Section 5.0, "SerDes Media Interface"	Section 5.1, "Fiber and Copper SFP Interface Pins and Descriptions"	Refer to Table 5-1 to make sure correct pins for SerDes Media interface are used in the design.		
	Section 5.2, "SerDes Media Interface Connecting to 1000BASE-X Fiber or 1000BASE-T Copper SFPs"	Refer to Figure 5-1 for SerDes media interface to connect to 1000BASE-X fiber SFPs design or to connect to 10/100/1000BASE-T copper SFPs design.		
	Section 5.3, "SerDes Media Interface Connecting to 100BASE-FX Fiber SFPs"	Refer to Figure 5-2 for SerDes media interface to connect to 100BASE-FX fiber SFPs design.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "QSGMII/SGMII/SerDes MAC Interface"	Section 6.1, "QSGMII/SGMII/SerDes MAC Pins and Connection"	Refer to Table 6-1 to make sure correct pins for QSGMII MAC interface are used in the design.		
	Section 6.2, "QSGMII MAC"	Refer to Figure 6-1 for QSGMII MAC interface to connect to four external QSGMII MACs in the design.		
	Section 6.3, "SGMII MAC"	Refer to Figure 6-2 for SGMII MAC interface to connect to four external SGMII MACs in the design.		
	Section 6.4, "SerDes MAC"	Refer to Figure 6-3 and Figure 6-4 for SerDes MAC interface to connect to four external SerDes MACs in the design or connect to 1000BASE-X SFPs or connect to 1000BASE-T SFPs in the design.		
	Section 6.5, "QSGMII/SGMII/SerDes MAC Design Rules"	Refer to this section for QSGMII/SGMII/SerDes MAC Interface PCB design.		
Section 7.0, "Device Clocks"	Section 7.1, "Reference Clock"	Refer to Table 7-1 to select the reference clock frequency and the correct reference clock pins in the design. Follow the layout required in PCB design.		
	Section 7.2, "Single-Ended REFCLK Input"	Refer to Figure 7-1 for single-ended reference input clock circuit design and use the correct resistor divider in the circuit based on Table 7-2 for correct resistors values.		
	Section 7.3, "Differential REFCLK Input"	Refer to Figure 7-2 for the differential reference input clock circuit design and use the correct capacitor AC coupling in the design.		
	Section 7.4, "Media Recovered Clock Output"	Refer to Figure 7-3 for a typical recovered clock circuit design and use the correct recovered clock pins and correct configuration.		
Section 8.0, "Digital Interface and I/O"	Section 8.1, "Serial Management Interface (SMI) Pins"	Refer to Table 8-1 and the descriptions in this section for SMI interface circuit design.		
	Section 8.2, "GPIO Pins"	Refer to Table 8-2 and the descriptions in this section for all GPIO pins in the circuit design.		
	Section 8.3, "JTAG Pins"	Refer to Table 8-3 and the descriptions in this section for all JTAG pins in the circuit design.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 9.0, "Miscellaneous"	Section 9.1, "Reset"	Refer to Table 9-1 to use the correct reset pin and see if the designed reset circuit to meet the reset time requirement.		
	Section 9.2, "Reference Resistor"	Refer to Table 9-2 to select the correct SerDes biasing pins in the design. Make sure to connect a $620\Omega \pm 1\%$ resistor between the <code>REXDES_REXT_0</code> and <code>REXDES_REXT_1</code> pins. See Figure 9-1 for the design reference.		
	Section 9.3, "LED Pins"	Check if correct LED pins are used based on Table 9-3 , current limit resistors, and LED power.		
	Section 9.4, "Analog Bias Pins for Voltage Reference"	Check if the correct pull-down resistor value is used for <code>REF_REX-T_A</code> pin and the correct pull-down capacitor value is used for <code>REF_FILT_A</code> pin based on Figure 9-2 .		
	Section 9.5, "Temperature Sensor Diode"	If designing with the temperature sensor diode, see Figure 9-3 as the design reference.		
	Section 9.6, "PHY Address Pins"	Check if the correct PHY address pins are used based on Table 9-4 to configure the correct PHY address the design requires.		
	Section 9.7, "SPI Slave (Optional Use)"	Highly recommended for MACsec applications with more than two slaves on the MDIO bus. Allows MaCsec register access.		
	Section 9.8, "Other Pins"	For <code>COMA_MODE</code> and <code>FASTLINK_FAIL</code> pins, check this section for the correct design.		
	Section 9.9, "Unused and No Connection Pins"	Verify all reserved pins and NC pins are unconnected.		
	Section 9.10, "General External Pull-Up and Pull-Down Resistors"	Generally, it is recommended to use 4.7 k Ω pull-up resistor and 1 k Ω pull-down resistor.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005010A (05-12-23)	Initial release	

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at <https://www.microchip.com/en-us/support/design-help/client-support-services>.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, KoD, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2023, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-2464-6

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta

Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX

Tel: 512-257-3370

Boston

Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago

Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Novi, MI
Tel: 248-848-4000

Houston, TX

Tel: 281-894-5983

Indianapolis

Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles

Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC

Tel: 919-844-7510

New York, NY

Tel: 631-435-6000

San Jose, CA

Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto

Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820