Opamp_PIC32MK Model Usage Guidelines

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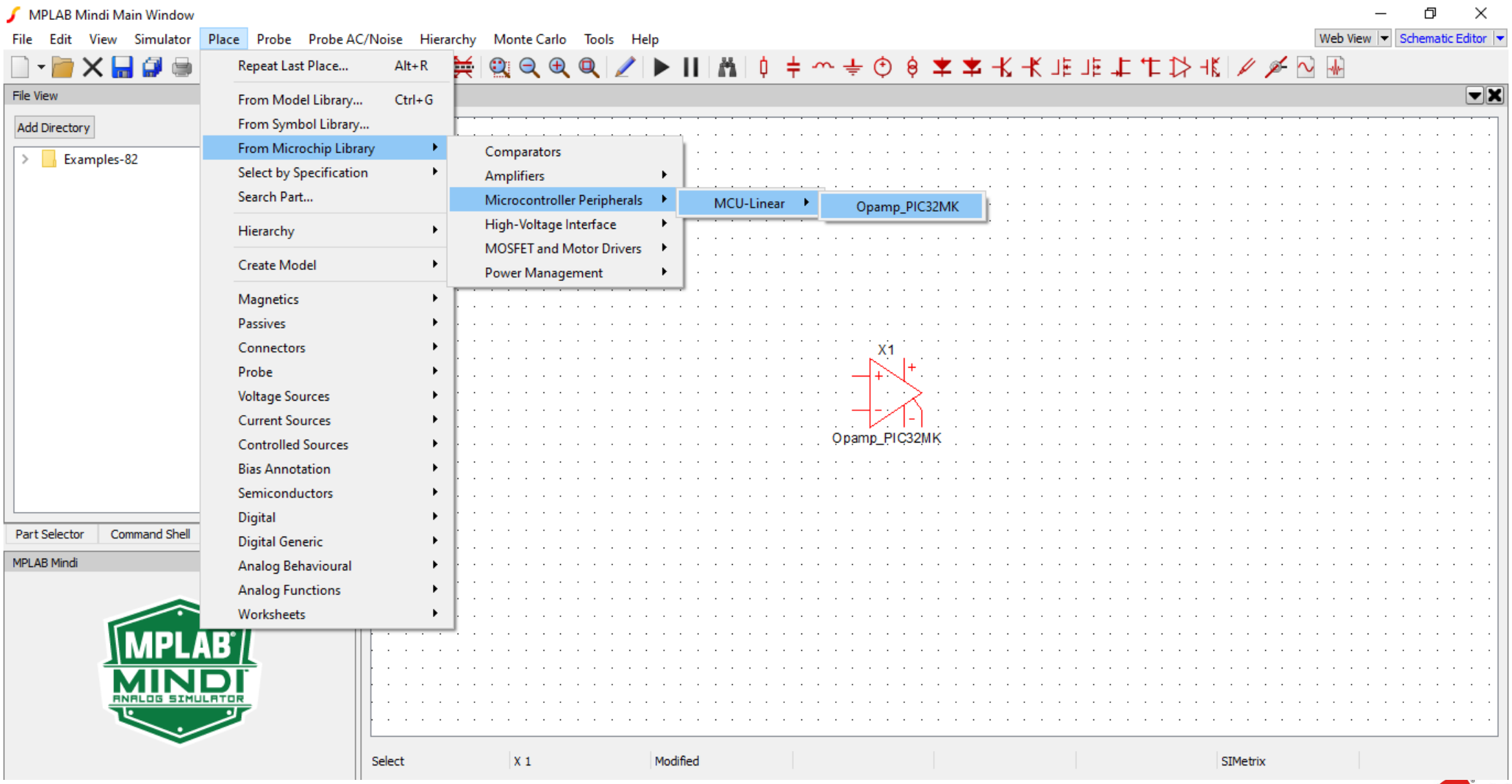
DS70005431A

General Info

- **Model Name: Opamp_PIC32MK**
- **Modelled to mimic the 100MHz Opamp from the PIC32MK class of devices. This is used in MCU32 90nm projects.**
- **Matching of model with the device is done at the worst case corner.**
- **Objective: Get an estimate on the Opamp performance, and understand the PCB effect.**

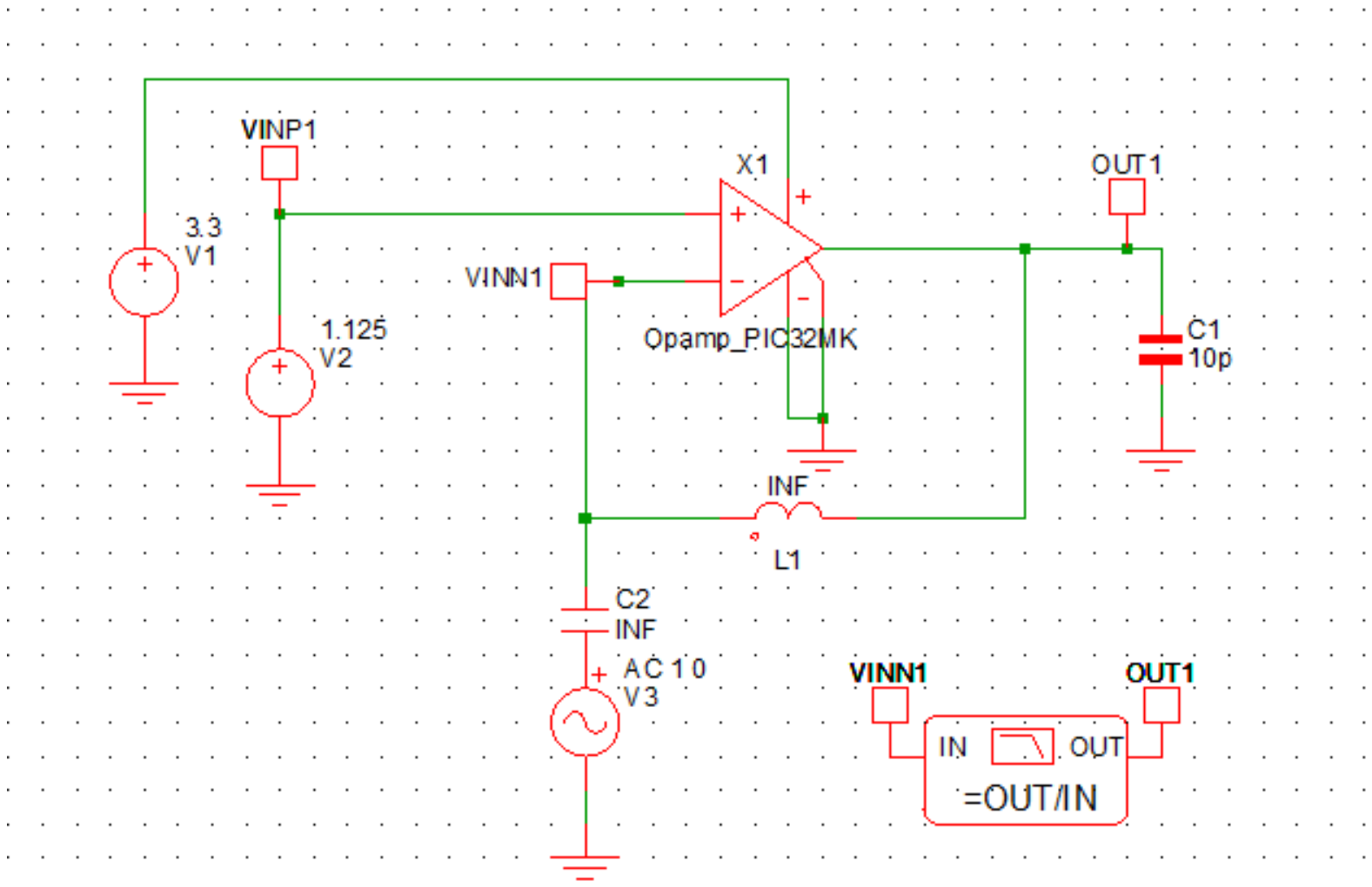
Finding the model in Mindi



Example Schematics

AC, Transient Analysis

Stability – Open Loop Response - Schematic



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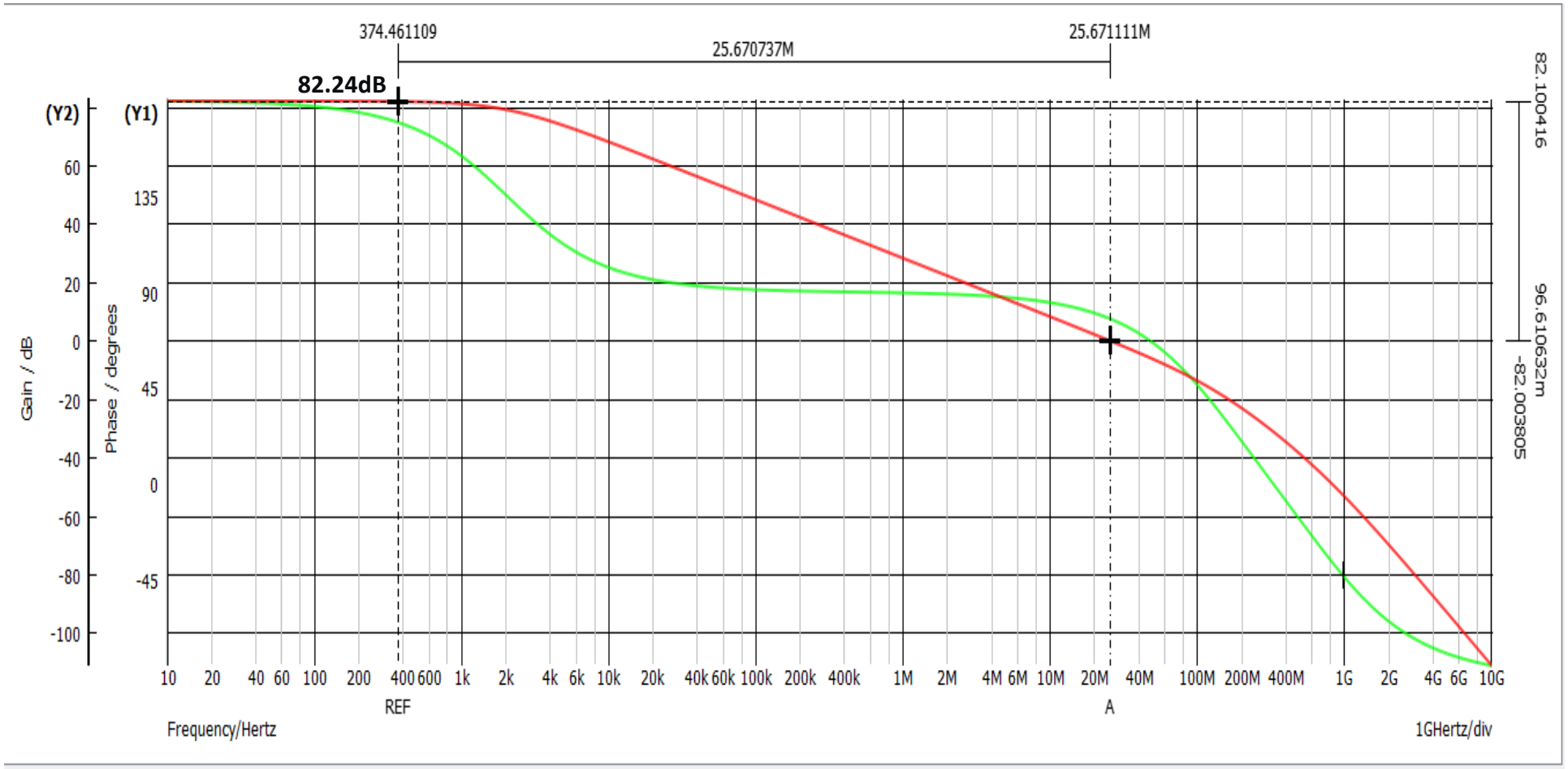
Stability – Open Loop Response – Simulation Plot



Curve label	Name	Value
Gain (Y2)	Gain Crossover Frequency	25.94306MegHz
Gain (Y2)	Gain Margin	30.881942dB
Phase (Y1)	Phase Margin	77.221836degrees

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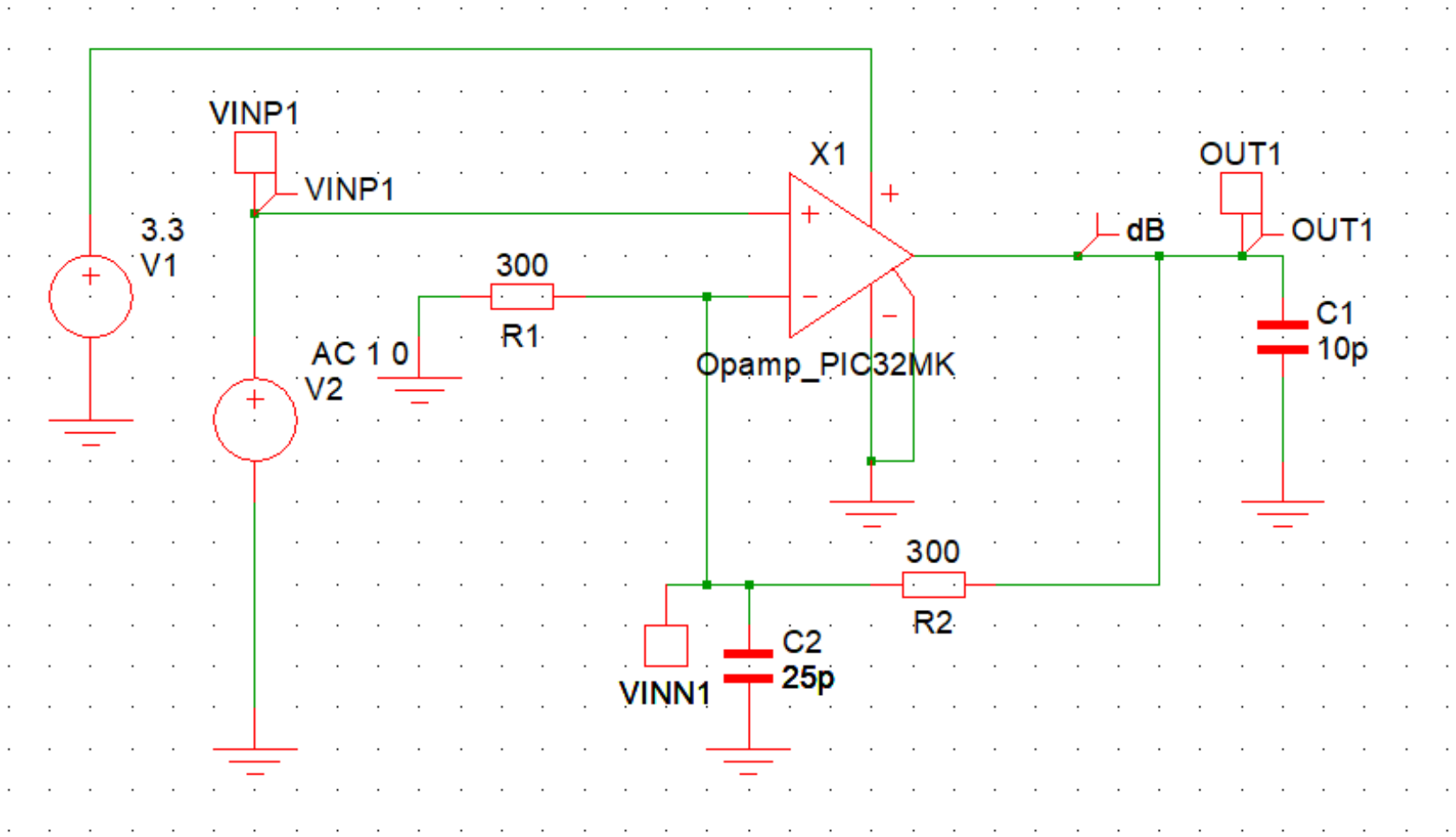
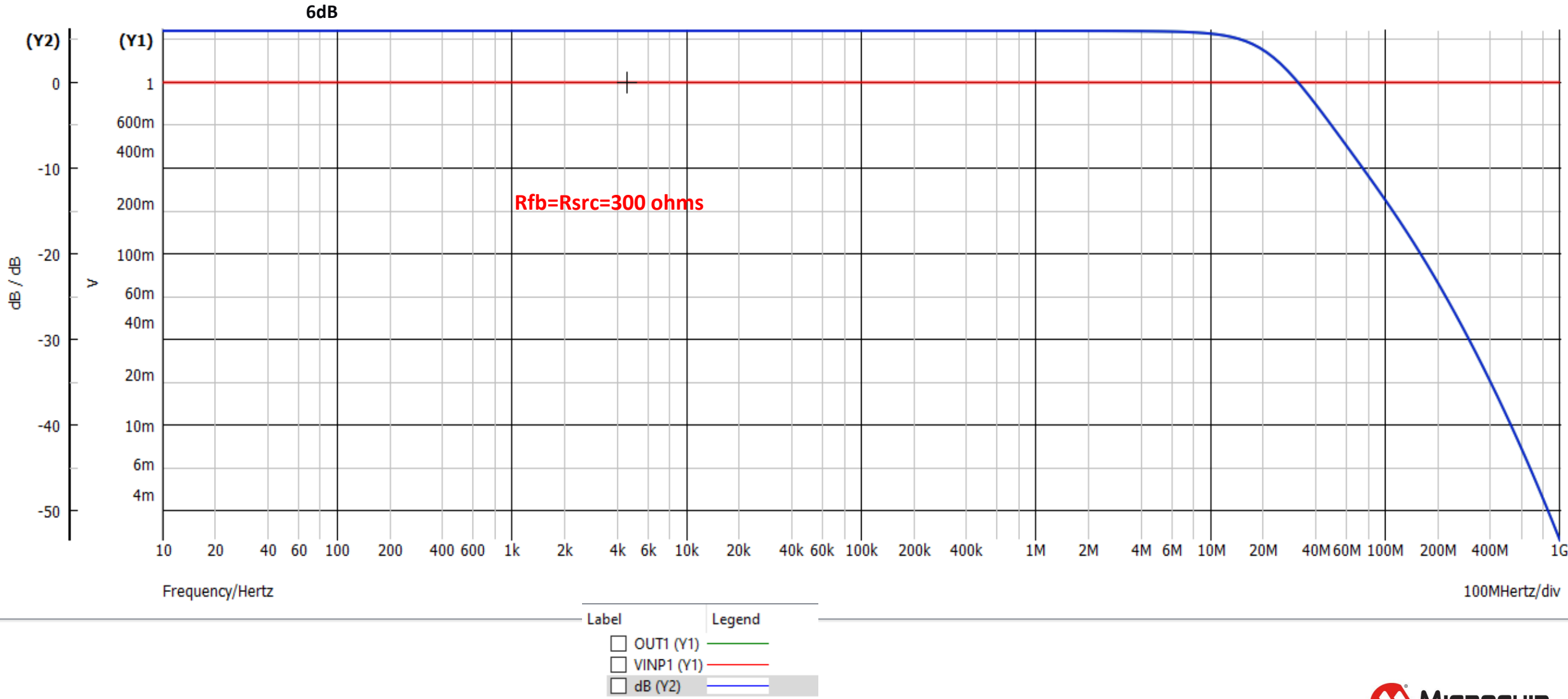
AC – Closed Loop Response - Schematic



Including 25pF input parasitic capacitance

AC – Closed Loop Response – Simulation Plot



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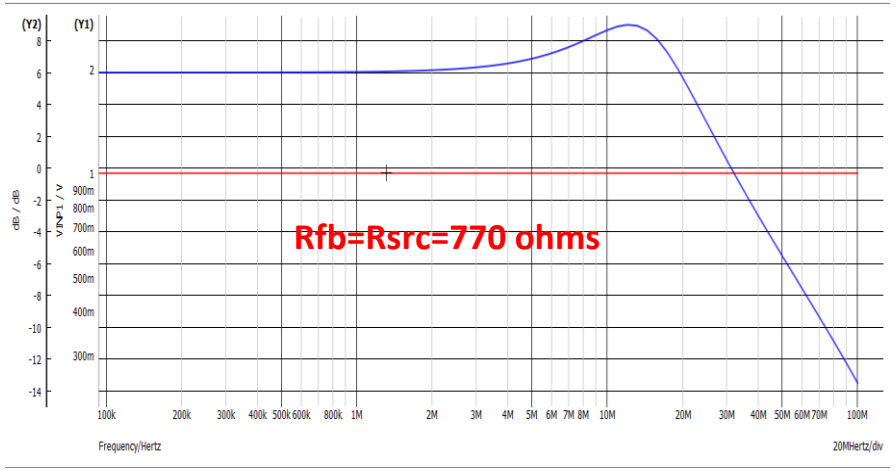
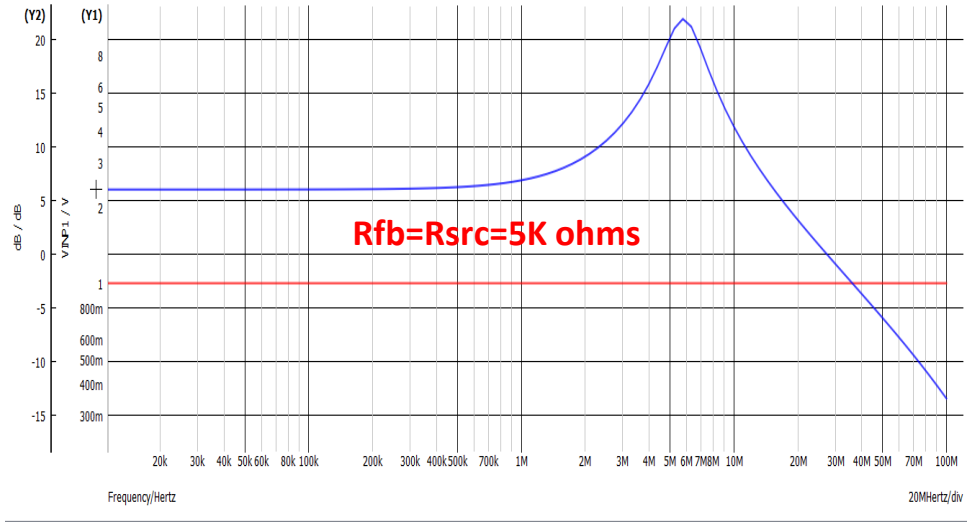
AC – Closed Loop Response- Component selection

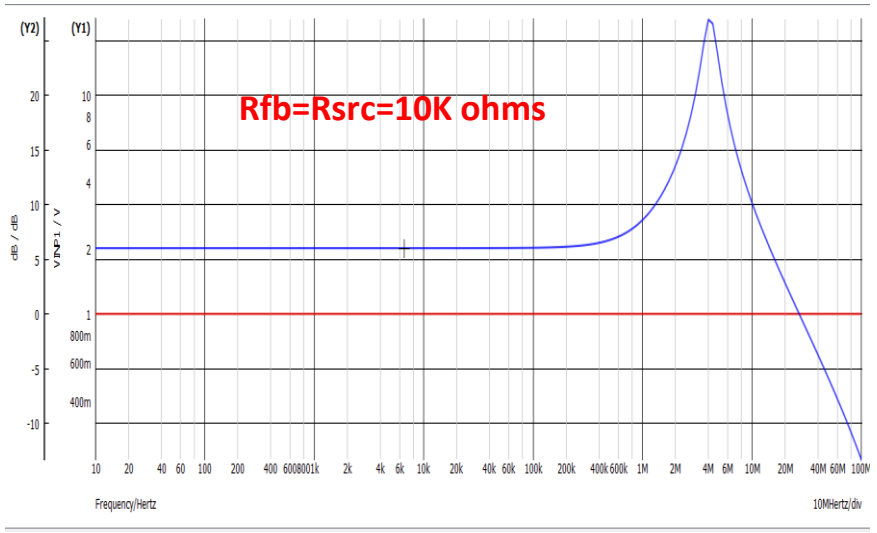
- **The below table shows the Vout peaking for different resistor values, for Acl=2 and Cin=25pF.**

Parameter				
Rfb, Rsrc (ohms)	300	770	5k	10k
Output				
Closed Loop Gain @ 10Hz (dB)	6.019	6.019	6.019	6.019
Vout peaking (dB)	-	2.91	15.72	20.88

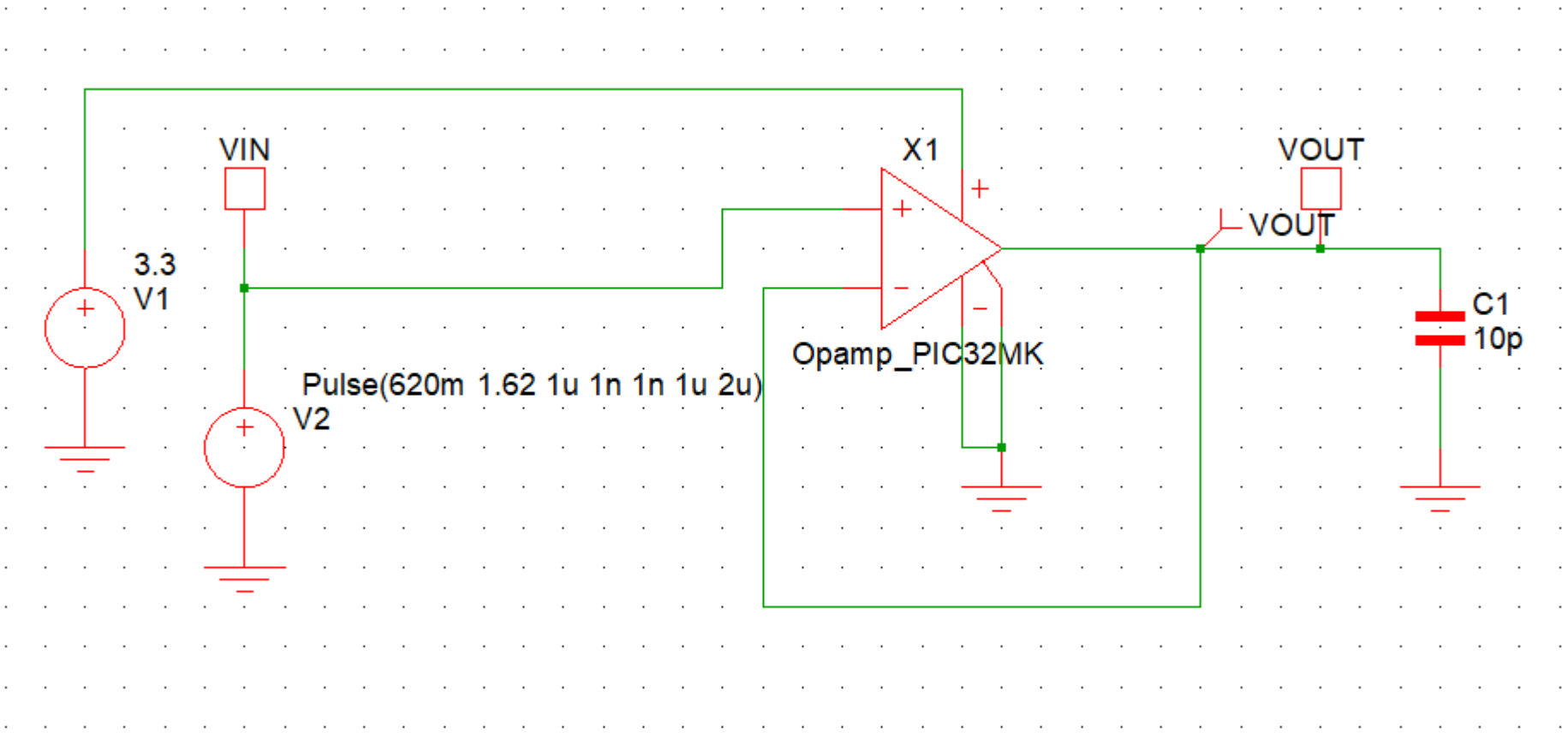
We get around 3dB peaking at Rsrc=Rfb=770 Ohms







Transient Analysis – Slew Rate - Schematic



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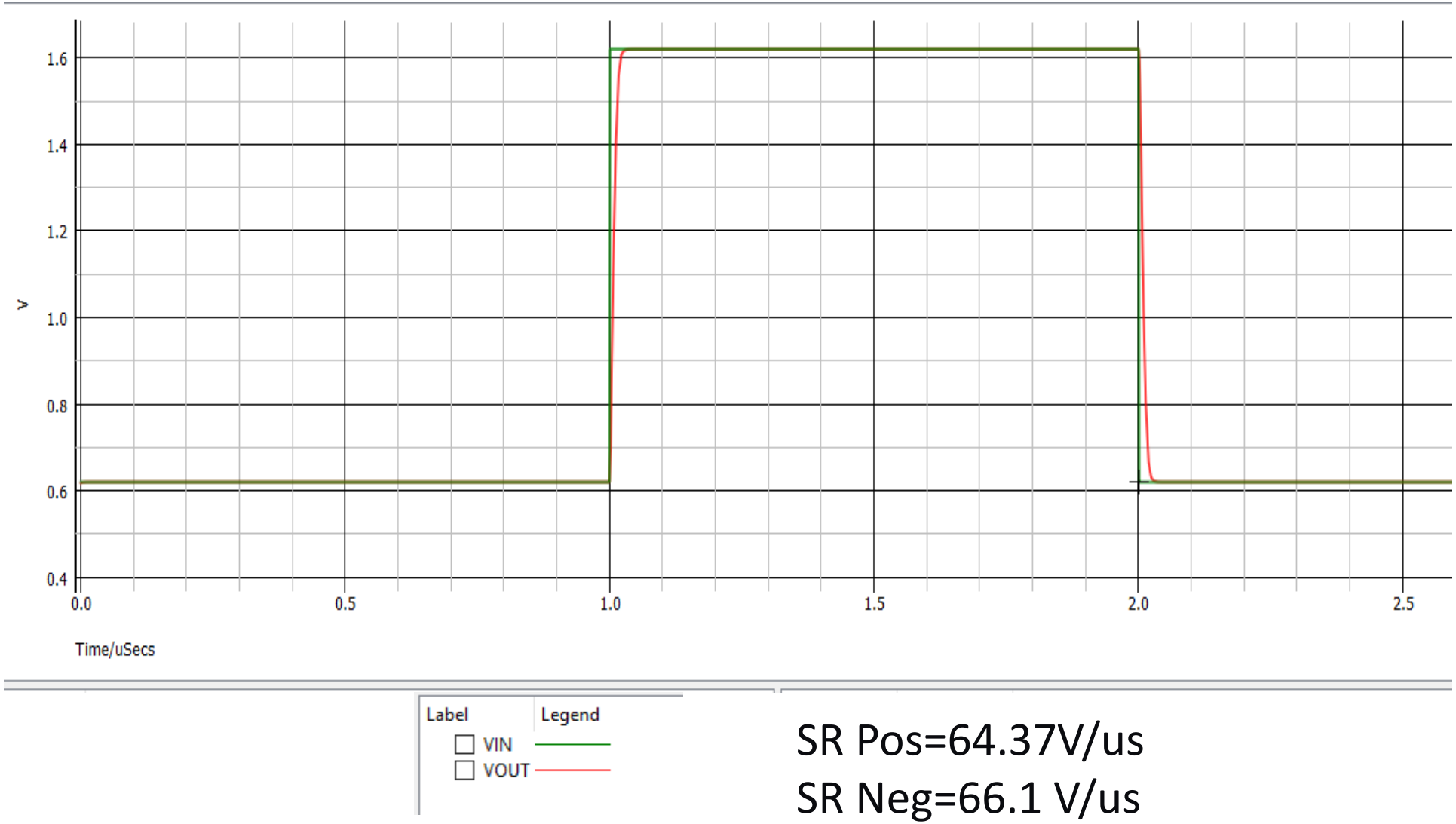
Transient Analysis – Slew Rate – Simulation Plot



SR Pos=64.37V/us

SR Neg=66.1 V/us

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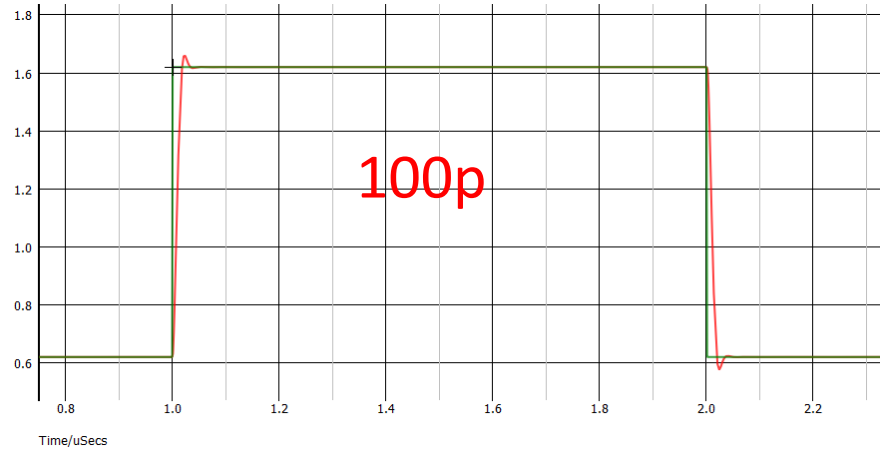
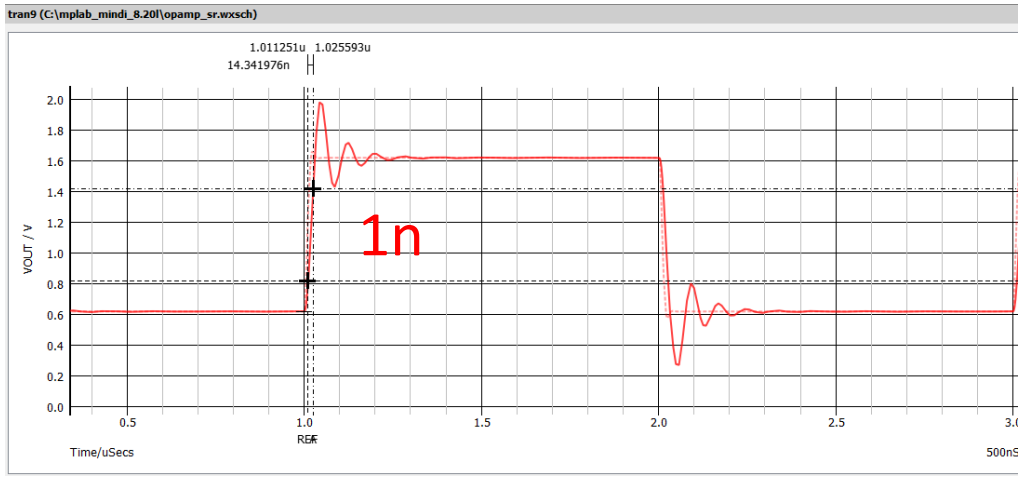
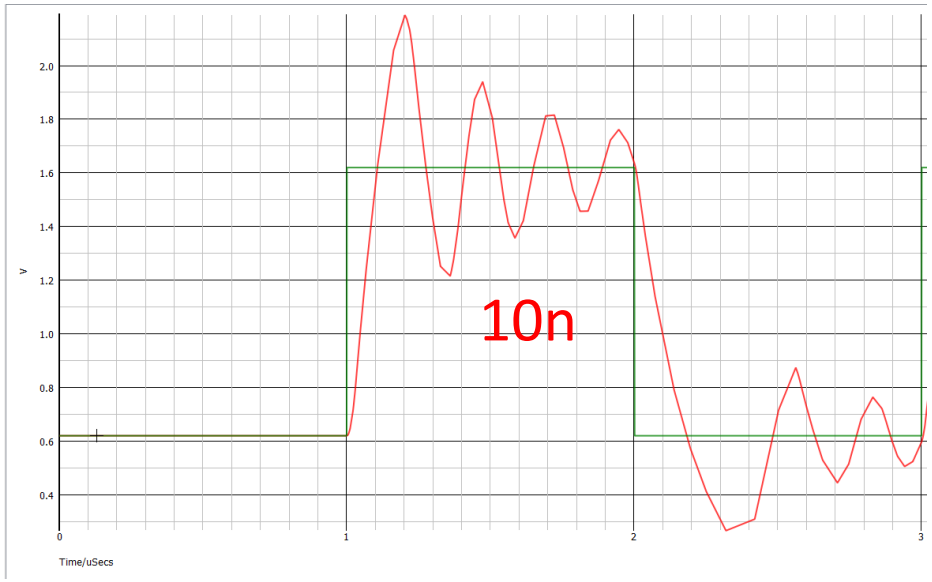
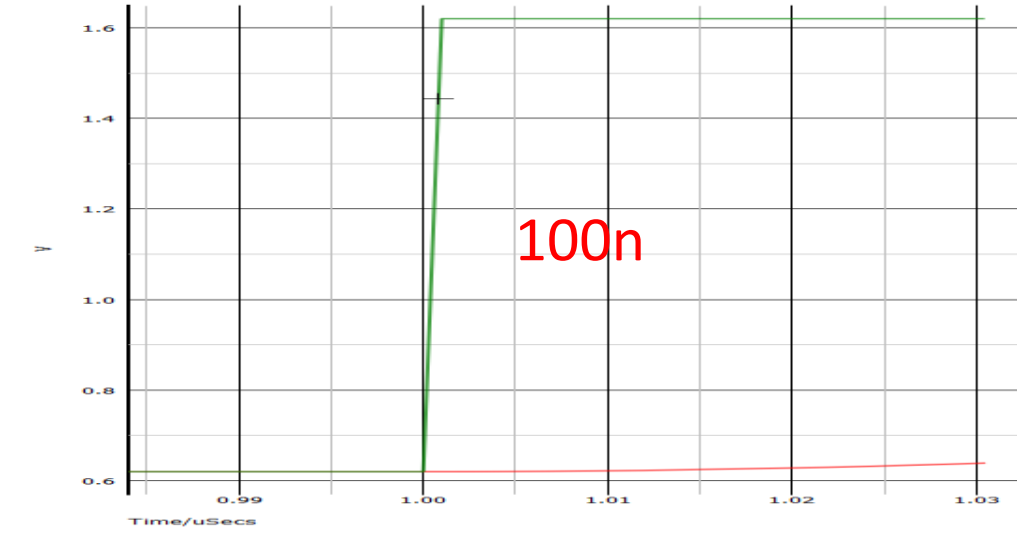
Transient Analysis – Slew Rate - Component selection

- **The plots for different load caps are shown below:**



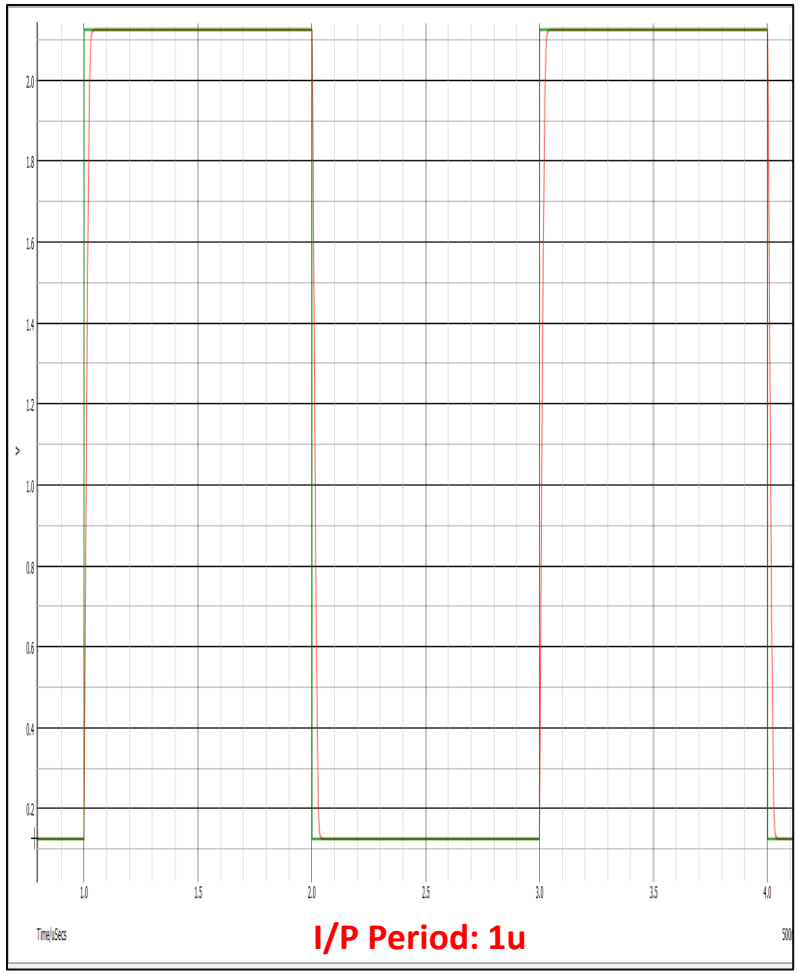




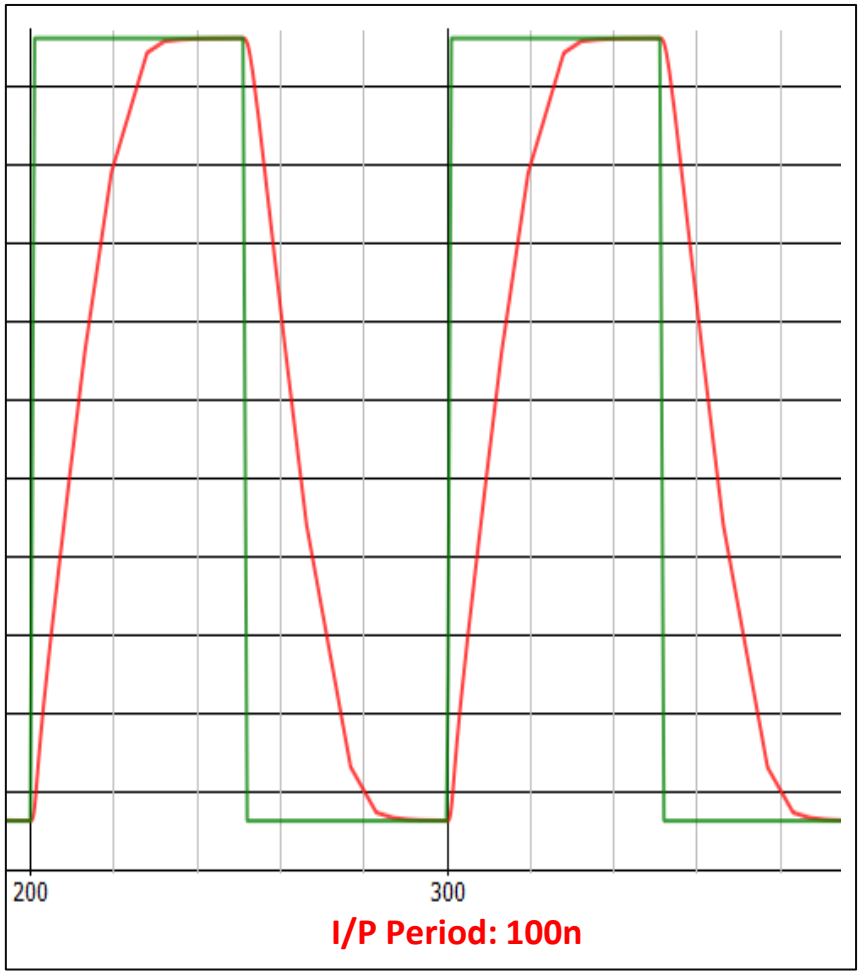


Model output doesn't converge for Cload of 100n

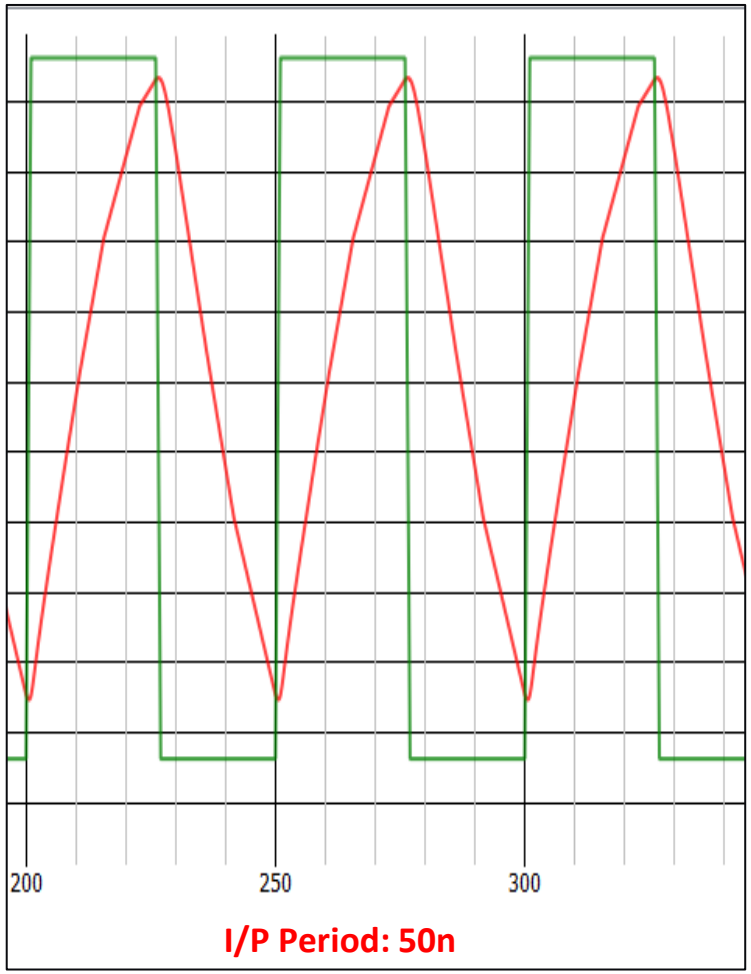
Transient Analysis – Slew Rate – Simulation Plot - Different I/P Period



I/P Period: 1u



I/P Period: 100n



I/P Period: 50n

VIN
VOUT

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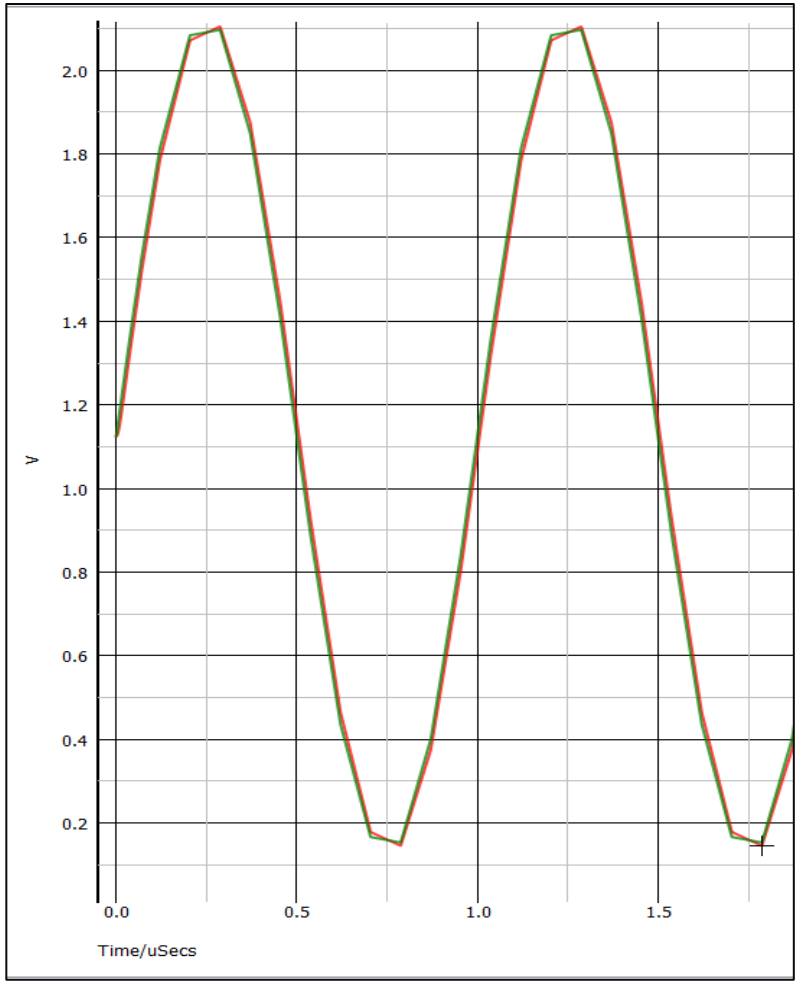
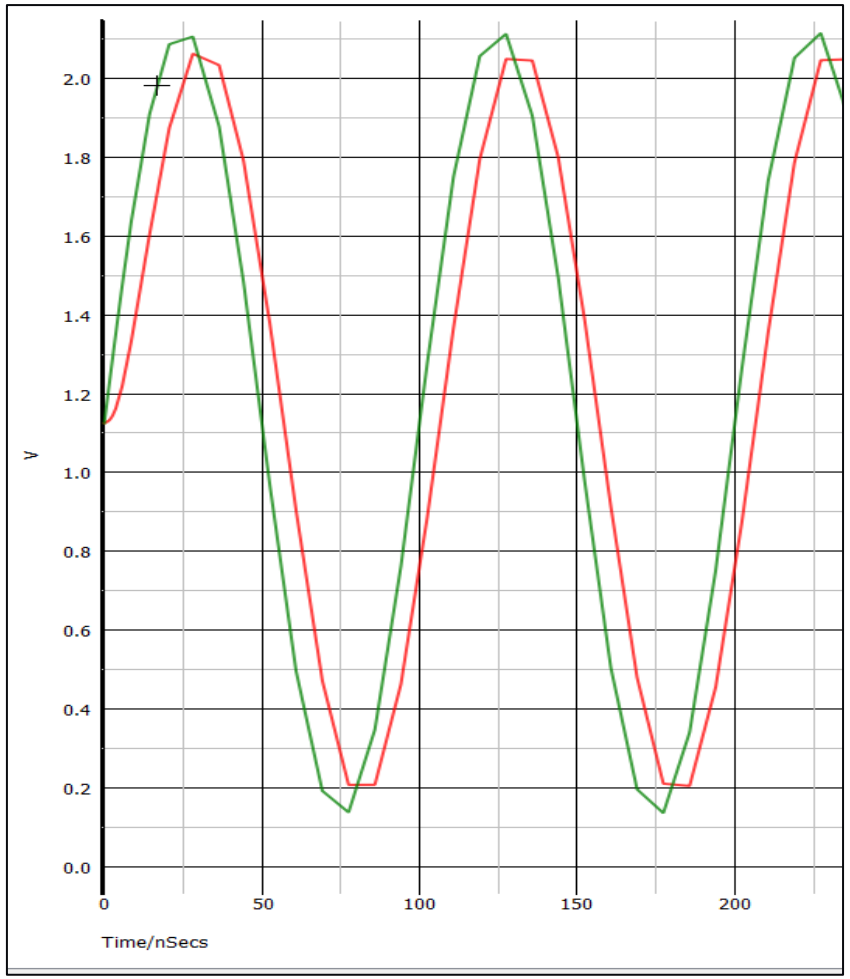
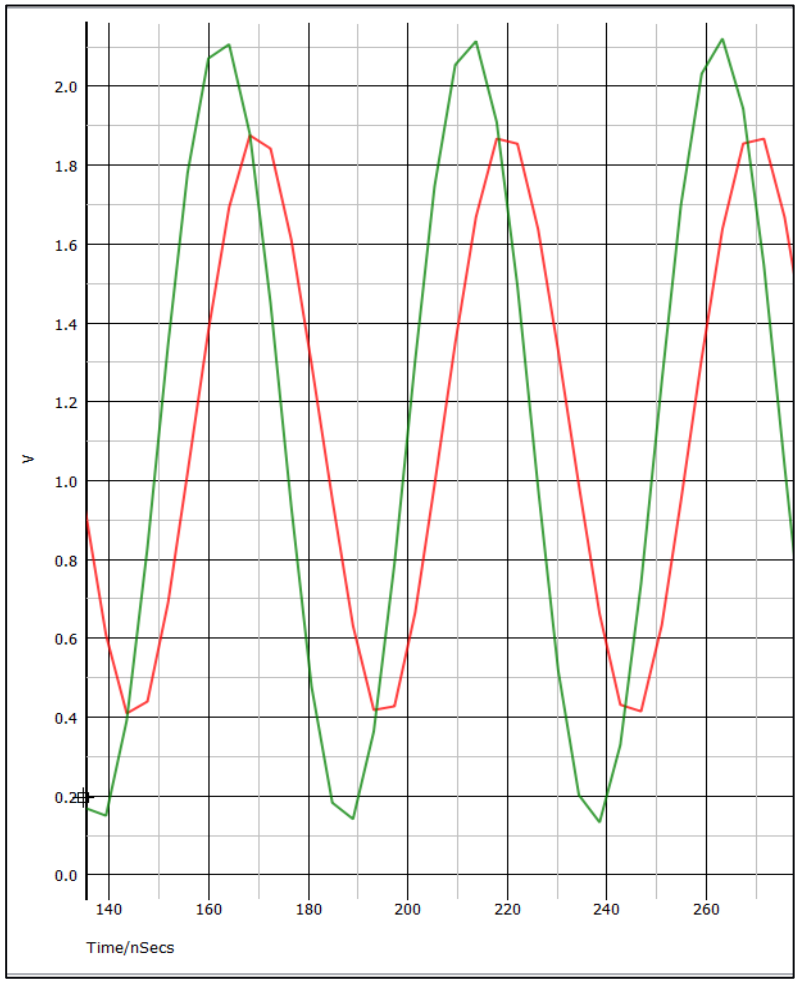
Transient Analysis – Slew Rate – Simulation Plot - Different I/P Period



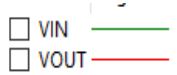
I/P Period: 1u



I/P Period: 100n



I/P Period: 50n



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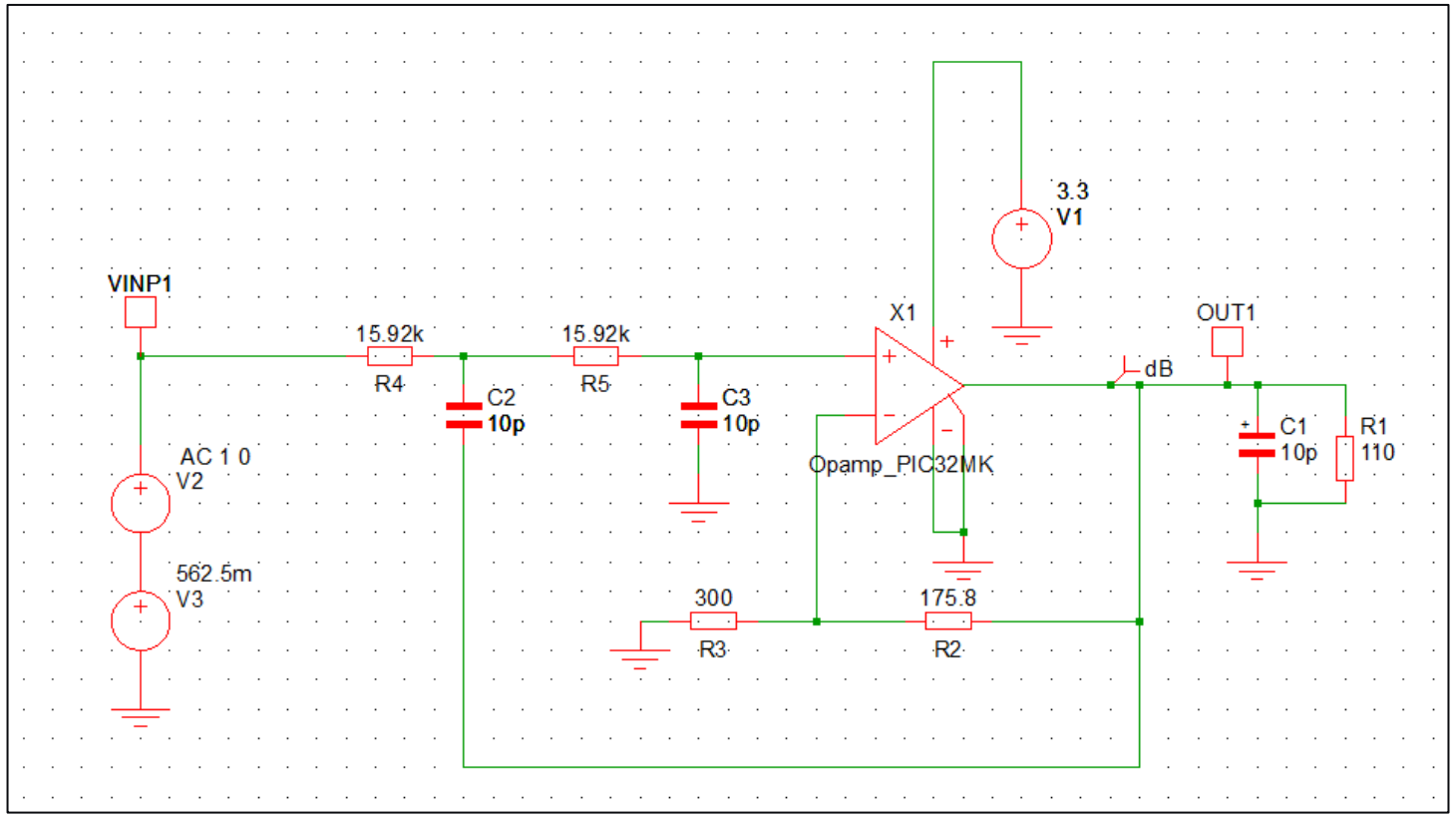
Transient Analysis – Slew Rate – Different Iload

- **The slew rate for different load current is tabulated below:**

Parameter								
Iload	Min	Max	500u	1m	2m	10m	20m	50m
Output								
SR Pos (V/us)	37.54	64.09	64.09	63.54	61.99	54.57	49.64	37.54
SR Neg (V/us)	39.31	65.79	65.79	65.49	64.51	56.27	49.66	39.31

Application Schematics

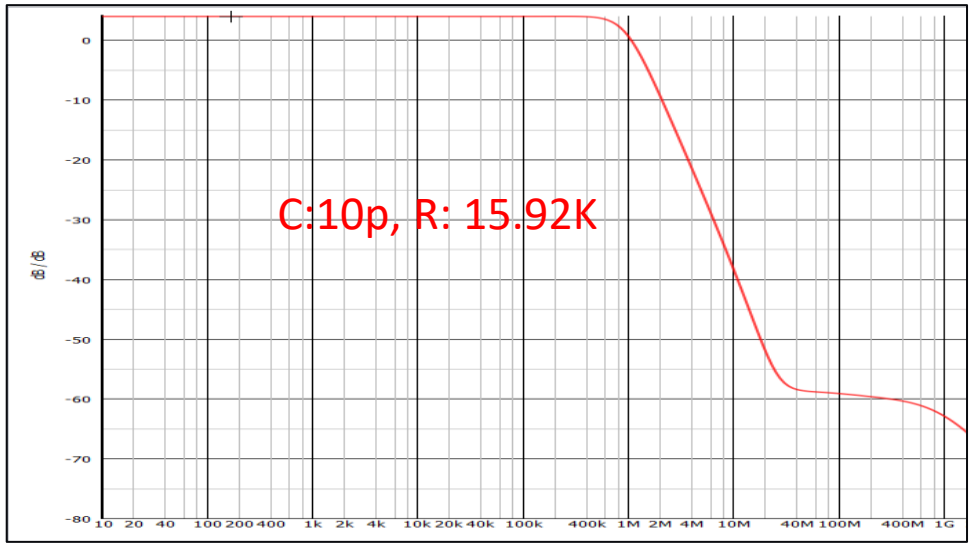
2nd order LP BWF - Schematic

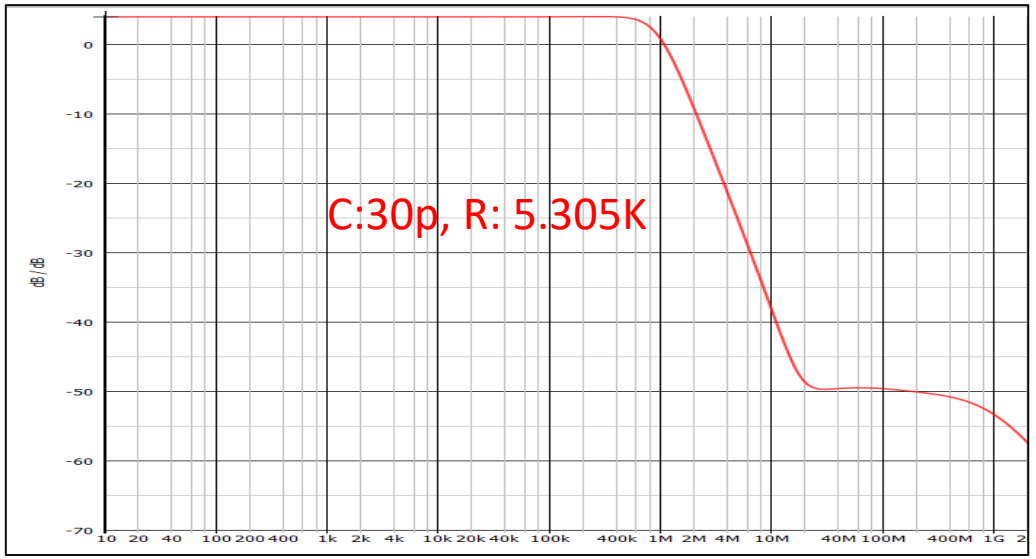


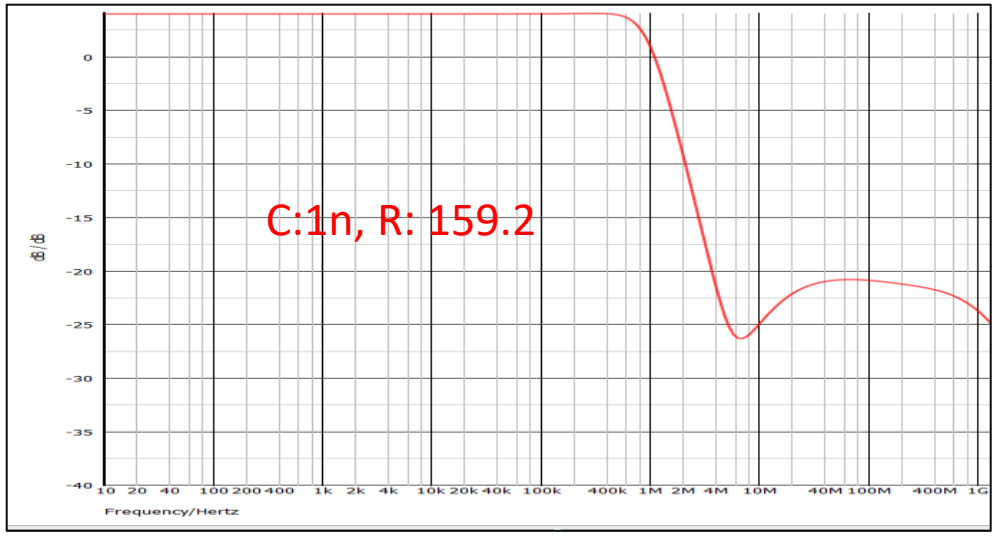
f=1/(2*pi*RC)

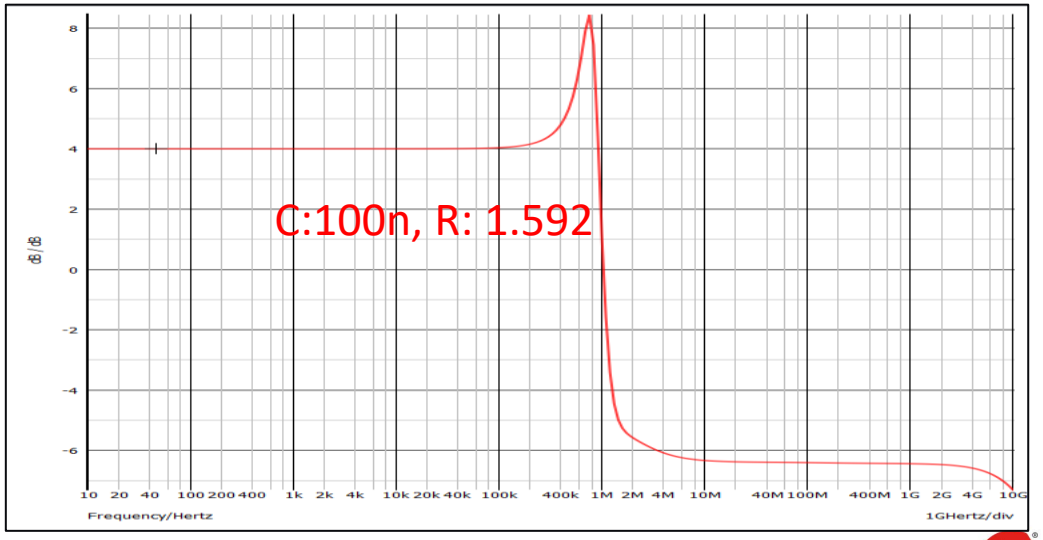
Parameter				
C (F)	10p	30p	1n	100n
R (Ohms)	15.92k	5.305k	159.2	1.592
Output				
Closed Loop Gain @ 10Hz (dB)	4.0102	4.0102	4.0102	4.0102
Vout 3dB BW (Hz)	964.92k	982.14k	994.32k	1.0052M

2nd order LPBWF – Simulation Plot - Different RC values (f:1MHz)









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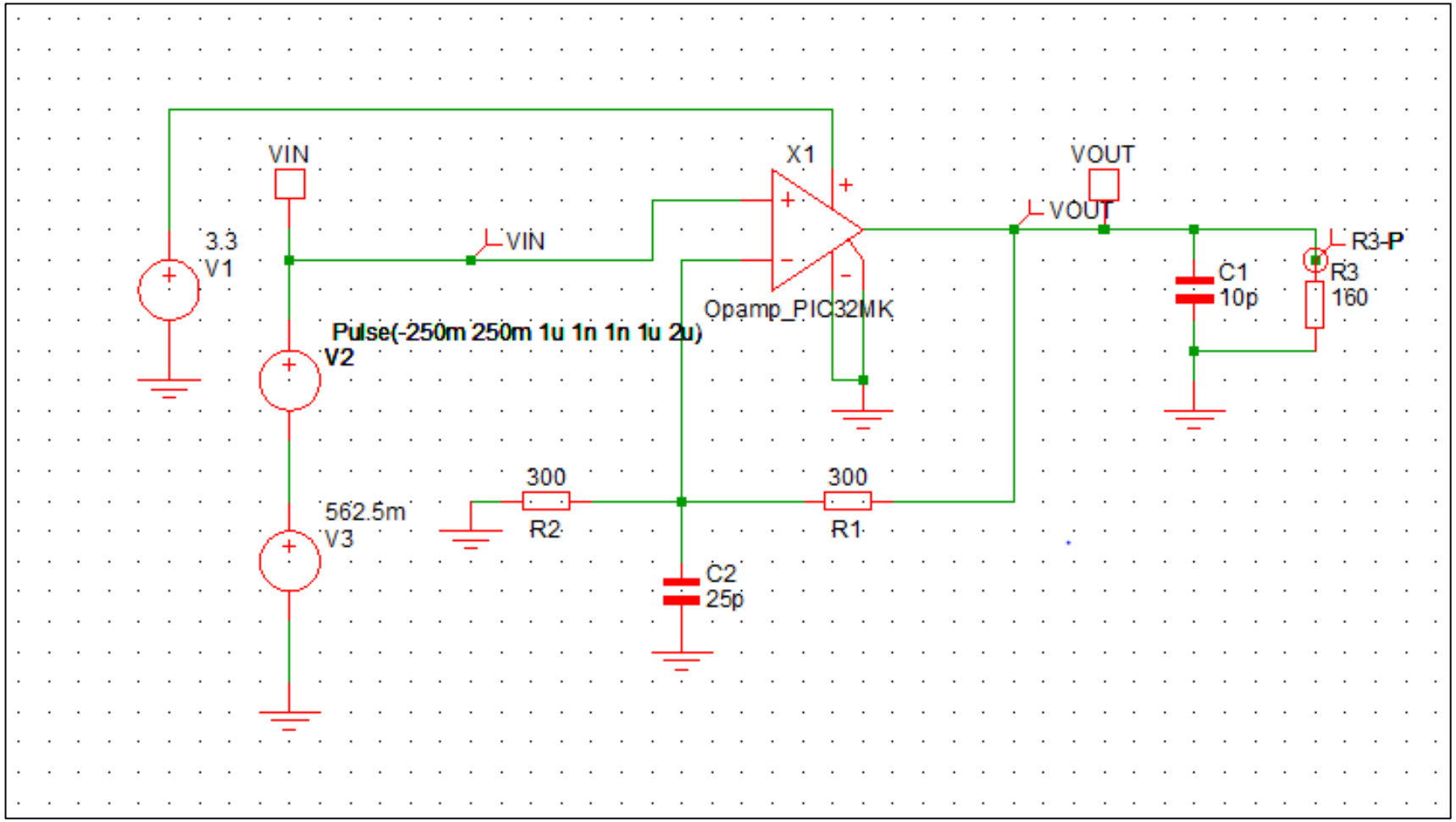
Non-Inverting Amplifier - Schematic



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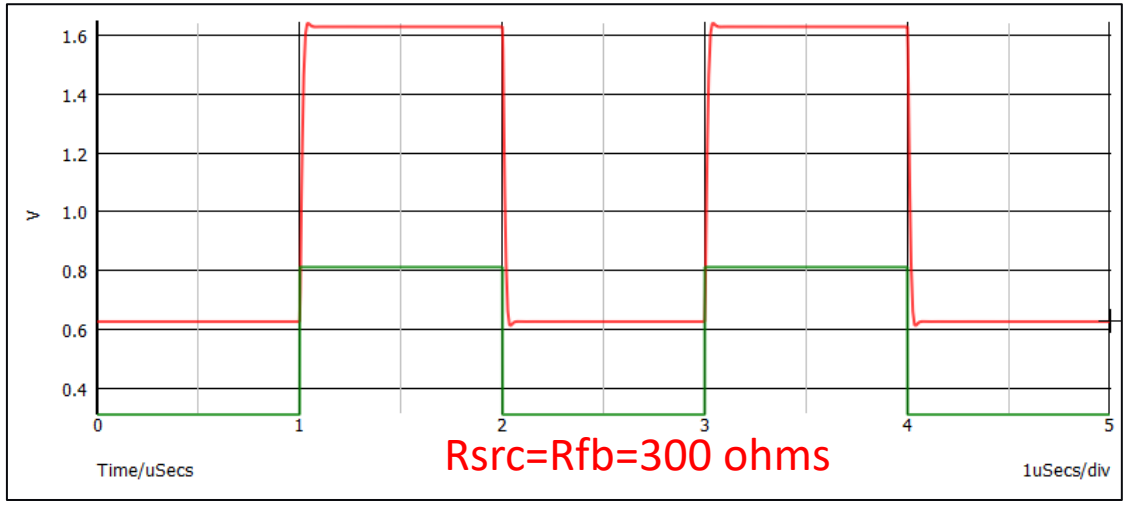
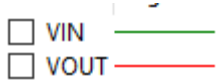
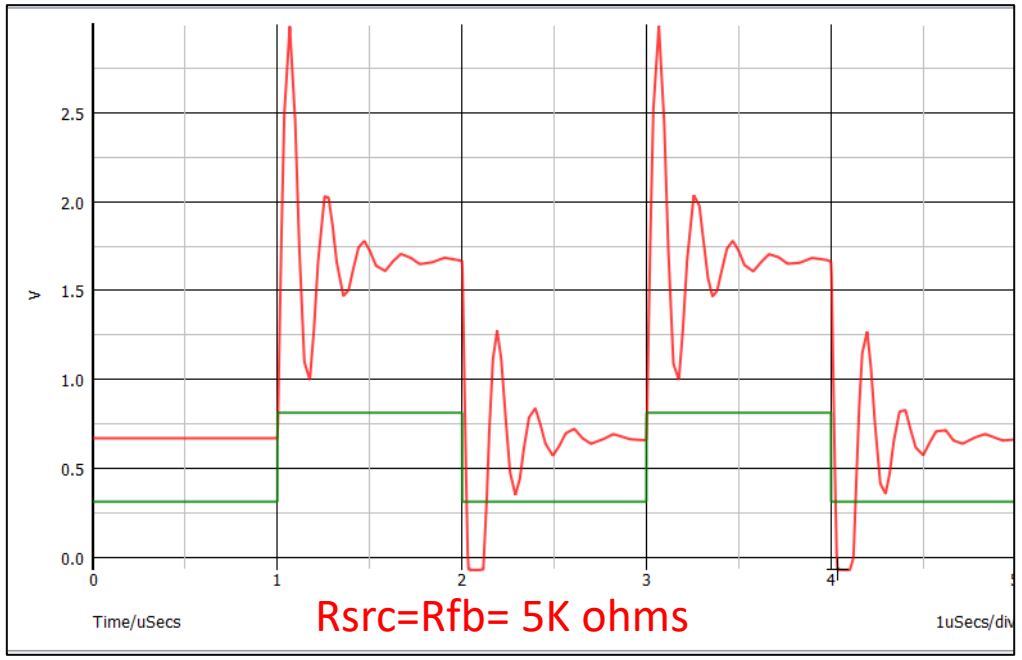
Non-Inverting amplifier - Simulation Plot - Different R values (Acl=2)

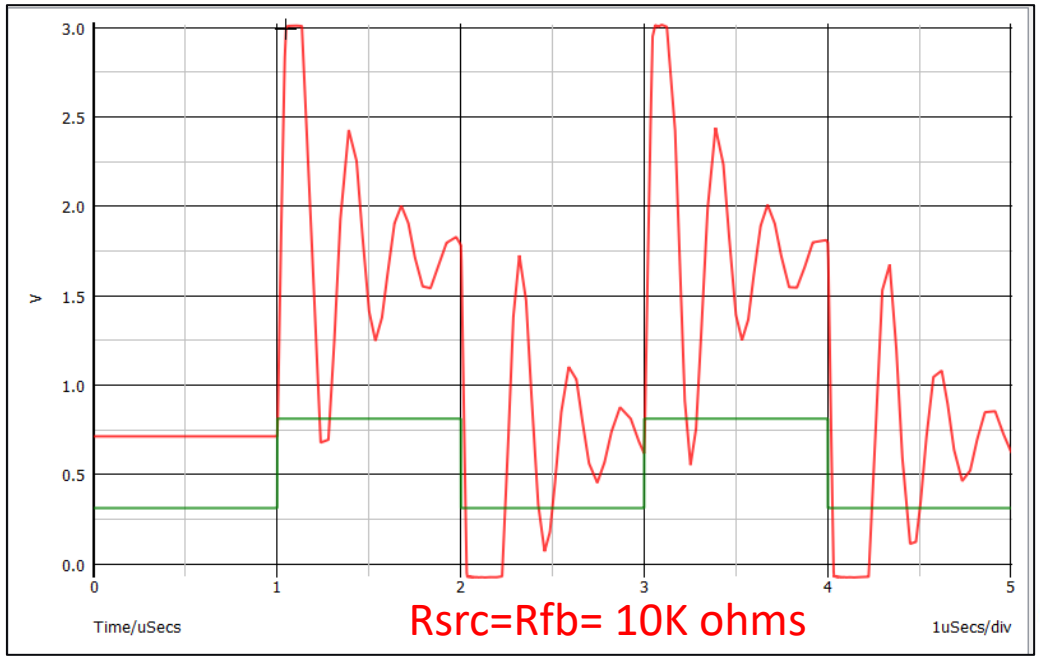


Rsrc=Rfb=300 ohms





Rsrc=Rfb= 5K ohms



Rsrc=Rfb= 10K ohms

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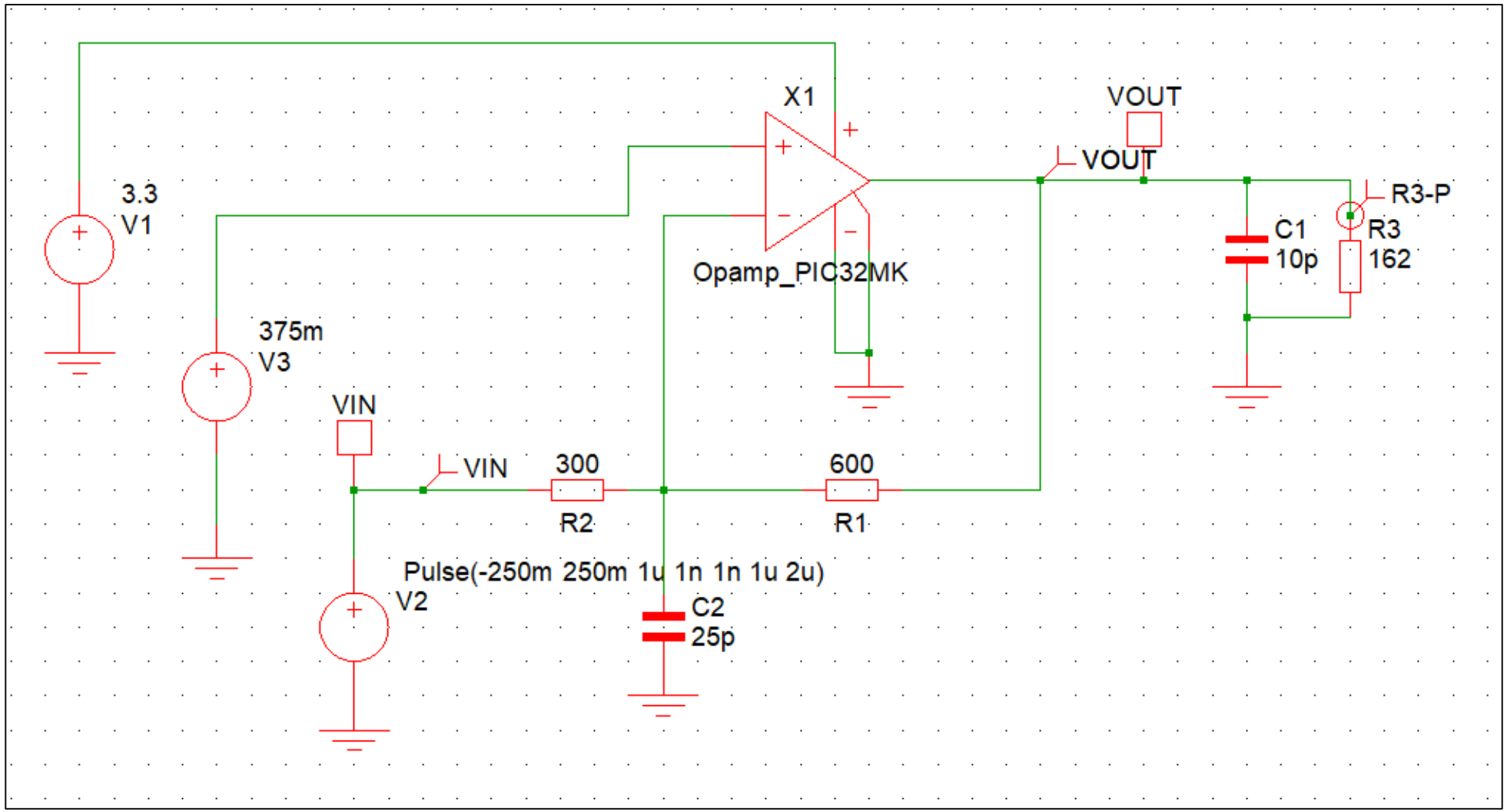
Inverting Amplifier - Schematic



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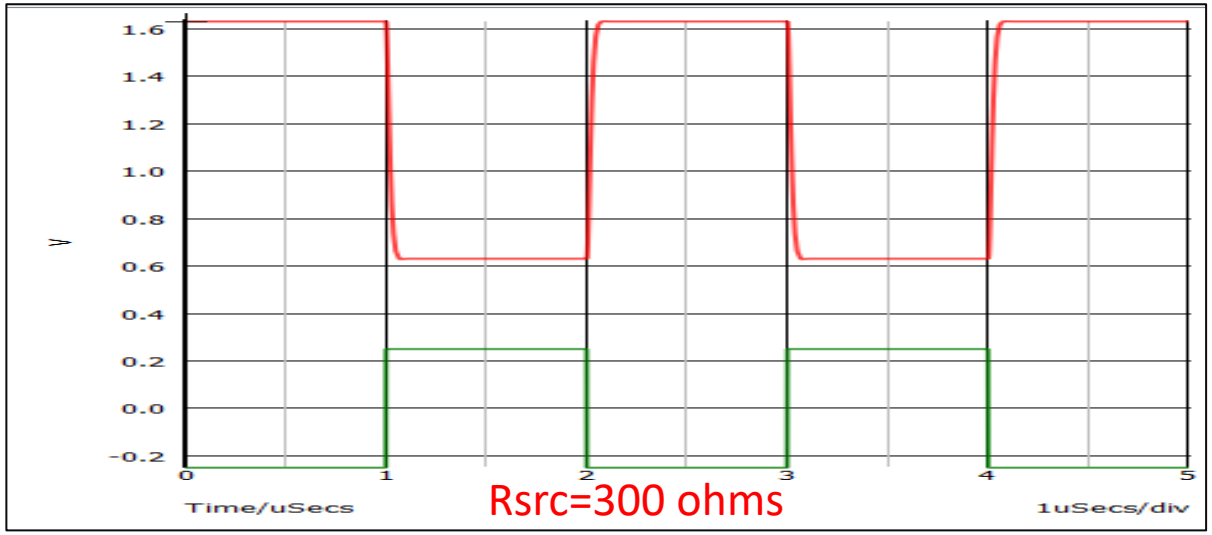
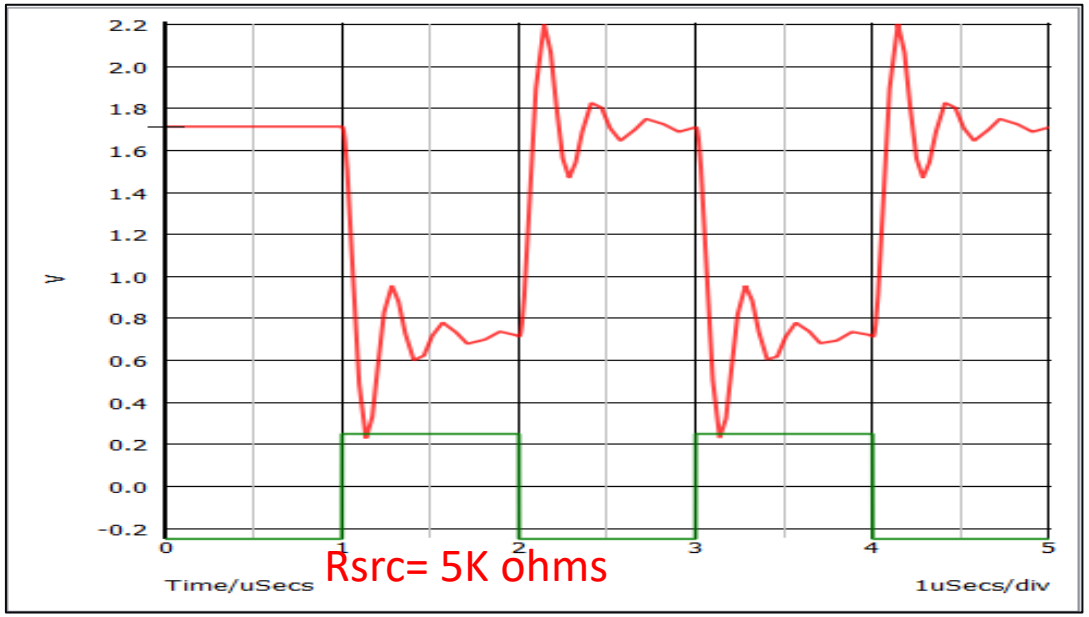
Inverting amplifier - Simulation Plot - Different R values (Acl=2)



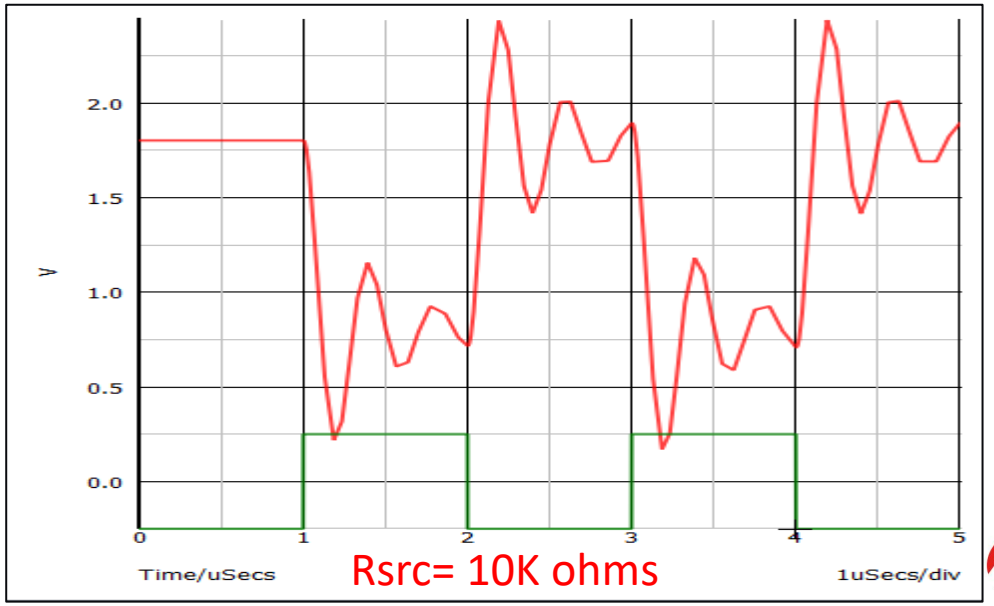
Rsrc=300 ohms

VIN
VOUT

Rfb=2*Rsrc



Rsrc= 5K ohms



Rsrc= 10K ohms

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Limitations

- The model is ideal and not affected by PVT variations.
- The model is preliminary and doesn’t include common mode input range, output impedance, noise parameters etc.
- Doesn’t support noise model.
- CMRR and PSRR not modelled at higher frequencies.
- Performance not guaranteed outside the specified limits(Large Cload, Iload etc)