PolarFire FPGA Transceiver Decision Feedback Equalization

AN4950

Introduction (Ask a Question)

The PolarFire® Field Programmable Gate Array (FPGA) family includes multiple embedded low power and performance-optimized transceivers. Each transceiver has both Physical Medium Attachment (PMA), Protocol Physical Coding Sub-layer (PCS) logic interfaces to the FPGA fabric.

The transceiver has a multi-lane architecture with each lane natively supporting serial data transmission rates ranging from 250 Mbps to 12.7 Gbps.

At the receiver front end, Continuous Time Linear Equalization (CTLE) with optional auto calibration compensates the high-frequency losses to improve the received signal integrity. However, for lossy channels, the CTLE technique amplifies the high-frequency noise along with the data. This is resolved by using Decision Feedback Equalization (DFE), which mitigates lane noise caused due to Inter Symbol Interference (ISI) or crosstalk without amplifying the high-frequency noise within the data.

CTLE technique is sufficient to interpret data up to 8 Gbps for short reach applications. Beyond this, Decision Feedback Equalizer is capable of equalizing channel response. For more information on CTLE, DFE, and Transceiver insertion loss, see PolarFire FPGA and PolarFire SoC FPGA Transceiver User Guide.

An optionally enabled 5-tap DFE is available to equalize the lane response in conjunction with the CTLE.

The DFE-based operation uses current bit information to cancel ISI for the next bit through a feedback mechanism, allowing the next bits to be correctly sampled. Using taps to delay and by multiplying the symbols, the DFE effectively cancels out interference on the analog signal. The operation is nonlinear, allowing it to overcome the notch response that the CTLE does not perform. The DFE also includes an automatic calibration that finds the best possible tuning to match the transceiver lane to the system channel. DFE mode supports serial data transmission rates ranging from 3 Gbps to 12.7 Gbps.

Incremental DFE is another option of calibration to incrementally improve the performance of the DFE path.

Two independent algorithms, Data Eye Clock Centering Re-calibration and DFE Coefficient Re-calibration, offer incremental methods to improve DFE path performance after an initial calibration. These algorithms help in improving Data Eye for the most gradients, which occur from temperature and voltage and reduces the calibration time significantly. You can select the incremental DFE option in configurator, allowing them to trigger inputs for this calibration.

This application note demonstrates the simple procedure to perform run time DFE calibration using a Dynamic Reconfiguration Interface (DRI). It also shows how to plot eye diagrams using the SmartDebug tool and verify signal integrity in DFE mode. DFE equalization enables PolarFire transceivers to be efficient for systems running at approximately 10 Gbps or above where channel complexity is higher.

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1. DFE Calibration (Ask a Question)

DFE Calibration is carried out by a robust descent algorithm, which is optimized to avoid local minima, achieve predictable results, enable low area, and operate at high clock speeds. It adjusts the feedback coefficients (H1 - H5) by trial-and-error in response to the eye-area.

The algorithm operates on one dimension (a single coefficient) at a time. It takes a step of size 1 in the positive and then in the negative direction that is H1+1 and H1-1. If the area improves on either step, it continues to take another step in the same direction. If both directions yield a lower area, it continues to the next coefficient with the same step-size. After failing to improve the area on all coefficients, it increases the step-size and continues. If the area is improved the step-size immediately reduces to 1.

These demo designs are programmed using either of the following options:

- Using the `.job` file: To program the device using the `.job` file provided with the design files, see 7. Appendix 1: Programming the Device Using FlashPro Express.
- Using Libero® SoC: To program the device using Libero SoC, see Table 5-2.

2. Design Requirements (Ask a Question)

The following table lists the resources required to run the demo.

Table 2-1. Design Requirements

Requirement	Version
Operating System	64-bit Windows® 10
Hardware	
PolarFire® Evaluation Kit (MPF300-EVAL-KIT)	Rev D or later
2 SMA-to-SMA cables with 10 Gbps support (not provided with the kit)	—
Host PC	—
Utility Software	
FlashPro Express	**Note:** Refer to the `readme.txt` file provided in the design files for the software versions used with this design.
Libero® SoC Design Suite	

Important: Libero SmartDesign and configuration screenshots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

3. Prerequisites (Ask a Question)

Before you start the demo, ensure that the following components are in place:

1. For demo design files download link: www.microchip.com/en-us/application-notes/AN4950.
2. Download and install Libero SoC (as indicated on the website for this design) on the host PC from Libero SoC v12.0 and later.

The latest versions of ModelSim® and Synplify Pro® are included in the Libero SoC installation package.

4. Demo Design (Ask a Question)

The following sequence describes the data flow in the demo design and ensure that the transceiver CDR is locked:

1. The design uses a transceiver interface (PF_XCVR) configured in native PMA mode running at 10.3125 Gbps data-rate, 40-bit PCS fabric interface, and using 125 MHz reference clock.
2. The PRBS_Generator module generates a PRBS-7 pattern and forwards the data to the Transceiver Tx end.
3. The differential serial data of Tx and Rx is looped back using the onboard SMA-to-SMA cables.
4. This data is then received by the PRBS_checker module, which checks for data match. If matched the Lock is asserted, otherwise, an error signal is generated.

The following sequence describes how DFE calibration is triggered:

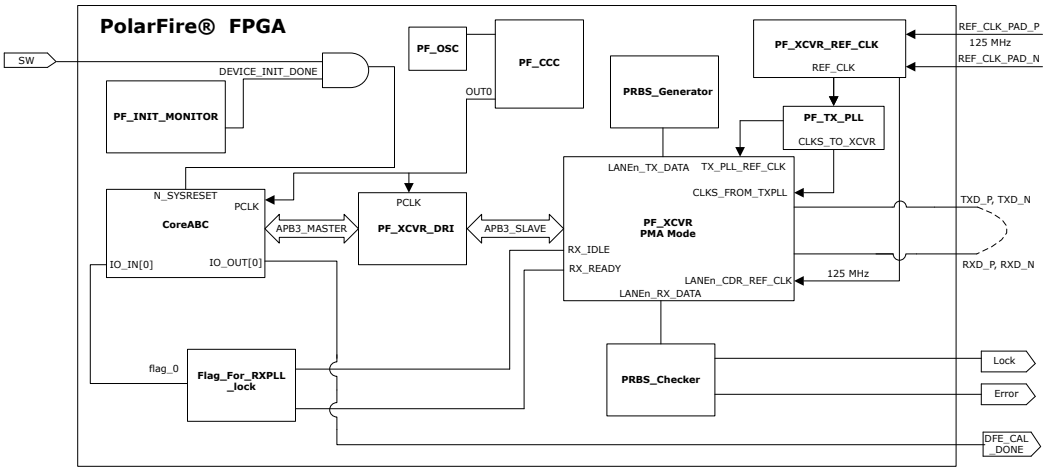
1. When the CDR is locked, valid RX_IDLE and RX_READY signals are sent to the Flag_for_RXPLL_lock_0 module.

> **Important:** RX_IDLE is low during data transmission and RX_READY is asserted when CDR is locked to the incoming serial data.

2. The Flag_for_RXPLL_lock_0 module determines proper transceiver RX PLL lock using the condition NOT RX_IDLE and RX_READY.
3. When the preceding condition is true, Flag_0 is asserted and sent to the CoreABC module.
4. This initiates the DFE calibration sequence using the CoreABC interface.
5. CoreABC acts as APB3 master and dynamically performs Read/Write to transceiver registers using the PF_XCVR_DRI interface. The transceiver interface is connected as APB3 slave to the PF_XCVR_DRI interface.
6. When the DFE calibration sequence is successful, the DFE_CAL_DONE flag is asserted.

The following figure shows the block diagram of the design.

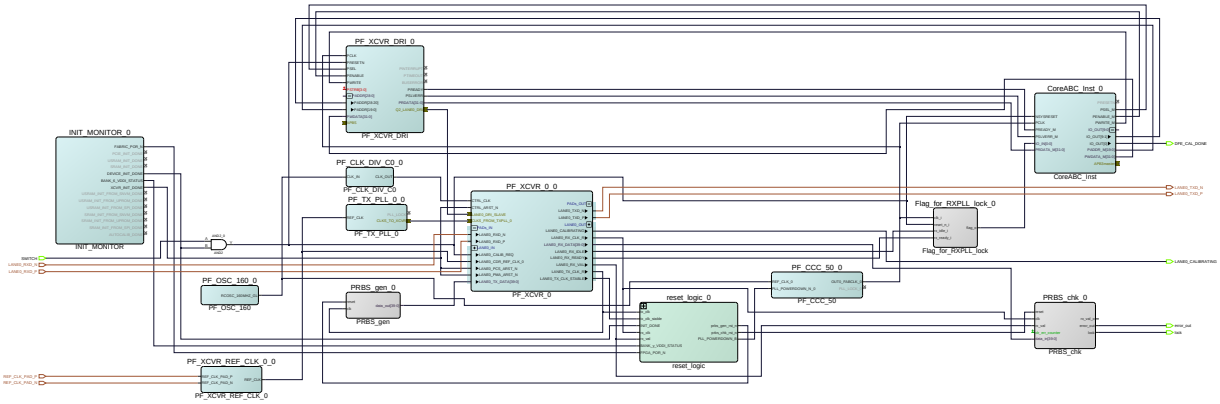
Figure 4-1. DFE Block Diagram



4.1 Design Implementation (Ask a Question)

The following figure shows the top-level Libero design of the PolarFire Transceiver DFE design.

Figure 4-2. Top Level Libero® Design



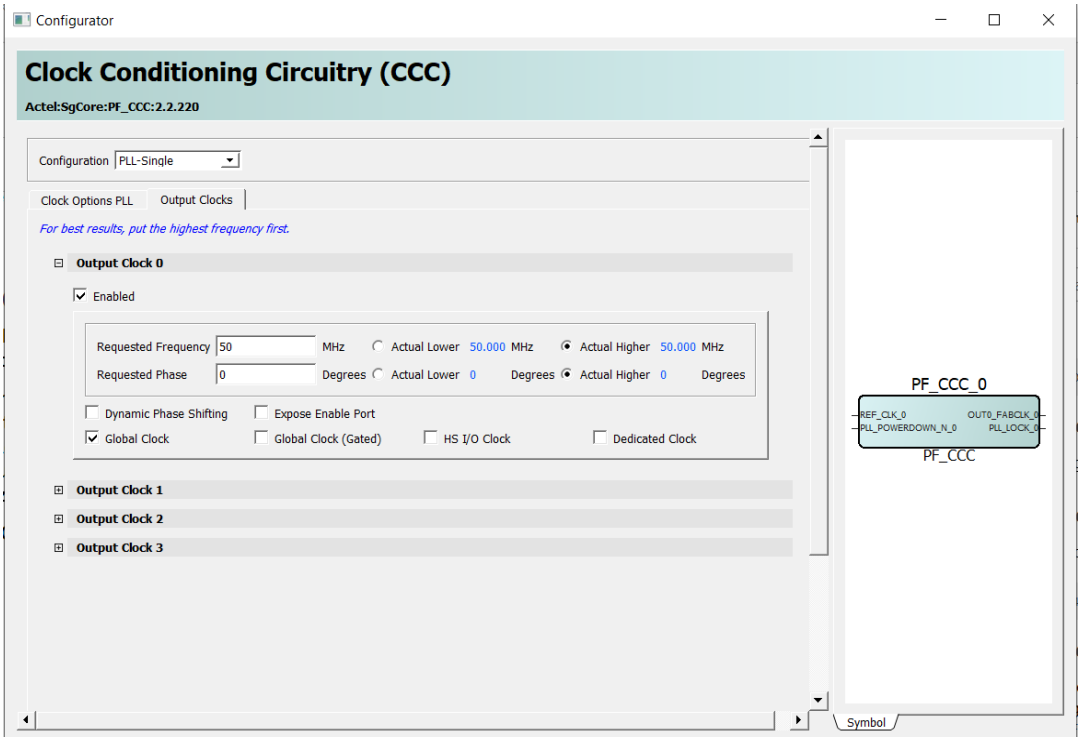
The following sections describe the IP cores used in the design and their configurations.

Important: The IP cores, which are not described in the following section, keep the default configuration.

4.1.1 PF_CCC_0 Configuration (Ask a Question)

The PF_CCC block provides a clock for the CoreABC and Dynamic Configuration Interface. The input for the Clock Conditioning Circuitry (CCC) is from the 160 MHz on-chip RC oscillator. In this design, the clock is configured to 50 MHz.

Figure 4-3. CCC Configuration



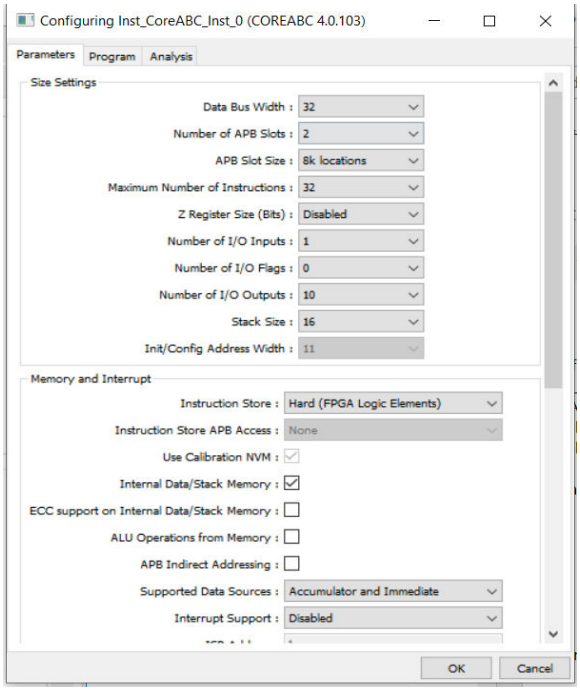
4.1.2 CoreABC (Ask a Question)

The CoreABC is a programmable soft-controller targeted for implementing the Advanced Microcontroller Bus Architecture (AMBA) based designs.

CoreABC in this design is connected to the Dynamic Reconfiguration Interface (DRI) as an APB3 master. The APB3 slave of DRI is connected to transceiver. The CoreABC initiates the DFE calibration sequence and dynamically performs Read/Write operation on the transceiver register. The number of APB slots, the APB slot size, and the maximum number of instructions are configured depending on the number of peripherals and address size used.

The following figure shows the parameter configuration of CoreABC interface.

Figure 4-4. CoreABC Configuration

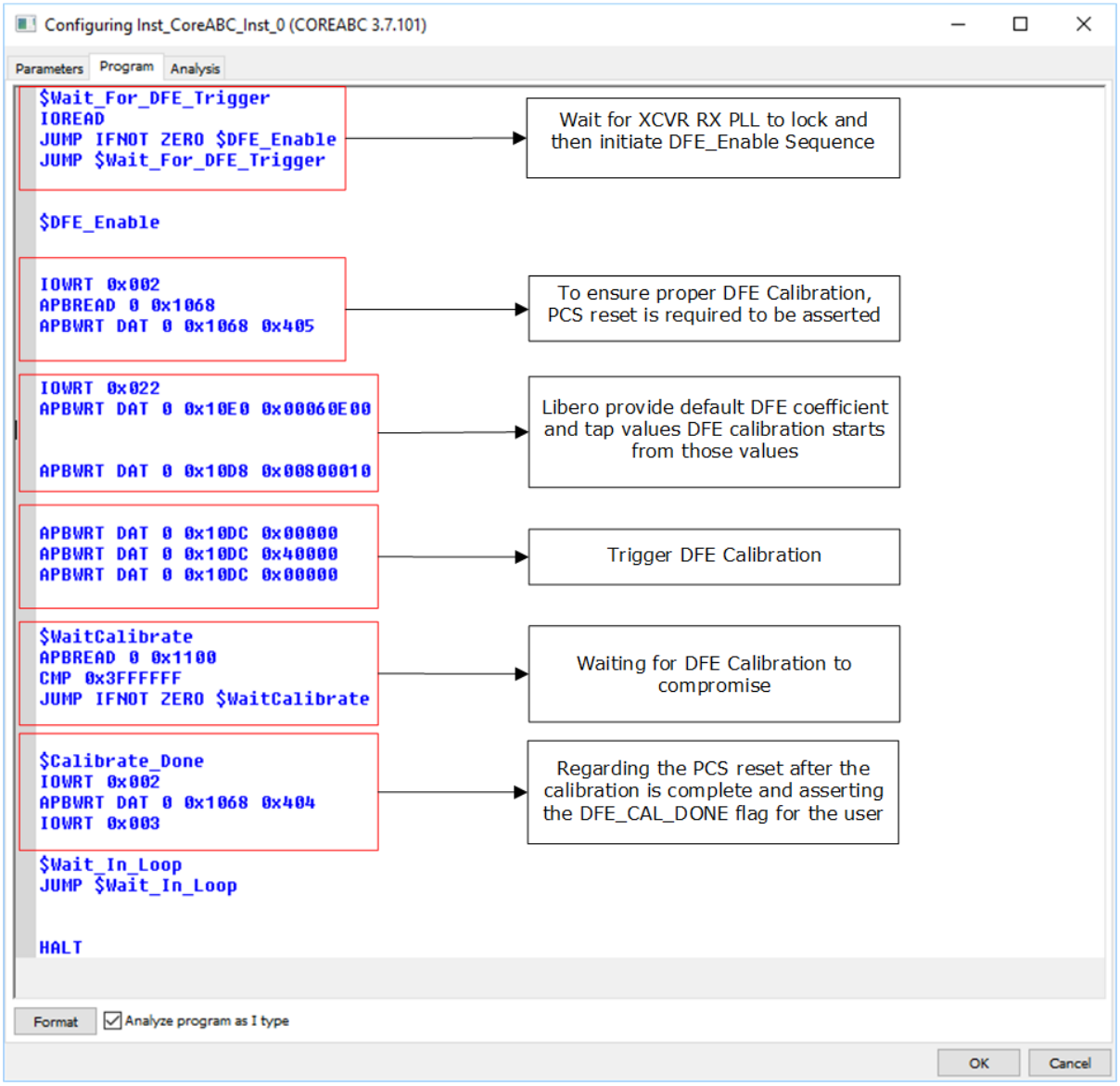


4.1.2.1 CoreABC Program (Ask a Question)

The following figure illustrates the register settings required for performing DFE calibration.

Important: The register address changes depending on the transceiver Quad and Lanes used. In this demo, Q2 Lane0 is used. For more information, see PolarFire Device Register Map and PolarFire SoC Device Register Map.

Figure 4-5. CoreABC Program

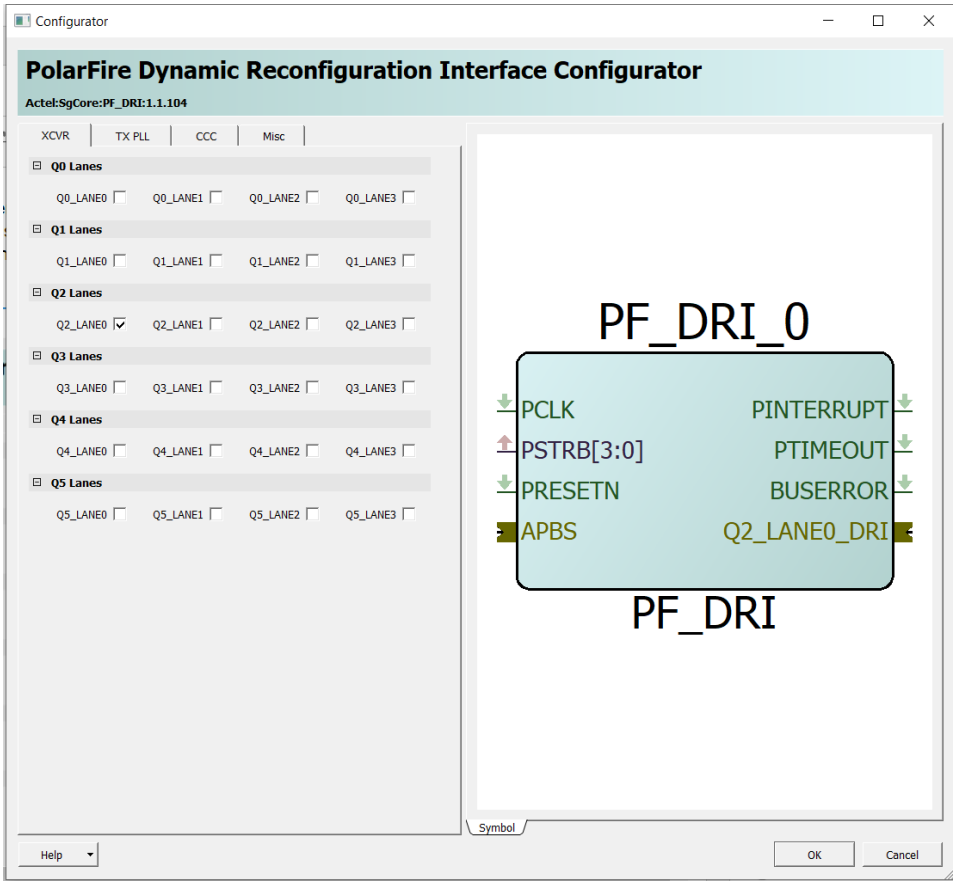


4.1.3 Dynamic Reconfiguration Interface (Ask a Question)

Dynamic Reconfiguration Interface (DRI) performs the run time configuration of transceiver PMA/PCS, PCIe, CCC, and Transmit PLLs after initialization.

In this demo design, DRI is used for performing run time calibration of transceiver and CCC. Q2_LANE0 is enabled to expose slave to the Transceiver Interface, as shown in the following figure.

Figure 4-6. PF_XCVR_DRI Configuration

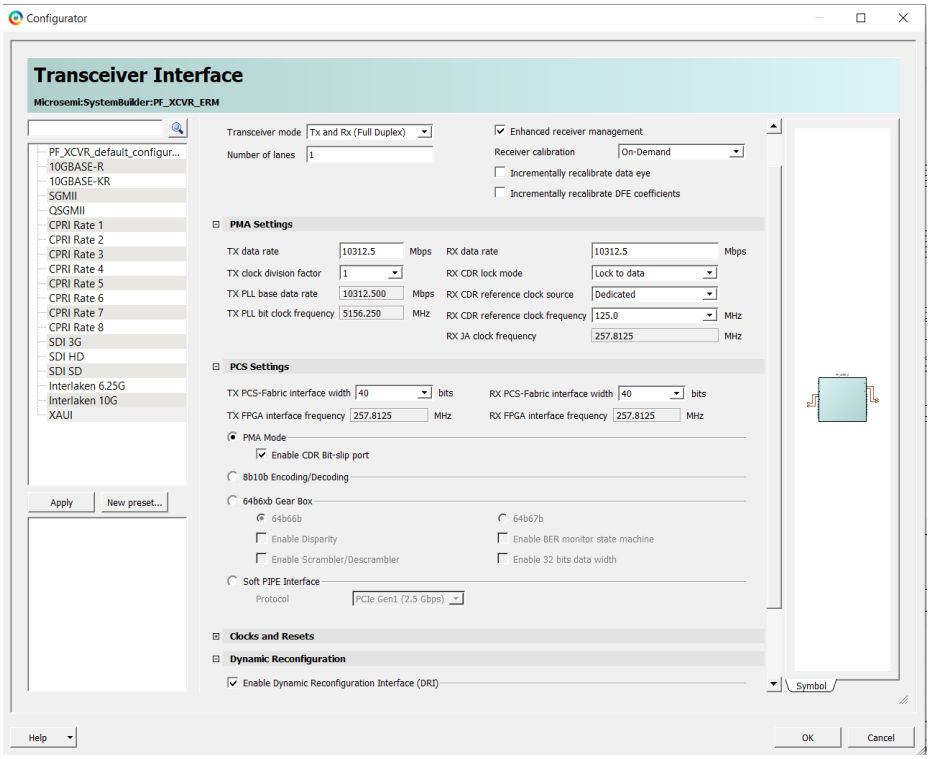


4.1.4 Transceiver Interface Reconfiguration (Ask a Question)

The PolarFire Transceiver Interface configurator is set to 10312.5 Mbps, 40-bit PCS-Fabric interface width,and native PMA mode. The ERM is enabled, and the receiver calibration is done on-demand.

The following figure shows the PolarFire Transceiver Interface configurator settings and how to enable DRI.

Figure 4-7. PolarFire Transceiver Reconfiguration GUI



Important: Incrementally recalibrate data eye is intended to improve the data eye for most gradients that typically occur due to temperature or voltage changes within the system. Incrementally recalibrate DFE coefficients is recomputed in an incremental manner when an initial calibration is performed. Incremental calibration of any two features is only applied after at least one full calibration is done.

4.1.5 PolarFire Transceiver Reference Clock (Ask a Question)

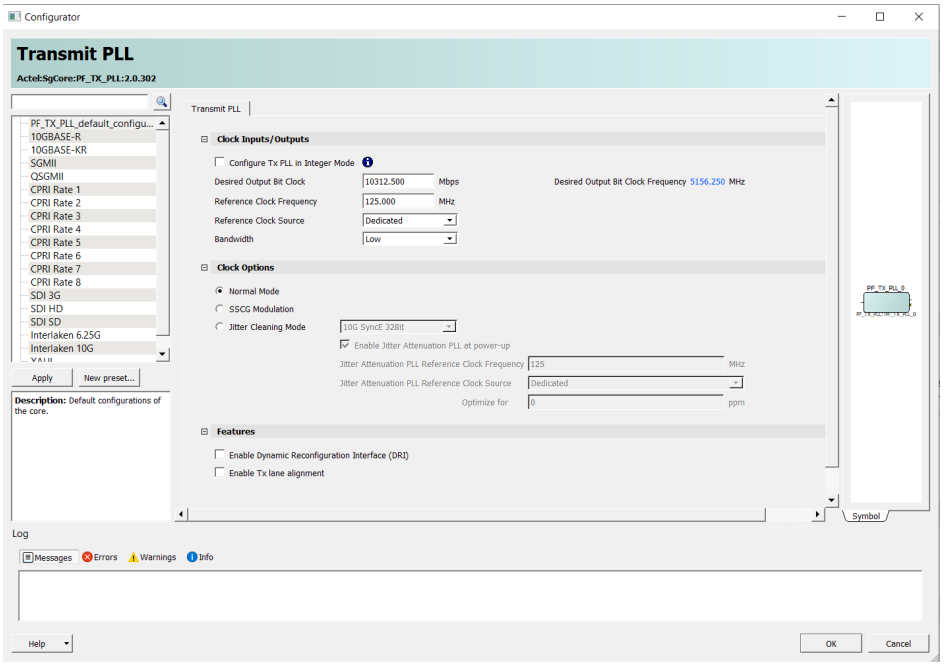
The transceiver reference clock is configured either as a differential clock or as a two single-ended REFCLKs. This design requires a single REFCLK. REFCLK sources the transceivers and global clock network in this design. The reference clock 0 is configured as a differential reference clock.

4.1.6 Transmit PLL (Ask a Question)

The transmit PLL reference clock and desired output clock are set to 125 MHz and 5156.25 MHz respectively,as shown in the following figure. The PolarFire transceiver is a half-rate architecture, which is the internal high-speed path uses both edges of the clock to keep the clock rates down. The clock thus runs at half of the data-rate, thereby consuming less dynamic power.

The following figure shows the Transmit PLL configurator.

Figure 4-8. Transmit PLL Configurator



4.1.7 Flag_for_RXPLL_Lock (Ask a Question)

The Flag_for_RXPLL_Lock signal looks for signal activity on the transceiver. This is done by looking for RX_READY going HIGH and RX_IDLE going LOW (RX_READY and RX_IDLE). The flag output is used as an input to CoreABC to start DFE.

4.1.8 PRBS Generator and Checker (Ask a Question)

The generator implements the PRBS polynomial and generates a continuous sequence of PRBS7 patterns of 40 bits each. The PRBS checker receives data from the transceiver to generate PRBS data locally and then the received data from both checker and generator are compared for data integrity. A lock signal is asserted if there is a data match otherwise, an error signal is asserted.

4.2 Port Description (Ask a Question)

The following table lists the port signals for this design.

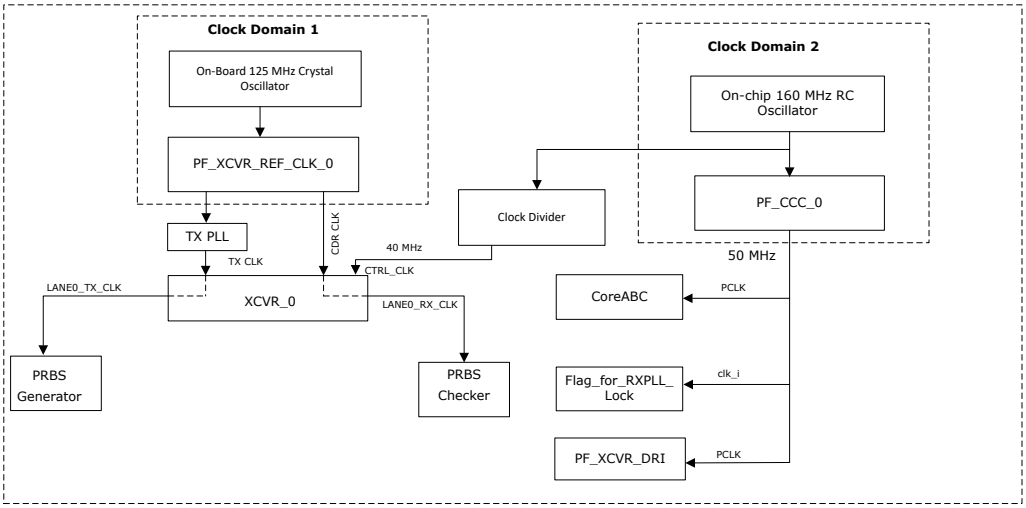
Table 4-1. Port Description

Signal	Direction	Description
REF_CLK_PAD_P and REF_CLK_PAD_N	Input	Differential reference clock is generated from the on-board 125 MHz oscillator
LANE0_RXD_N	Input	Transceiver receiver differential input
LANE0_RXD_P	Input	Transceiver receiver differential input
SWITCH	Input	DIP switch setting to initiate DFE calibration trigger for DFE calibration is also generated by user design using the condition (RX_READY and RX_IDLE)
LANE0_TXD_N	Output	Transceiver transmitter differential output
LANE0_TXD_P	Output	Error flag generated from PRBS checker module when there is data mismatch
error_out	Output	Dynamic CCC OUT3 Fabric Clock
Lock	Output	Lock signal flag generated from PRBS checker module when there is data match
DFE_CAL_DONE	Output	Output signal goes HIGH to indicate that DFE calibration is done
LANE0_CALIBRATING	Output	Output signal goes HIGH to indicate that the DFE/CDR is calibrating

4.3 Clocking Structure (Ask a Question)

In this design, there are two clock-domains. The on-board 125 MHz crystal oscillator drives the XCVR reference clock. XCVR REFCLK sources the transceivers and global clock network in this design. The on-chip 160 MHz RC oscillator drives CoreABC, Flag_for_RXPLL_lock, PF_XCVR_DRI block, and the ERM module of XCVR. The following figure shows the clocking structure in this design.

Figure 4-9. Clocking Structure



4.4 Reset Structure (Ask a Question)

In this design, the reset signal of the PRBS generator and the PRBS checker, are issued using the Reset_logic module. The Reset_sync_tx_0 (CoreReset_PF) module releases active-low reset of data generator block when the TX_CLK_STABLE signal from the PF_XCVR interface and the DEVICE_INIT_DONE signal from the PF_INIT_MONITOR block are asserted.

Similarly, the Reset_sync_rx_0 (CoreReset_PF) module releases active-low reset of data checker when the RX_READY signal from the PF_XCVR interface and the DEVICE_INIT_DONE signal from the PF_INIT_MONITOR block are asserted.

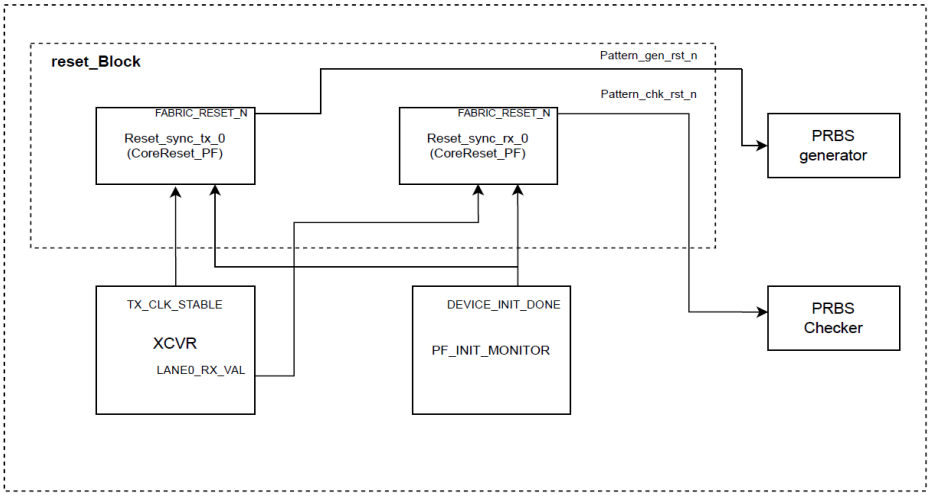
The previous setup ensures that the PRBS generation and PRBS checker does not start until TX_clock_stable and LANEO_RX_VAL are asserted respectively.

The DEVICE_INIT_DONE signal is asserted when the device initialization is completed. For more information about device initialization, see PolarFire Family Power-Up and Resets User Guide.

For more information on CoreReset_PF IP core, see CoreReset_PF from the Libero® SoC catalog.

The following figure shows the reset structure in this design.

Figure 4-10. Reset Structure



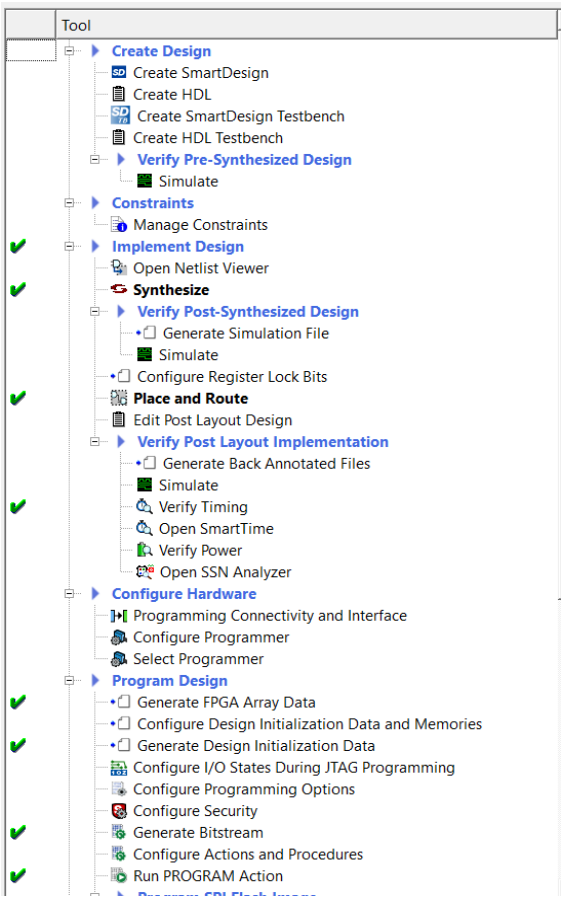
5. Libero Design Flow (Ask a Question)

The Libero design flow involves running the following processes in the Libero® SoC:

- Synthesize
- Resource Utilization
- Place and Route
- Verify Timing
- Design and Memory Initialization
- Generate Bitstream
- Run PROGRAM Action

The **Design Flow** tab options are depicted in the following figure.

Figure 5-1. Libero® Design Flow Options



5.1 Synthesize (Ask a Question)

To synthesize the design, perform the following steps:

1. On the **Design Flow** tab, double-click **Synthesize**. When the synthesis is successful, a green tick mark appears as shown in Figure 5-1.
2. Right-click **Synthesize** and click **View Report** to view the synthesis report and log files in the **Reports** tab.

5.2 Resource Utilization (Ask a Question)

The following table lists the resource utilization of the DFE design after synthesis.

Important: These values vary slightly for different Libero runs, settings, and seed values.

Table 5-1. Resource Utilization

Type	Used	Total	Percentage
4LUT	1259	299544	0.42
DFF	759	299544	0.25
I/O Register	0	1536	0.00
User I/O	5	512	0.98
Single-ended I/O	5	512	0.98
Differential I/O Pairs	0	256	0.00
uSRAM	0	2772	0.00
LSRAM	8	952	0.84
Math	0	924	0.00
H-Chip Global	3	48	6.25
Local Global	2	1008	0.20
PLL	1	8	12.50
DLL	0	8	0.00
BANKEN	1	7	14.29
CRN_INT	1	24	4.17
INIT	1	1	100.00
OSC_RC160MHZ	1	1	100.00
DRI	1	1	100.00
Transceiver Lanes	1	16	6.25
Transceiver PCIe	0	2	0.00
TX_PLL	1	11	9.09
XCVR_REF_CLK	1	11	9.09
ICB_CLKDIV	1	24	4.17
ICB_CLKINT	3	72	4.17
ICB_INT	1	12	8.33

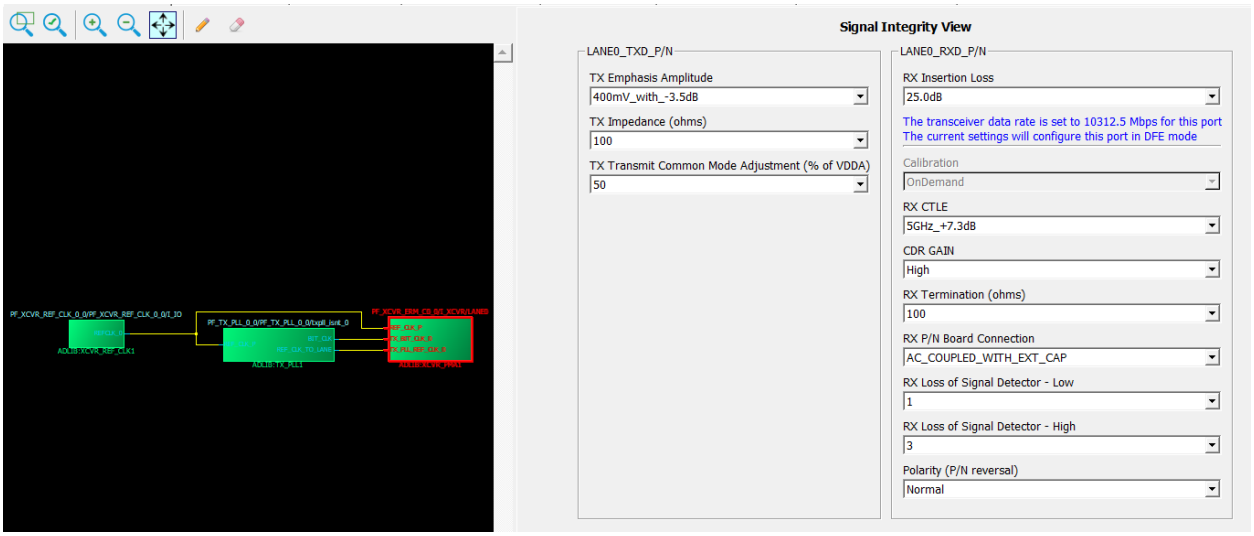
5.3 Place and Route (Ask a Question)

To place and route, perform the following steps:

1. On the **Design Flow** tab, double-click **Place and Route**, a green tick mark appears as shown in Figure 5-3.
2. To view I/O Editor in Transceiver view, on the **Design Flow** tab, double-click **Manage Constraints**.
3. On the **I/O Attributes** tab, from the **Edit** drop-down list, click **Edit with I/O Editor**.
4. In the **I/O Editor**, open **XCVR View**.

For DFE design, TX_PLL, XCVR_REF_CLK, and XCVR are constrained using the I/O Editor as shown in the following figure.

Figure 5-2. I/O Editor-Transceiver View

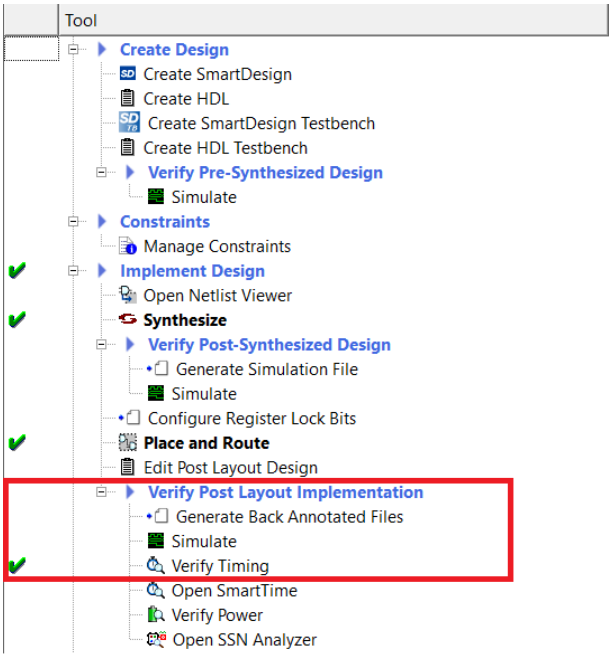


5.4 Verify Timing (Ask a Question)

To verify timing, perform the following steps:

1. On the **Design Flow** tab, double-click **Verify Timing**. When the design successfully meets the timing requirements, a green tick mark appears as shown in the following figure.
2. To view the verify timing report and log files on the **Reports** tab, right-click **Verify Timing**, and then click **View Report**.

Figure 5-3. Design Flow

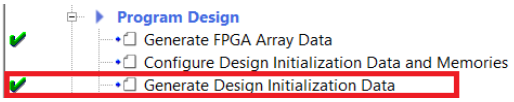


5.5 Design and Memory Initialization (Ask a Question)

Generate Design Initialization Data option is used to create the XCVR initialization client, which is used in the demo design. When the PolarFire device powers up, the transceiver block is initialized by the initialization client, generated during the Configure Design Initialization Data and Memories

stage in the design flow. For more information about device power-up, see PolarFire FPGA and PolarFire SoC FPGA Power-up and Resets User Guide .

Figure 5-4. Generate Design Initialization Data



5.6 Generate Bitstream (Ask a Question)

To generate the bitstream, perform the following steps:

1. To select the bitstream components: Custom security, Fabric and sNVM, right-click **Generate Bitstream**, and then click **Configure Options**.
2. On the **Design Flow** tab, double-click **Generate Bitstream**. When the bitstream is successfully generated, a green tick mark appears as shown in Figure 5-1.
3. To view the corresponding log file, on the **Reports** tab, right-click **Generate Bitstream** and then click **View Report**.

5.7 Run PROGRAM Action (Ask a Question)

After generating the bitstream, the PolarFire device must be programmed with the system services design.

To program the PolarFire device, perform the following steps:

1. Ensure that the following jumper settings are set on the board.

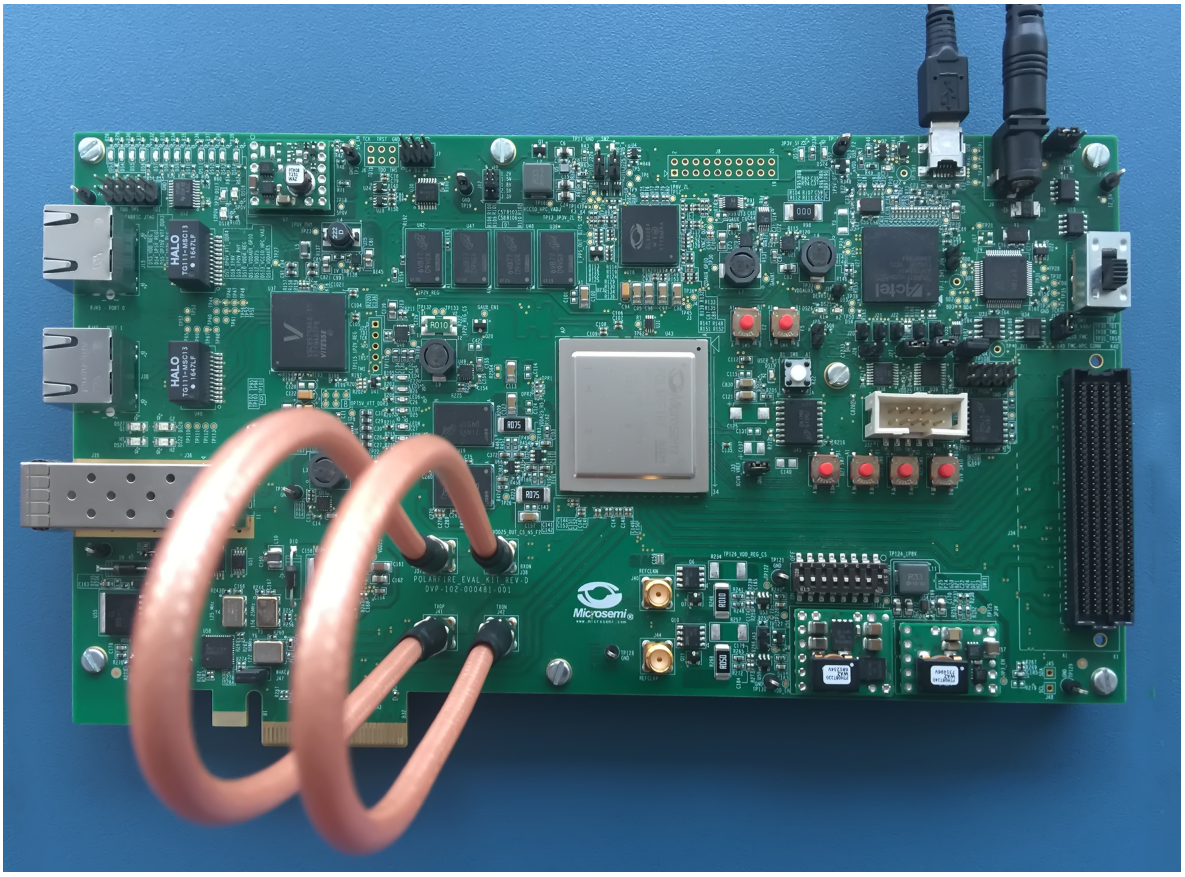
Table 5-2. Jumper Settings for PolarFire® Device Programming

Jumper	Description
J18, J19, J20, J21, and J22	Short pin 2 and 3 for programming the PolarFire® FPGA through FTDI
J28	Short pin 1 and 2 for programming through the onboard FlashPro5
J26	Short pin 1 and 2 for programming through the FTDI SPI
J27	Short pin 1 and 2 for programming through the FTDI SPI
J4	Short pin 1 and 2 for manual power switching using SW3
J12	Short pin 3 and 4 for 2.5 V
J46	Short pin 1 and 2 for routing 125 MHz differential clock oscillator output to the line side Open pin 1 and 2 for routing 122.88 MHz differential clock oscillator output to the line side

Important: The power supply switch must be switched off while making the jumper connections.

2. Connect the power supply cable to the **J9** connector on the board.
3. Connect the USB cable from the host PC to the **J5** (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.
5. Connect TXN to RXN and TXP to RXP using the 2 SMA to SMA cables as shown in the following figure.
   The following figure shows the board setup after these connections are made.

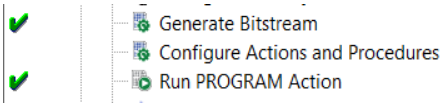
Figure 5-5. Board Setup



6. In the **Libero Design Flow**, double-click **Run PROGRAM Action**.

The device is successfully programmed and the onboard LEDs 4, 5, 6, and 7 glow. A green tick mark appears next to **Run PROGRAM Action** as shown in following figure.

Figure 5-6. Programming the Device



6. Running the Demo (Ask a Question)

This section describes how to optimize DFE coefficients and check the result on board.

Prerequisites for the procedure:

- The PolarFire Evaluation board is connected.
- The PolarFire FPGA is programmed with the DFE design.

To run the demo, perform the following steps:

1. After the device is programmed, change **SW11 DIP1** from 0 to 1. This brings the CoreABC interface out of reset and starts DFE calibration.

Important: Trigger for DFE calibration is also generated by monitoring the condition (RX_READY and RX_IDLE).

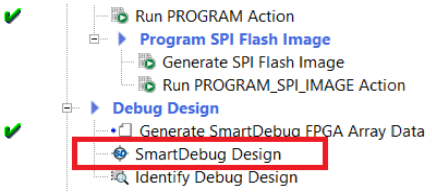
2. Observe if LED4 is OFF, and LED10 and LED5 are in ON state. This signifies that run time DFE calibration is complete and there is no bit error. Here LED4 represent bit error status, LED10 represent data lock flag signal, and LED5 represents DFE calibration status.

Eye Monitor enables visualizing the eye diagram present within the receiver. This feature plots the receive eye after the CTLE and DFE functions. For plotting the **Eye Diagram**, follow the following procedure.

On the **Design Flow** window, perform the following steps:

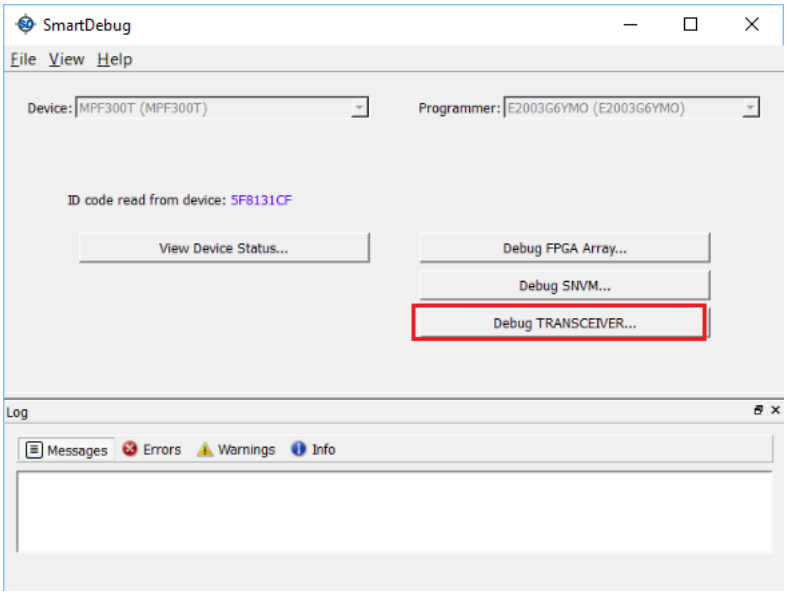
1. To generate data for **SmartDebug Design**, click **Generate SmartDebug FPGA Array Data**. Once the data is generated, a green tick mark is seen on the left side of the option indicating that the data generation is successful.
2. To open **SmartDebug Design**, double-click **Debug Design**.

Figure 6-1. Launching SmartDebug Design



3. Open the **SmartDebug** window, and then click **Debug TRANSCEIVER** as shown in following figure.

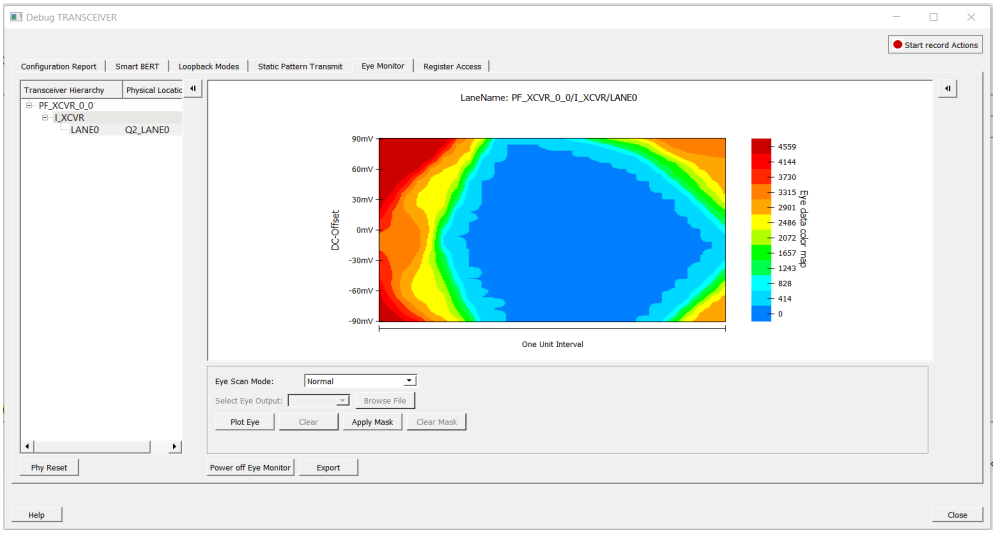
Figure 6-2. SmartDebug Window Debug Options



4. On **EYE Monitor** tab, select **LANE0**.
5. To plot the eye, click **Plot Eye**.

The following figure shows the **Eye Plot**.

Figure 6-3. Eye Plot



7. Appendix 1: Programming the Device Using FlashPro Express (Ask a Question)

This section describes how to program the PolarFire device with the Job programming file using a FlashPro programmer. The default location of the Job file is located at the following location: `mpf_an4950_v2023p1_df\Programming_Job\top.job`

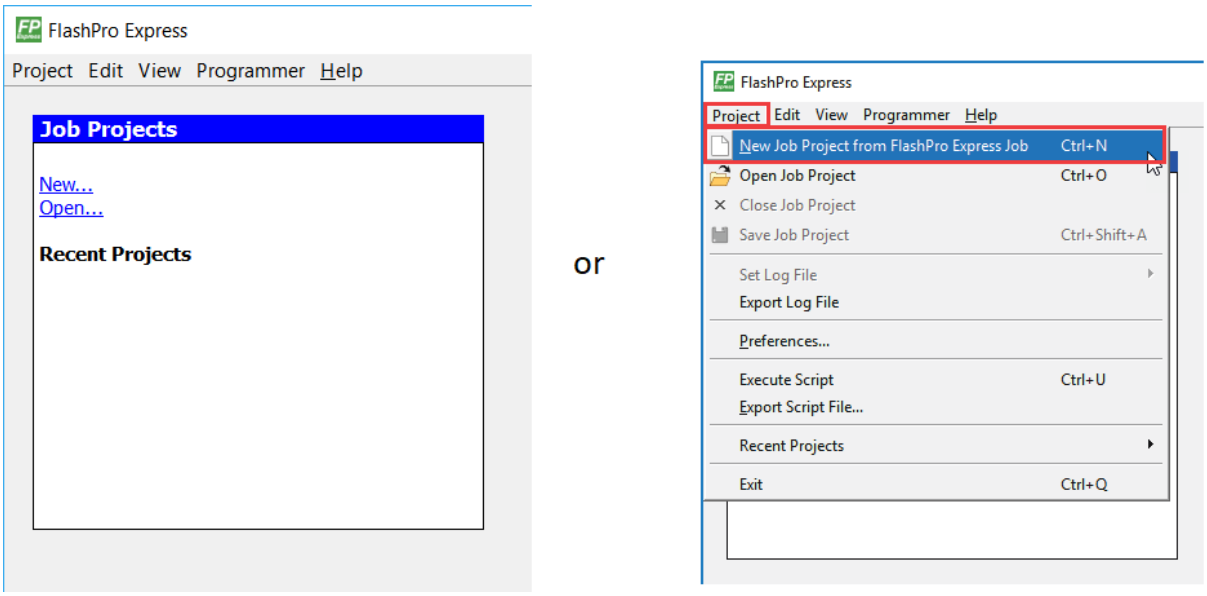
To program the PolarFire device using FlashPro Express, perform the following steps:

1. Ensure that the jumper settings on the board are the same as listed in Table 5-2.

> **Important:** The power supply switch must be switched off while making the jumper connections.

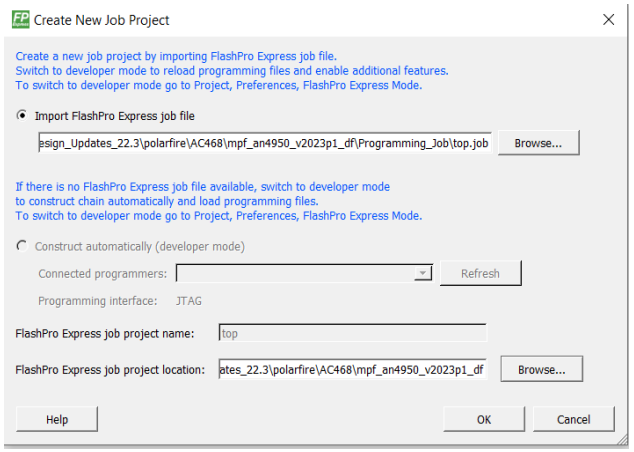
2. Connect the power supply cable to the **J9** connector on the board.
3. Connect the USB cable from the Host PC to the **J5** (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.
5. On the host PC, launch the FlashPro Express software.
6. To create a new job, click **New** or in the **Project** menu, click **New Job Project from FlashPro Express Job** as shown in the following figure.

Figure 7-1. FlashPro Express Job Project



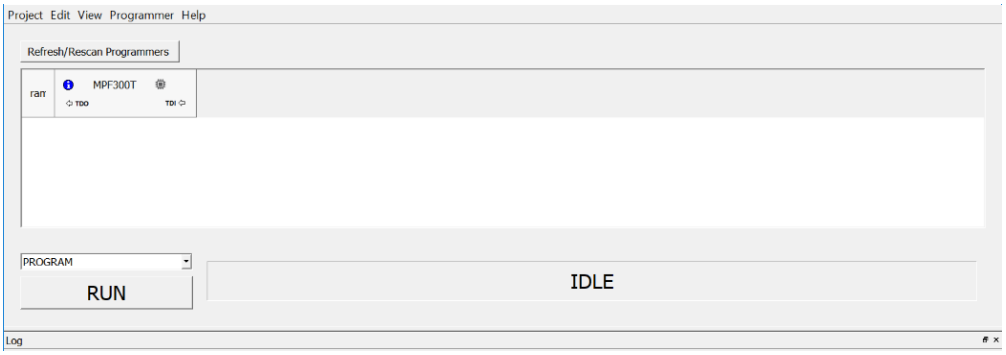
7. Enter the following files in the **Create New Job Project** dialog box:
   - **Programming job file**: Click **Browse**, navigate to the location where the `.job` file is located, and select the file. The default location is: `mpf_an4950_v2023p1_df\Programming_Job\top.job`.
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.

Figure 7-2. New Job Project from FlashPro Express Job



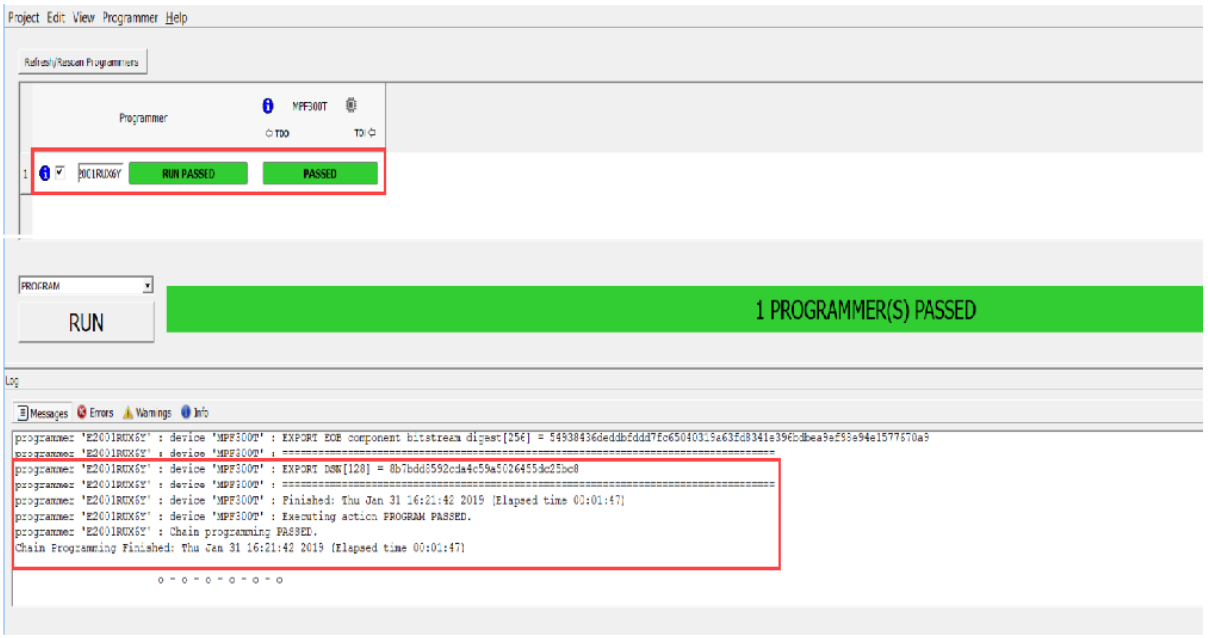
8. Click **OK.** The required programming file is selected and ready to be programmed in the device.
9. The **FlashPro Express** window appears as shown in the following figure. Confirm that a programmer number appears in the **Programmer** field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.

Figure 7-3. Programming the Device



10. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure.

Figure 7-4. FlashPro Express—RUN PASSED



11. To close **FlashPro Express**, click the close button or on the **Project** tab, click **Exit**.

8. Appendix 2: Running the Tcl Script (Ask a Question)

TCL scripts are provided in the design files folder under directory `TCL_Scripts`. If required, the design flow is reproduced from Design Implementation till generation of job file.

To run the TCL, perform the following steps:

1. Launch the **Libero** software.
2. Click **Project** > **Execute Script**.
3. Click **Browse** and in the downloaded `TCL_Scripts` directory, select `script.tcl`.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within `TCL_Scripts` directory.

For more information about TCL scripts, see `mpf_an4950_v2023p1_df\TCL_Scripts\readme.txt`

For more details on TCL commands, see Tcl Commands Reference Guide.

9. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 9-1. Revision History

Revision	Date	Description
A	08/2023	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template • The document number was updated to AN4950 from AC468 • Updated Introduction and 2. Design Requirements sections • Replaced Figure 4-2 in the 4.1. Design Implementation section • Replaced Figure 4-3 in the 4.1.1. PF_CCC_0 Configuration • Replaced Figure 4-4 in the 4.1.2. CoreABC • Replaced Figure 4-6 in the 4.1.3. Dynamic Reconfiguration Interface • Replaced Figure 4-7 and added a note in the 4.1.4. Transceiver Interface Reconfiguration • Replaced Figure 4-8 and updated the 4.1.6. Transmit PLL • Updated 4.2. Port Description by adding 2 signals • Replaced Figure 4-10 and updated the 4.4. Reset Structure • Removed Point 5 and replaced Figure 6-3 in the 6. Running the Demo • Updated the Table 5-1 • Replaced job file path in the and replaced Figure 7-2 in the 7. Appendix 1: Programming the Device Using FlashPro Express • Replaced readme.txt file path in the 8. Appendix 2: Running the Tcl Script
6	—	The following is the list of changes in revision 6 of the document: Added 8. Appendix 2: Running the Tcl Script section
5	—	The following is the list of changes in revision 5 of the document: • Updated the document for Libero® SoC v12.2 • Removed the references to Libero version numbers
4	—	Updated the document for Libero SoC v12.0
3	—	Updated the document for Libero SoC PolarFire v2.3
2	—	Updated the document for Libero SoC v12.2
1	—	The first publication of this document

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