AN2497

Designing Digital RF Receiver Using MCP37DXX High-Speed ADC

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INTRODUCTION

In recent years, digital RF receiver technology has made significant progress, mainly due to the availability of high-speed ADCs. The direct conversion, IF sampling and software defined radio architectures are becoming common practice in the modern RF receiver design.

Due to ongoing advances in chip manufacturing and ADC design technologies, many of the Digital Signal Processing (DSP) functions, which used to be in separate devices or done by software, are now included in the ADC itself.

For example, the MCP37XXX high-speed ADC includes various programmable Digital Signal Processing building blocks for specific applications, such as (a) Digital Down-Conversion for in-phase and quadrature signal detection, (b) digital decimation filtering for higher Signal-to-Noise Ratio (SNR) and (c) Continuous-Wave (CW) beamforming for the phase correction of acquired signals from multiple inputs, such as signals from phased array antennas or ultrasound transducers.

These built-in digital building blocks can greatly reduce the overall system hardware requirements, while also improving the system performance. The reduced system component requirements and lower power consumption enable lower overall system cost, and make portable system design much easier and simpler[4].

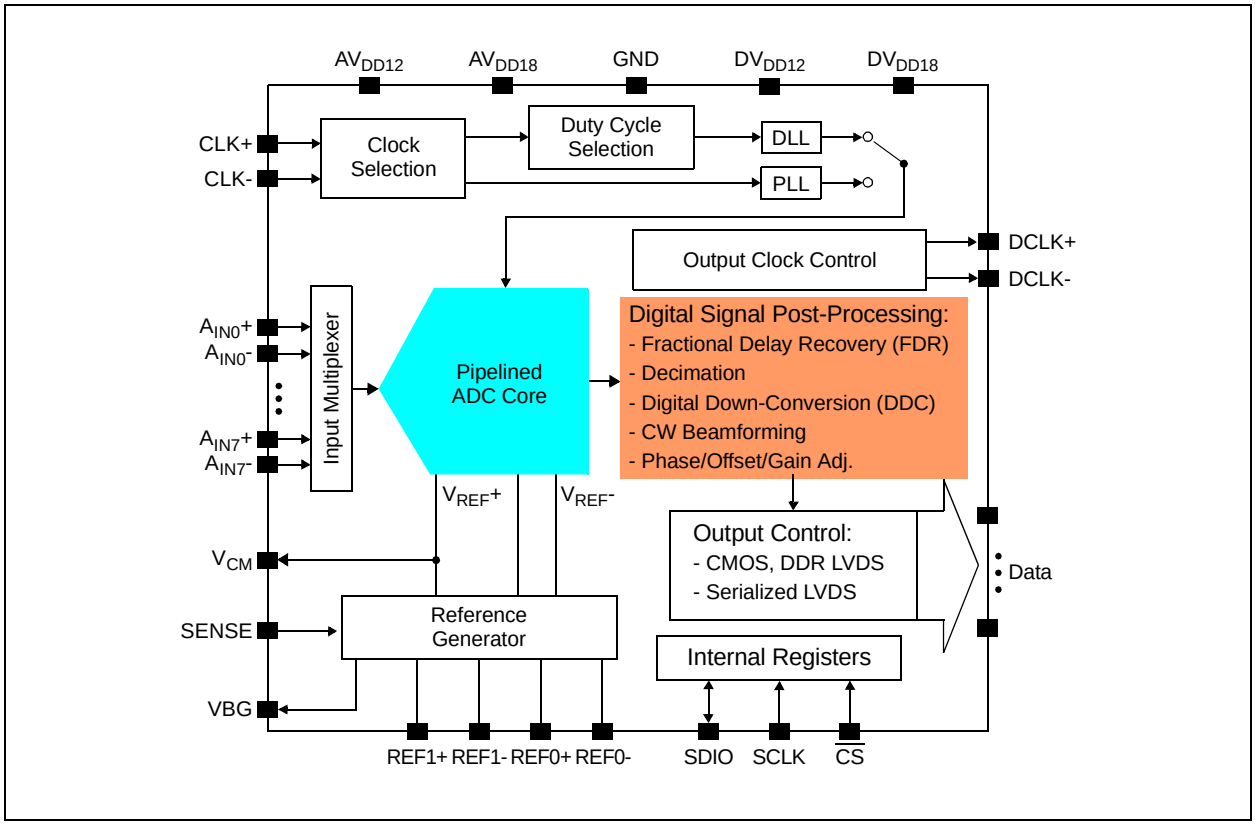

FIGURE 1: *Block Diagram of Digitally Enhanced ADC with Built-In Digital Signal Post-Processing Features*[1-2].

BUILT-IN DIGITAL SIGNAL PROCESSING BUILDING BLOCKS[1-3]

Figure 1 shows a simplified block diagram of a multi-channel high-speed ADC with built-in Digital Signal Post-Processing (DSPP) features. The analog input signal is digitized by the ADC core and post-processed internally, depending on the user's selection, before the digital output is available at the output pins.

The optional DSPP features are (a) Fractional Delay Recovery, (b) decimation, (c) Digital Down-Conversion, (d) CW beamforming and (e) phase/offset/gain adjustment per channel. These digital options are selectable using user Configuration register bit settings, which are dynamically programmable on the fly. Table 1 summarizes these Digital Signal Processing options.

TABLE 1: BUILT-IN DIGITAL SIGNAL POST-PROCESSING FEATURES

Features	Descriptions	Applications	Availability
Fractional Delay Recovery (FDR)	Digitally compensates the time delay of the sampling events between input channels. Without using FDR, the input sampling time difference between adjacent channels is 1 ADC core clock cycle. When FDR is enabled, the time difference is synthetically reduced to less than 1 ns.	This feature is only needed in Multichannel mode.	Available in Dual and Octal-Channel mode only. In other modes, the FDR can be done by software in the host device if needed.
Decimation	Finite Impulse Response (FIR) decimation filter for higher SNR. When applied, the output data throughput is reduced by the decimation factor, N.	This is a preferred option for high-resolution imaging applications or when higher SNR is needed.	• Single and Dual Channel modes • CW Octal-Channel mode
Digital Down-Conversion (DDC)	In-Phase and Quadrature Component Detection: • Shifts the input frequency spectrum to lower frequency band. • Outputs the resulting signal as either I/Q data or as a real signal centered at ¼ of the output data rate.	• Software defined radio • Wireless communications, including: radar, sonar, ultrasound sensors, etc.	• Single and Dual Channel modes • CW Octal-Channel mode
CW Beamforming	In octal-channel configuration, beamforming is used to correct the time delay of the incoming signals (at input pin) with respect to the reference. The beamforming is achieved by controlling the phase and gain of each input channel individually.	• Octal-channel transducers for ultrasound/sonar • Phased array antenna	Octal-Channel mode only.
Phase/Offset/ Gain Adjustment per Each Channel.	Digital correction of phase, offset and gain of individual channel.	—	Available for all Channel modes.

USING FRACTIONAL DELAY RECOVERY (FDR) FOR MULTICHANNEL CONFIGURATION[1]

When the device is used in Multichannel mode, it samples the channel inputs sequentially using a MUX, while the single ADC core is operating at a constant full speed. This sequential sampling of multiple channels introduces a time delay between the sampling of different input channels relative to a multicore ADC, which samples all inputs at the same instant. The Fractional Delay Recovery (FDR) option digitally compensates the time delay of the sampling events.

When the FDR is enabled, a high-order, band limited interpolation filter deskews the sampling instant within a limited input bandwidth and synthetically removes the time delay of the input sampling. The FDR is available in Dual Channel and Octal-Channel modes.

USING DIGITAL DECIMATION FILTER[1-3]

The Finite Impulse Response (FIR) decimation filter can be applied when a higher SNR is needed or to provide out-of-band rejection for the desired signal. The output bandwidth of the FIR filter is reduced by the decimation factor, N. The final output bandwidth of the FIR filter is determined by dividing the ADC sampling rate by N.

In conventional applications, the digital decimation is typically processed at the host computing device. This process takes extra resource time from the computing device and can delay the decision-making process. Instead, this decimation filter can be applied within the ADC before the digital output is available to the host device, reducing the resource overhead of the computing device.

Figure 2 shows the performance of a 16-bit 200 Msps ADC before any decimation is applied. The ADC achieves an SNR of 74.7 dBFS. Table 1 shows the overall SNR performance versus decimation settings. The SNR is improved with higher decimation rates. About 2.5 dB improvement is achieved per step (2x per step), up to a decimation rate of 128x. The SNR improvement becomes almost flat after the decimation rate reaches about 128x. An SNR of 92.3 dBFS can be achieved with the 512x decimation setting using the 200 Msps 16-bit ADC. This is a significant improvement compared to the performance of typical high-speed ADCs without this feature. See Reference [1-3] for more details on using the digital decimation filter.

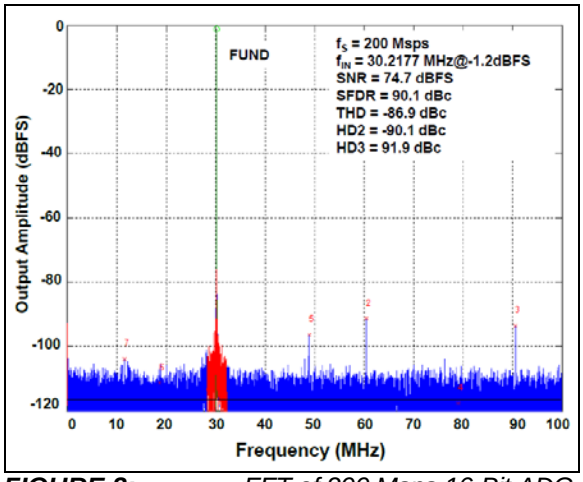

FIGURE 2: *FFT of 200 Msps 16-Bit ADC Output:*[1] *Input (F_{IN}) = 30.2177 MHz @ -1.2 dBFS, SNR = 74.7 dBFS, SFDR = 90.1 dBc.*

TABLE 2: DECIMATION RATE vs. SNR PERFORMANCE

Decimation Rate	SNR (dBFS)
	16-Bit Output Mode
8x	82.3
16x	84.8
32x	87.1
64x	89.2
128x	91.0
256x	92.0
512x	92.3

USING DIGITAL DOWN-CONVERSION (DDC) FEATURE FOR WIRELESS APPLICATIONS[1-4]

Figure 3 shows a simplified block diagram of the built-in DDC configuration. The DDC includes a 32-bit complex Numerically Controlled Oscillator (NCO), a selectable (high/low) half-band filter, optional decimation filters and two Output modes (I/Q or $f_S/8$). Frequency translation is accomplished by the NCO. The NCO frequency is programmable, anywhere from 0 Hz to the input Sampling Frequency (f_S). Phase and amplitude dither can be enabled to improve spurious performance of the NCO.

Each of the processing sub-blocks are individually controlled using register settings. This DDC feature can be used to simplify various RF receiving system designs and to reduce system cost. Figure 6 shows an example of Software Defined Radio (SDR) using the MCP37DXX. As shown in the figure, the entire digital IF block in the SDR can be replaced with a single MCP37DXX.

The FFT output from the ADC core is shown in Figure 2 for a 30.2177 MHz input signal. When the NCO is set at 31 MHz, the I/Q signals appear at 0.7823 MHz. Figure 4 shows the I/Q output signals: (a) when the decimation filter is not applied and (b) when the decimation filter (16x) is applied. Figure 5 shows the output signal when upconverted by $f_S/8$/DER, where DER is the decimation rate applied (16x). See Reference [1-4] for more details on the Digital Down-Conversion feature.

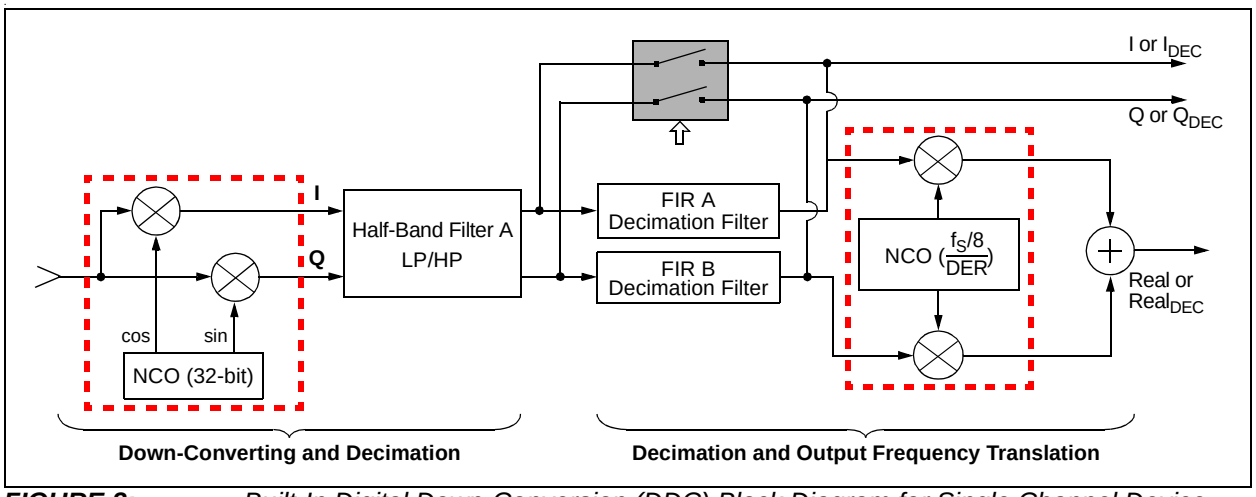

FIGURE 3: *Built-In Digital Down-Conversion (DDC) Block Diagram for Single Channel Device.*

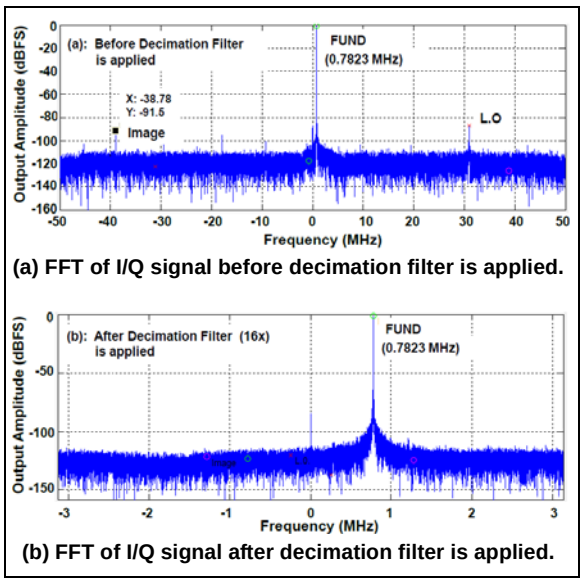

FIGURE 4: *FFT of In-Phase and Quadrature Signal after Digital Down-Conversion.*

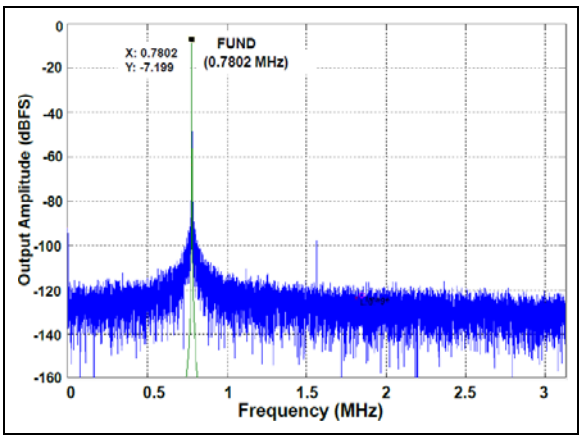

FIGURE 5: *FFT of Upconverter Output.*

USING DIGITAL DOWN-CONVERSION FOR SOFTWARE DEFINED RADIO (SDR)

Figure 6 shows an example of a software defined radio receiver employing a super-heterodyne, dual stage conversion architecture. This architecture is popularly used in various modern digital RF communication systems, including LTE, IEEE 802.11. The received Radio Frequency (RF) signal is down-converted to an Intermediate Frequency (IF) in the first stage and then converted to baseband signals in the second stage. The second stage includes an ADC, which digitizes the IF signal, and a Digital Down-Conversion circuit, which converts the digitized IF signal to the in-phase and quadrature baseband signals. The Digital Down-Conversion block includes a Numerically Controlled Oscillator (NCO), digital mixers, I/Q demodulation and FIR decimation filters.

In a conventional digital radio architecture, the Digital Down-Conversion is typically achieved by extensive firmware operations using a high-end Field Programmable Gate Array (FPGA) device. The firmware development and management are very time-consuming tasks for the system designers. Additionally, the FPGA tends to be the highest cost component in many systems.

Instead of implementing the digital IF processing block with discrete components, or using extensive FPGA-based logic, system designers can now utilize the built-in Digital Down-Conversion (DDC) feature in the MCP37DXX ADC. As shown in Figure 6, the MCP37DXX minimizes the RF components needed for the RF receiver design and simplifies the system architecture.

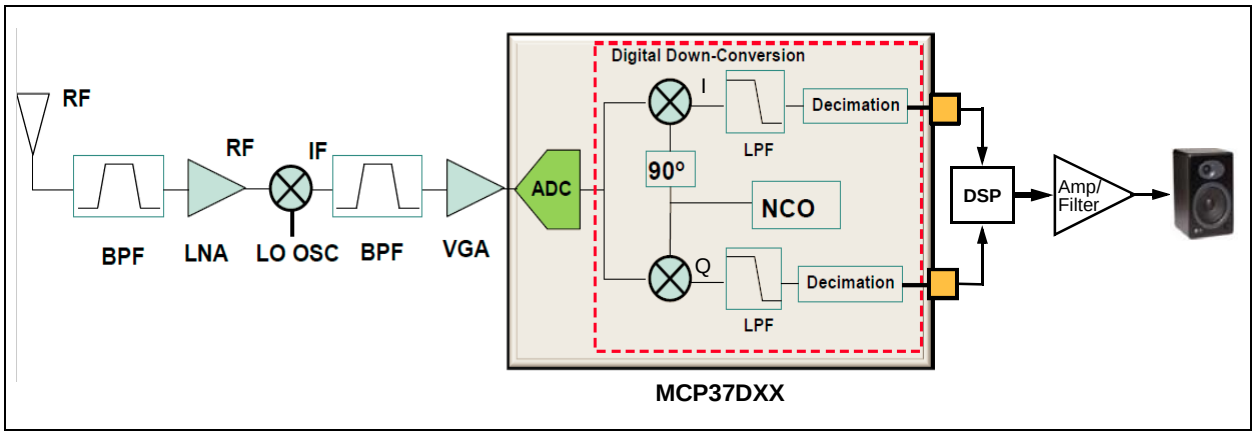

FIGURE 6: *Example of Using the MCP37DXX for Software Defined Radio.*

USING DIGITAL BEAMFORMING[1-3]

Digital beamforming is widely used in the sonar, radar and ultrasound imaging systems, where multiple antenna/transducers are used. When a large number of antennas/transducers is used, the signals from each receiving element arrive at the detection device with a different time delay. Also, in multichannel scanning operations using the MUX, there is a time delay between acquiring input signals. These time delays can be corrected before all input signals are combined for the final signal processing.

The time delay correction involves the phase alignment of the detected signals with respect to a reference.

The MCP37D31/21-200 device has built-in Continuous-Wave (CW) digital beamforming and Doppler signal processing features, which are available in the octal-channel operation only. These features can significantly simplify the conventional beamforming circuits.

Figure 7 shows a simplified block diagram for continuous beamforming with the DDC I/Q decimation stage. The device achieves beamforming by scanning all inputs while correcting the phase of each channel with respect to a reference. This can be done using:[1]

- Fractional Delay Recovery (FDR)
- Phase offset settings of each individual channel
- Gain setting per channel

While the input channel is multiplexed sequentially, the phase offset can be added to the NCO output (each channel individually), which corrects the time delay of the incoming signals with respect to the reference[1].

The phase compensated input signal is then down-converted by a wide dynamic range I/Q demodulator stage. The digital beamforming of the inputs is then obtained by summing I and Q data from individual channels. This summed I and Q data are fed to the half-band filter. Equation 1 shows the I and Q data of an individual channel with phase, gain and offset correction, and the resulting digital beamforming signal.

The processing blocks, after the digital beamforming, are the same as for the DDC single channel operation[1].

EQUATION 1: BEAMFORMING SIGNALS

$$I_{CH(n)} = ADC(n, G, \delta) \times COS(2\pi f_{NCO} t + \phi(n))$$

$$Q_{CH(n)} = ADC(n, G, \delta) \times SIN(2\pi f_{NCO} t + \phi(n))$$

$$I = \sum_{n=0}^{N} I_{CH(n)} \quad \text{and} \quad Q = \sum_{n=0}^{N} Q_{CH(n)}$$

Where:

ADC(n) = ADC output of Channel n
δ = Digital offset adjustment of Channel n
G = Digital gain adjustment of Channel n
ϕ(n) = NCO phase offset of Channel n

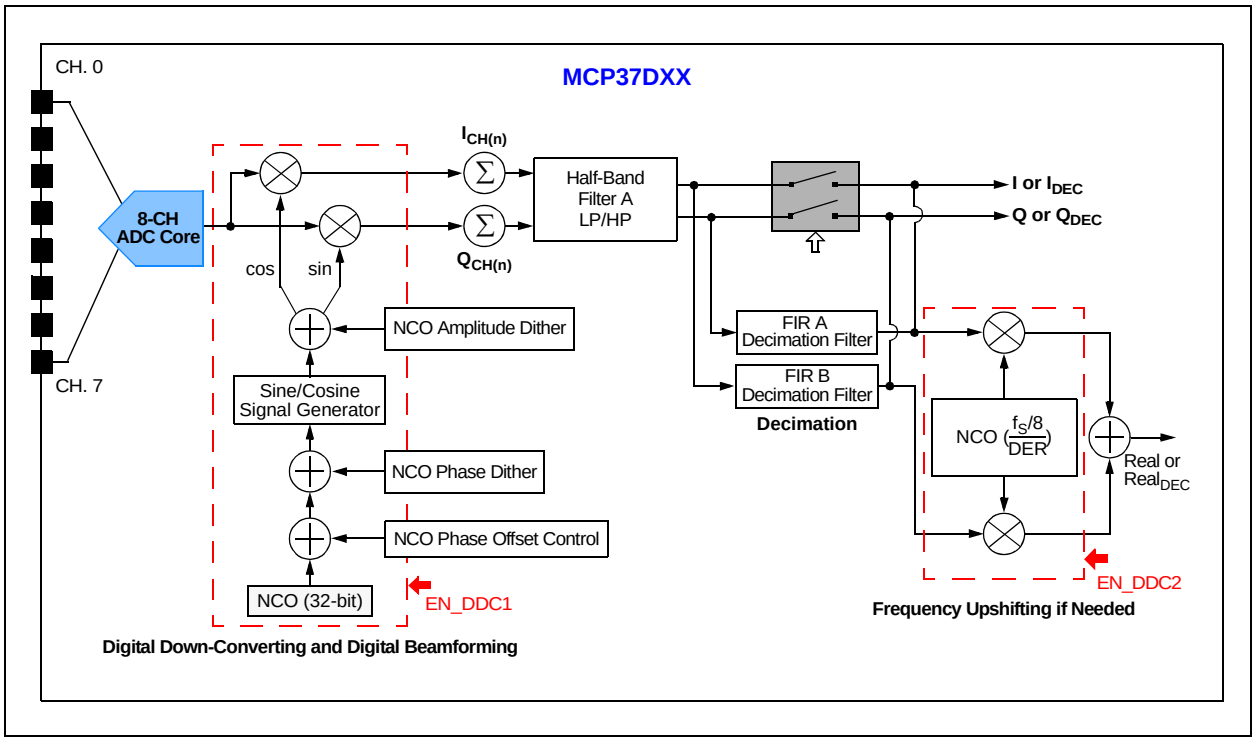

FIGURE 7: *Digital Beamforming Block Diagram in Octal-Channel Configuration*[1].

USING DIGITAL BEAMFORMING FOR ULTRASOUND IMAGING SYSTEMS

Figure 8 shows a simplified block diagram for the ultrasound imaging system, which utilizes analog and digital beamforming with DDC I/Q decimation.

The digital beamforming that is performed inside the FPGA unit can be achieved using the built-in feature set in the MCP37DXX.

Doppler shift measurement requires summing the input signals from multiple transducer channels and mixing them with a phase controlled local oscillator frequency.

The resulting low-frequency output is then centered near DC and can measure a Doppler shift produced by moving objects, such as blood flow, changes in blood pressure in arteries, etc. The I/Q outputs that represent the Doppler shift can be processed using the 1 Msps 16-bit SAR ADCs, such as MCP33131.

The MX57XXX and DSC400 clock devices from Microchip can be used to provide the timing source of each building block.

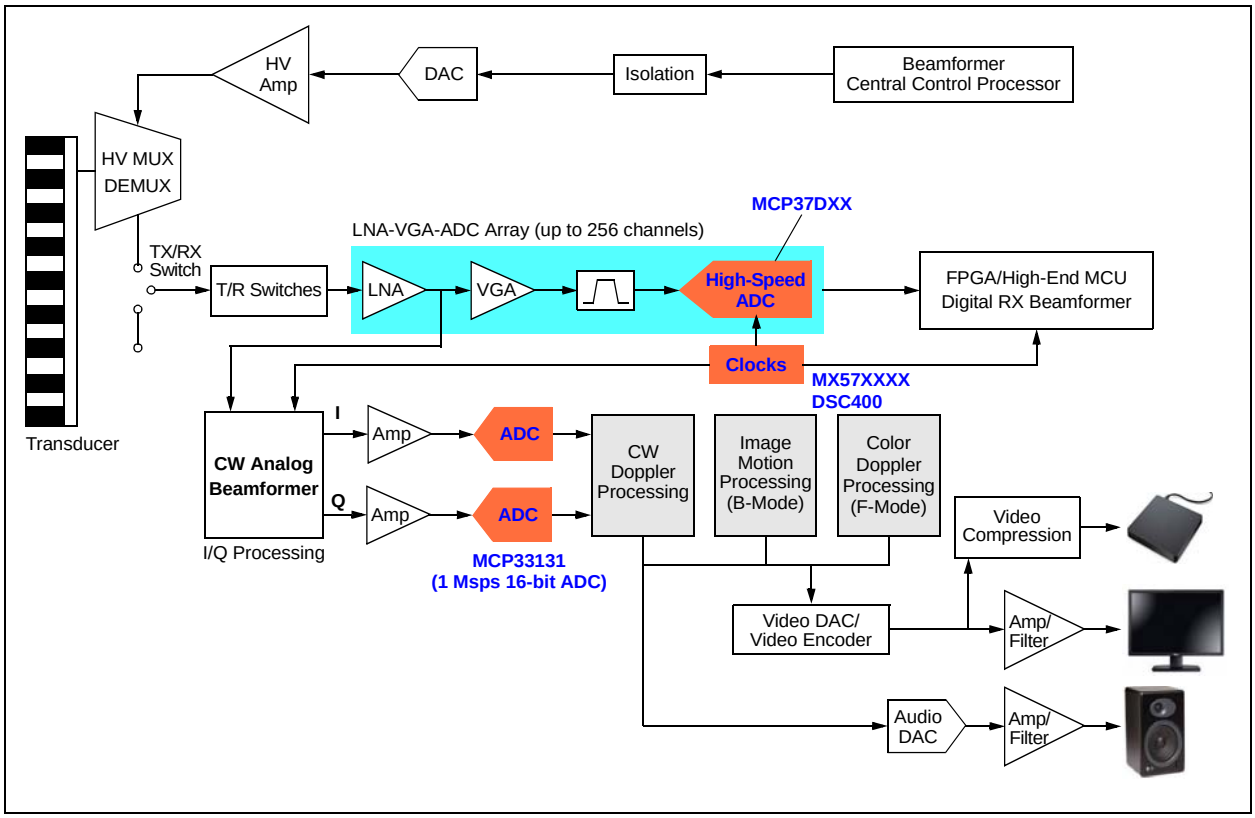

FIGURE 8: *Example of Ultrasound Imaging System Building Block.*

USING MCP37DXX FOR SONAR SYSTEMS

Figure 9 shows an example of a receiver block diagram for Sonar. The octal-channel MCP37DXX is an ideal device for the Sonar receiver design. The device's DDC and digital beamforming feature can be utilized.

In Octal-Channel mode, the amplitude and time delay of the incoming signals of each channel are digitally corrected, with respect to the reference. The digital beamforming of the inputs is then obtained by summing I and Q signals from individual channels.

The Doppler signal information for the moving target can be easily extracted from the I and Q data.

Note:	The digital beamforming is available in Octal-Channel mode only. Other than Octal-Channel mode, the offset and gain control for each individual channel is still available, except the phase control.

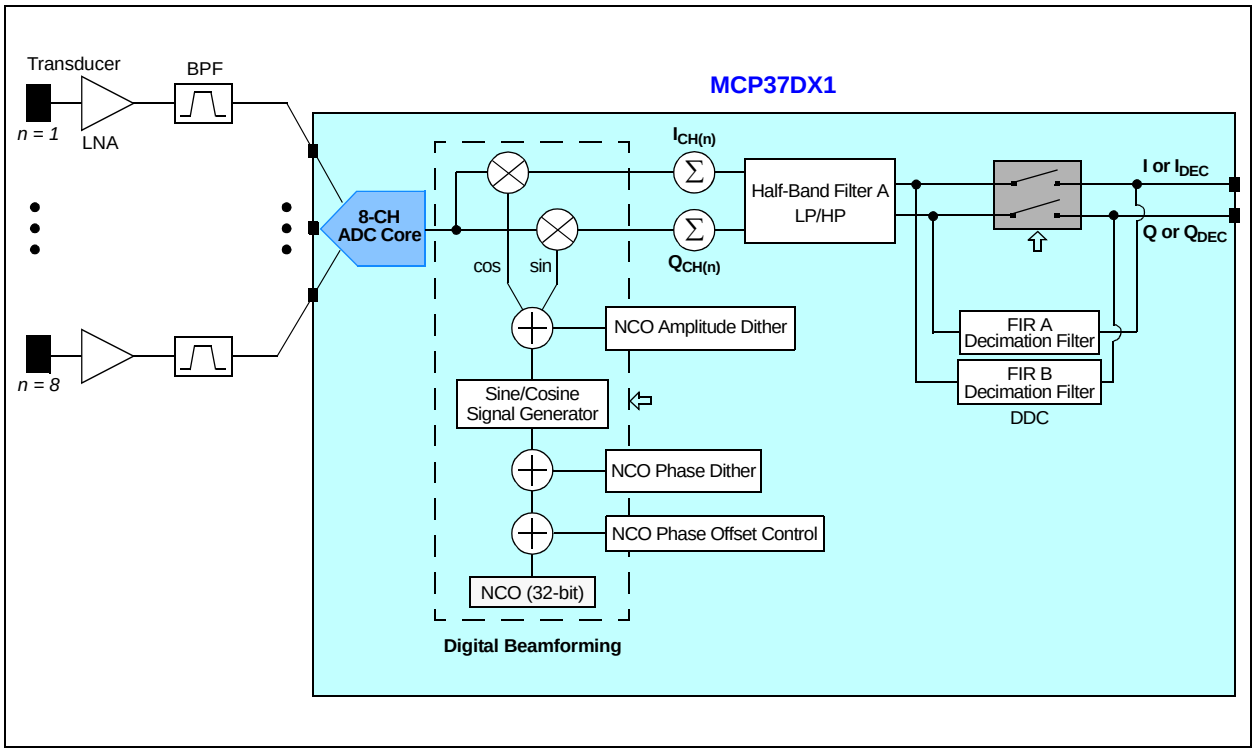

FIGURE 9: *Sonar Receiver Block Diagram Utilizing the Beamforming Feature of the 8-Channel MCP37DX1.*

EXTERNAL TIME-INTERLEAVING FOR HIGHER SPEED DATA CONVERSIONS[1-3]

Figure 10 shows an example of achieving external timing-interleaving for higher data conversion. As an example, 800 Msps time-interleaved conversion can be achieved by using four 200 Msps devices. This configuration can be used for digital oscilloscope design. For 1 Gsps conversion, the user can operate the four ADCs with a 250 MHz clock with 90 degree phase difference.

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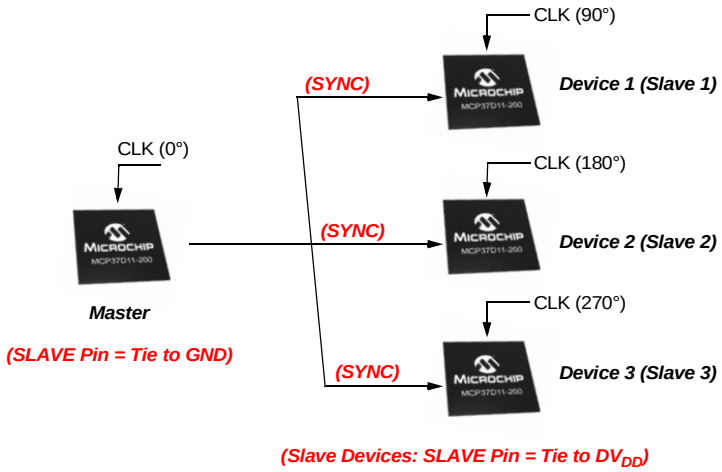
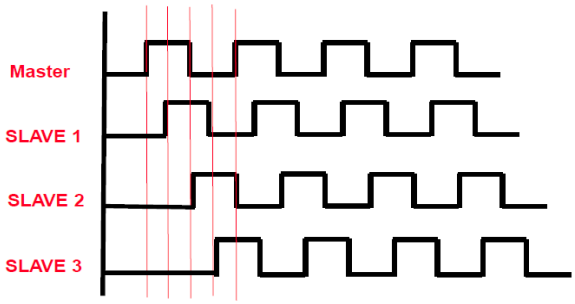


(a) External clock phase control in Auto-Sync mode.



(b) Clocks for each device.

Note: Each device samples input at the its own clock phase.

FIGURE 10: *Time-Interleaved Configuration for Higher Speed Data Conversion.*

POWER CONSUMPTION

In RF system design, meeting the system power budget is an important criteria, which is especially needed for portable applications, such as oscilloscopes and hand-held data acquisition devices. With advanced ADC design and manufacturing technology, the digitally enhanced high-speed ADC of today can be designed with very low-power consumption. The power consumption of this ADC core is about 490 mW for a 16-bit, 200 Msps device with LVDS output and 338 mW for a 12-bit, 200 Msps device with LVDS output[1-2]. Figure 11 shows the power consumption of a single channel 14-bit, 200 Msps device over input sampling rates[2].

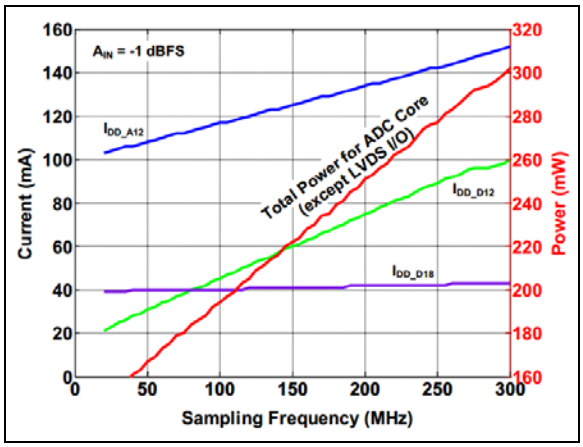


FIGURE 11: *Power Consumption vs. Sampling Frequency of the Digitally Enhanced ADC: Single Channel, 14-Bit Device*[2].

CONCLUSIONS

The built-in digital blocks in the MCP37DXX ADC can simplify modern digital receiver designs. Dynamically reconfigurable features improve the overall system performance and allow for improved system design flexibility. By utilizing the built-in digital features, the overall receiving system components can be reduced significantly, which allows miniaturization of the RF receiver. The low-power consumption of the digitally enhanced ADC offers an excellent solution for power-sensitive portable device designs. RF designers should take advantage of all these available options for their RF system designs.

REFERENCES

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[2] *"MCP37220-200/MCP37D20-200 Family Data Sheet"* (DS20005396), Microchip Technology Inc., 2015-2016.

[3] *"MCP37210-200/MCP37D10-200 Family Data Sheet"* (DS20005395), Microchip Technology Inc., 2015-2016.

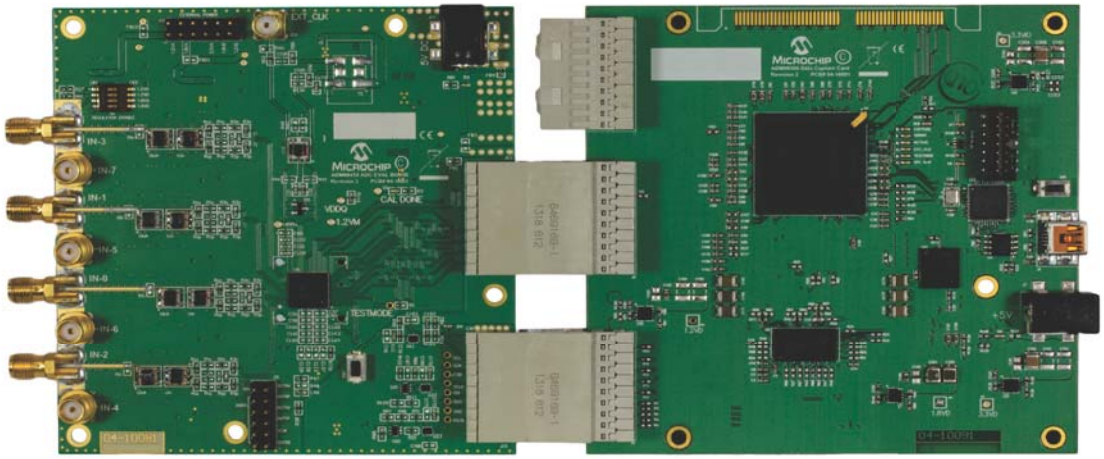
[4] Thomas Youbok Lee, Andrea Panigada, Dan Meacham, Trent Butcher, Toshikazu Ishida, *"Digitally Enhanced High Speed ADC for Low-Power Wireless Applications"*, IEEE MTT-S International Conference on Microwaves for Intelligent Mobility (ICMIM), Nagoya, Japan, March 20, 2017.

APPENDIX A: DEVELOPMENT SUPPORT

A.1 High-Speed ADC Evaluation Platform

Microchip offers a high-speed ADC evaluation platform which can be used to evaluate Microchip's high-speed ADC products. The platform consists of an MCP37XXX evaluation board, an FPGA-based data capture card board, and a PC-based Graphical User Interface (GUI) software for ADC configuration and evaluation.

Figure A-1 and Figure A-2 show the evaluation tools. This evaluation platform allows users to quickly evaluate the ADC module's performance for their specific application requirements. More information is available at http://www.microchip.com.



(a) MCP37XXX-200 Evaluation Board (b) Data Capture Board

FIGURE A-1: *MCP37XXX Evaluation Kit.*

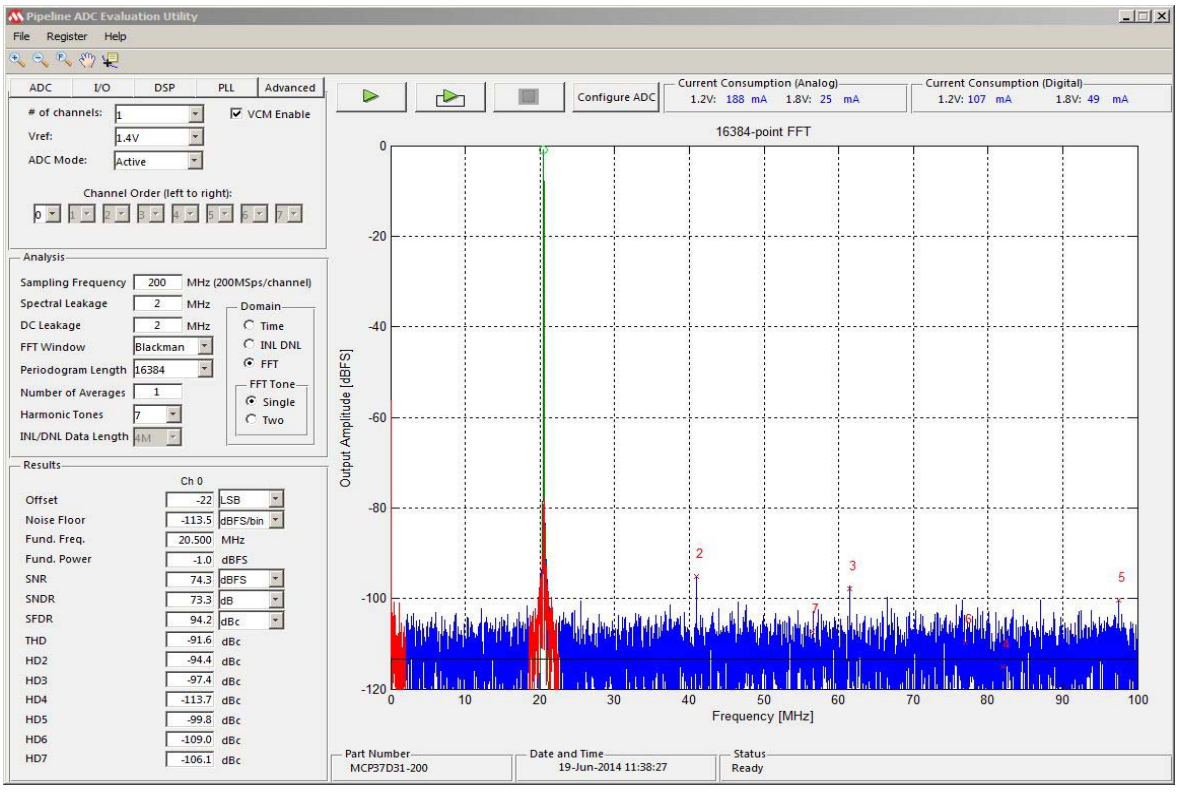


FIGURE A-2: *PC-Based Graphical User Interface (GUI) Software.*

NOTES:

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