

How to Use XDMAC on Cortex™-M7 Microcontrollers to Implement Ping-Pong Buffering in Audio Applications

Introduction

Audio system applications can pose typical producer-consumer problems associated with a real-time system. The timing constraints include latency, sampling rate, sampling period and real-time response. To implement a solution to the audio time challenges, an application typically uses the Ping-Pong data buffer method. The Ping-Pong method uses two buffers: one buffer reads data from the source and another buffer is submitting the data to the destination. When the submission to the destination is complete, the roles of the two buffers are switched. The Ping-Pong is accomplished by modifying the index (pointers) to the buffers.

The following figure represents a typical USB Audio headphone application implementation where the PC (acting as a USB host) streams audio data to the Cortex[™]-M7 microcontroller (MCU) based audio subsystem. The application updates *Buffer1* with streamed in audio data from the USB. The XDMAC sets up the transfer of audio data to the CODEC (through the SSC) by configuring the address of *Buffer1* as the source address, and the address of the SSC transmit register (SSC_THR) as the destination address. When the data transmission is completed, the XDMAC switches the source address to *Buffer2* (which would be updated by the latest streamed in audio data). When the *Buffer2* data transmission is completed, the XDMAC switches the source address to *Buffer1*, which can be updated by the latest streamed audio data. This process of the XDMAC switching the source address from *Buffer1* to *Buffer2* continues as the data is streamed in and updated in the buffers while transmitting the data from the buffers to the CODEC to realize the audio playback at the headphone.

Figure 1. USB Audio Headphone Application

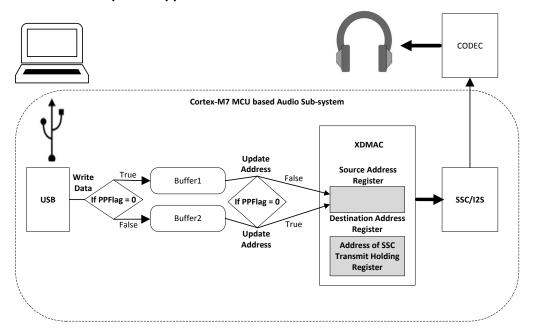


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1. Concept

The XDMAC peripheral provides support to implement the Ping-Pong buffering method through a multiple block data transfer feature. In multiple block data transfer, each block of data can be transferred with different configuration parameters such as, data source, destination address, data size, and trigger source. The XDMAC supports multiple block data transfer through the linked list. An implementation that uses a linked list feature requires the creation of linked list descriptors.

A linked list descriptor contains register settings to transfer a block of memory. When data is transferred using a linked list, the XDMAC fetches the first descriptor from the linked list, copies the register settings to channel registers, and performs the data transfer according to the configuration settings. When the first block transfer is completed, the XDMAC fetches the second descriptor from the linked list, copies the register settings to channel registers, and performs the data transfer according to the configuration settings. This process continues until the end of the linked list. Linked list descriptors are usually stored in internal data memory.

2. Solution

To implement Ping-Pong based audio data buffer handling in the USB Audio headphone application, build an XDMAC circular linked list consisting of two descriptors with the 'View 1' type. The 'View 1' type descriptor has four members, as shown in the following table.

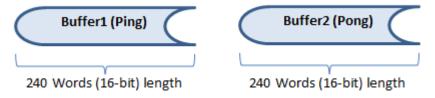
Table 2-1. View 1 Type Linked List Descriptor

MBF	Next Descriptor Address	
МВ	Source Address	
МВ	MBR_DA	
	UBLEN	Data length in microblocks
	NDE	Next Descriptor Enable
MBR_UBC (Microblock Control)	NSEN	Next Descriptor Source Update
	NDEN	Next Descriptor Source Update
	NVIEW	Next Descriptor View Type

Note: In this application, although the 'View 0' type descriptor is sufficient, the 'View 1' type descriptor is chosen to demonstrate the use case where one item of control configuration changes (NSEN enabled) from one block to other while another item remains the same (NDEN disabled).

The following figure is a representation of the application buffers used in the Ping-Pong implementation

Figure 2-1. Ping-Pong Audio Data Buffers

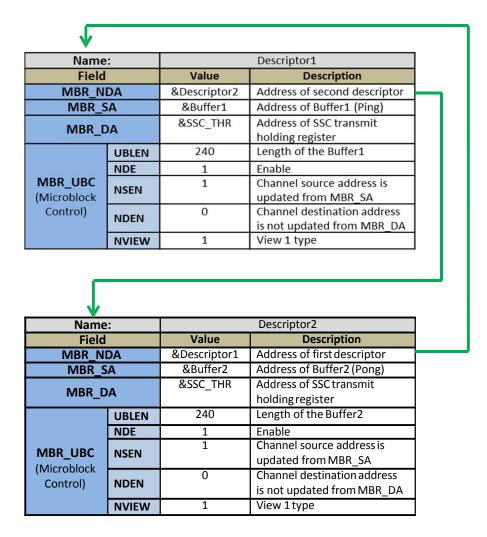


Note: The application buffers Buffer1 and Buffer2 are shared between the XDMAC and the USB.

- 1. Typically, the application maintains the exclusive access to these buffers through a global flag, such as PPFlag, shown in Figure 1.
- 2. If XDMAC is transmitting *Buffer1*, it is the responsibility of the application to ensure that the *Buffer2* is updated with data from USB before the completion of *Buffer1*.

The following figure shows the XDMAC circular linked list with two descriptors to implement the Ping-Pong buffering.

Figure 2-2. Circular Linked List



- 1. The next descriptor fields (NDA, NDE, NSEN, NDEN and NVIEW) control the transfer behavior of the next descriptor, not the current descriptor.
 - Descriptor1 controls the transfer behavior when the first descriptor is completed and the transfer of the second descriptor is to start
 - Descriptor2 controls the transfer behavior when the second descriptor is completed and the transfer of the first descriptor is to start
- 2. The NSEN field in both of the linked list descriptors above is set as '1' to enable updates of the channel-specific source address register (XDMAC_CSAx) with the value in the MBR_SA field. This is because at the end of a block transfer, the XDMAC_CSAx would have an invalid address for the next transaction. MBR_SA contains the address of the buffer, which would be the next buffer made ready for transfer.
 - After the end of transmission of Descriptor1, XDMAC_CSAx is updated to contain the address of Buffer2 (pong) from Buffer1 (ping).
 - After the end of transmission of Descriptor2, XDMAC_CSAx is updated to contain the address of Buffer1 (ping) from Buffer2 (pong).

- 3. The NDEN field in both the linked list descriptors above is set as '0' to disable updates of the channel-specific destination address register (XDMAC_CDAx) with the value in the MBR_DA field. This is because at the end of a block transfer, the XDMAC_CDAx would still have a valid address for the next transaction.
 - After the end of transmission of Descriptor1, XDMAC_CDAx contains the address of SSC transmit holding register (SSC_THR) and subsequently is not updated.
 - After the end of transmission of Descriptor2, XDMAC_CDAx contains the address of SSC transmit holding register (SSC_THR) and subsequently is not updated.
- 4. To start the data transfer, enable the implemented linked list by directly writing to the channel specific next descriptor control (XDMAC_CNDCx) and address (XDMAC_CNDAx) registers with the values of the first descriptor (NDA, NDE, NSEN, NDEN and NVIEW).

The following figure shows example code to create the circular linked list.

Figure 2-3. Create Circular Linked List

```
typedef struct {
    /** Next Descriptor Address number. */
    uint32 t mbr nda;
   /** Microblock Control Member. */
    uint32 t mbr ubc;
    /** Source Address Member. */
    uint32 t mbr sa;
    /** Destination Address Member. */
    uint32 t mbr da;
} lld_view1;
/** Bits per slot */
#define BITS BY SLOT
                                 (16)
/** Total number of buffers */
#define TOTAL BUFFERS
                                 2
/** Length of a buffer */
#define MAX DMA SIZE
                                 240
/** XDMA Descriptor */
static lld_view1 linklist_write[TOTAL_BUFFERS];
/** Audio Buffer */
static uint16 t Buffer[TOTAL BUFFERS][MAX DMA SIZE*(BITS BY SLOT / 8)];
  for(i = 0; i < TOTAL_BUFFERS; i++)</pre>
      linklist write[i].mbr ubc = XDMAC UBC NVIEW NDV1
                                   XDMAC UBC NDE FETCH EN
                                   XDMAC UBC NSEN UPDATED
                                   XDMAC UBC NDEN UNCHANGED
                                   XDMAC CUBC UBLEN(MAX DMA SIZE);
      linklist_write[i].mbr_sa = (uint32_t)(&Buffer[i]);
      linklist_write[i].mbr_da = (uint32_t)&(SSC->SSC_THR);
      if ( i == (TOTAL_BUFFERS - 1 ))
          linklist_write[i].mbr_nda = (uint32_t)&linklist_write[0];
      else
      {
          linklist_write[i].mbr_nda = (uint32_t)&linklist_write[i+1];
      }
  }
```

After initializing the linked list as previously described, and once the corresponding XDMAC channel is enabled, the XDMAC places the contents of *Buffer1* onto the SSC transmit register (SSC_THR) according to the configuration parameters. When the *Buffer1* transmission is completed, the XDMAC switches to *Descriptor2* in the linked list. The source address of the audio data in *Descriptor2* points to *Buffer2*. Once transmission completes, as with earlier descriptor, the XDMAC moves back to the *Descriptor1* in the list. The XDMAC switches between the two descriptors (implicitly between the two Ping-Pong audio buffers *Buffer1* and *Buffer2*) while transmitting the audio data through the SSC to the CODEC.

3. Relevant Resources

- Usage of XDMAC on SAM S/SAM E/SAM V
 http://www.atmel.com/Images/Atmel-42761-Usage-of-XDMAC-on-SAMS-SAME-SAMV ApplicationNote AT17417.pdf
- Synchronous Serial Controller (SSC) of SAMV71 Devices to Output an Audio Stream Through the On-board WM8904 CODEC http://asf.atmel.com/docs/latest/ sam.components.audio.codec.wm8904.example.samv71_xplained_ultra/html/index.html
- Synchronous Serial Controller (SSC) of SAM3S Devices to Output an Audio Stream Through the On-board WM8731 CODEC
 - http://asf.atmel.com/docs/latest/sam.components.audio.codec.wm8731.example.sam3x_ek/html/index.html

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