AN4885

Interfacing PCI1xxx with RS-232, RS-422 and RS-485 Through UART

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1.0 INTRODUCTION

This application note describes interfacing UART with RS-232, RS-422 and RS-485. It gives considerations for interfacing these standards with PCI1xxxx. This document describes the typical UART data frame as well as UART hardware and software flow control.

1.1 Sections

This document includes the following topics:

Section 2.0, "Executive Summary"

Section 3.0, "UART"

Section 4.0, "Signals"

Section 5.0, "Interfacing with PCI1xxx"

Section 6.0, "RS-232"

Section 7.0, "RS-422"

Section 8.0, "RS-485"

1.2 References

Consult the following references for details on the specific parts referred to in this document:

- TIA/EIA 232F
- TIA/EIA 422B
- TIA/EIA 485A
- ITU-T V.24
- TSB-89A

1.3 Terms and Abbreviations

This following terms and abbreviations are used in this document:

TABLE 1: TERMS AND ABBREVIATIONS

Term/Abbreviation	Definition
Baud rate	Symbols sent per second
Bit rate	Number of bits sent in a second
Bit time	The time required to send one bit. This is the inverse of bit rate.
BPS	Bits Per Second
CTS	Clear to Send
DCE	Data Circuit-Terminating Equipment
Differential signal	A pair of signals with opposite magnitude that when subtracted from each other contains the original logic signal

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TABLE 1: TERMS AND ABBREVIATIONS (CONTINUED)

Term/Abbreviation	Definition
DTE	Data Termination Equipment
EIA	Electronic Industries Alliance
FIFO	First In First Out
Generator	Device responsible for transmitting data on a bus
ITU	International Telecommunication Union
Marking	Binary 1 or logical high
NRZ	Non Return to Zero
Receiver	Device responsible for reading data on a bus
RTS	Ready to Send
Space	Binary 0 or logical low
TIA	Telecommunications Industry Association
Transmitter	Different name for a generator
UART	Universal Asynchronous Receiver-Transmitter

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2.0 EXECUTIVE SUMMARY

When working with PCI1xxxx, take note of the following important guidelines:

- UART
  - The receiver and transmitter must be configured beforehand to use the same transmission speed and data frame.
  - The longer the interconnecting medium, the lower the maximum transmission rate is.
  - Faster speed signals require balancing the cable. This involves adding a resistor matching the characteristic impedance of the cable on the terminating end of the cable.
- Flow control
  - Flow control can be implemented in hardware or software. The receiver and transmitter must be configured to utilize or respond to appropriate flow control signals or messages.
  - All flow control signals are optional.
  - RTS and CTS are commonly used. Most others are rarely used.
- PCI1xxxx
  - Each SKU supports up to four instances of UART. These can be assigned to specific pins (see details in Section 5.0, "Interfacing with PCI1xxx").
  - Not all PCI1xxxx SKUs have UARTs enabled by default. UARTs can be enabled or disabled through EEPROM configuration. See Section 5.1, "Per SKU Default" for details.
  - TX, RX, CTS and RTS all have functions that can be assigned to pins. Most other flow control signals do not.
- RS-232
  - RS-232 uses single-ended signaling, meaning one wire per signal.
  - RS-232 has standardized pinouts for DB25/26 and DB9 connectors. Not all pins are used in these pinouts.
  - RS-232 supports point-to-point connections.
- RS-422/RS-485
  - RS-422 and RS-485 have different voltage thresholds.
  - RS-422 and RS-485 have different supported bus architectures.
  - RS-422 and RS-485 are intercompatible within voltage and bus limitations.
  - RS-422 and RS-485 do not have standardized connector pinouts. Each manufacturer defines their own pinout.

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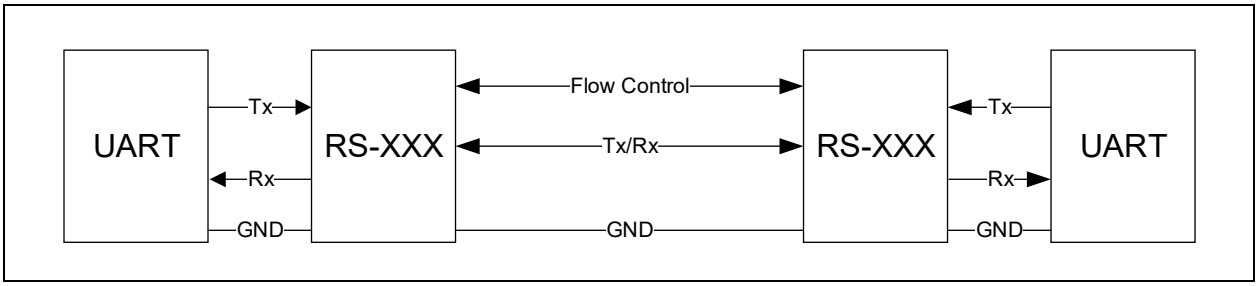
3.0 UART

A UART typically consists of a shift register for transmitting, a shift register for receiving, a clock generator and a FIFO buffer. The various interfaces are located between the local UART and the transmit/receive lines.

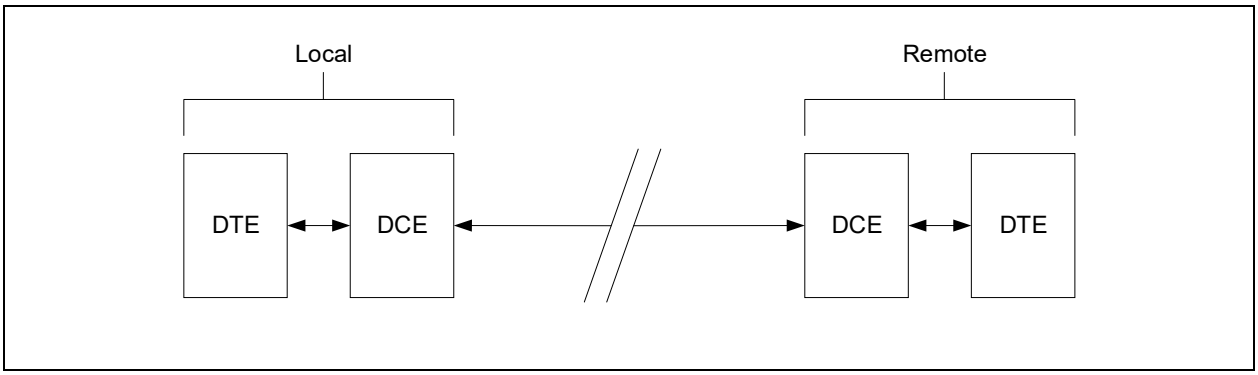
The general considerations common to all the interfaces are discussed in this section, and interface-specific considerations are discussed in their corresponding sections.

FIGURE 1: INTERFACING UART WITH RS-XXX



UART has two signals: Tx and Rx. There is no separate clock signal. The UART transmits and reads at an assumed bit rate (baud). In general, a UART can be part of a data terminal equipment (DTE) or a data circuit-terminating equipment (DCE). A DTE is assumed to be the controlling piece of hardware (such as a computer), and the DCE is assumed to be the receiving piece of hardware (such as a modem or terminal).

FIGURE 2: COMMUNICATION BETWEEN DTE AND DCE



A quick comparison of the different standards is listed in Table 2. RS-232, RS-422 and RS-485 do not define a maximum cable length, but the length of cable and the baud rate share an inverse relationship (that is, the longer the cable, the slower the baud rate).

TABLE 2: COMPARISON OF DIFFERENT STANDARDS

Standard	Operating Voltage	Number of Wires	Differential/Single Ended
RS-232	±12V	3/9/25	Single Ended
RS-422	±10V	5/9	Differential
RS-485	–7V to +12V	5/9	Differential

3.1 UART Data Frame

The typical UART data frame consists of a start bit, five to nine data bits, an optional parity bit and a stop bit. When idle, UART holds the Tx line high.

- Start bit: To begin transmitting, the UART pulls the Tx line low for exactly one bit time. This signals to the receiver that data is to follow. Data is transmitted immediately after the Start bit.
- Data bits: The actual data to be transmitted, with the least significant bit (lsb) transmitted first.

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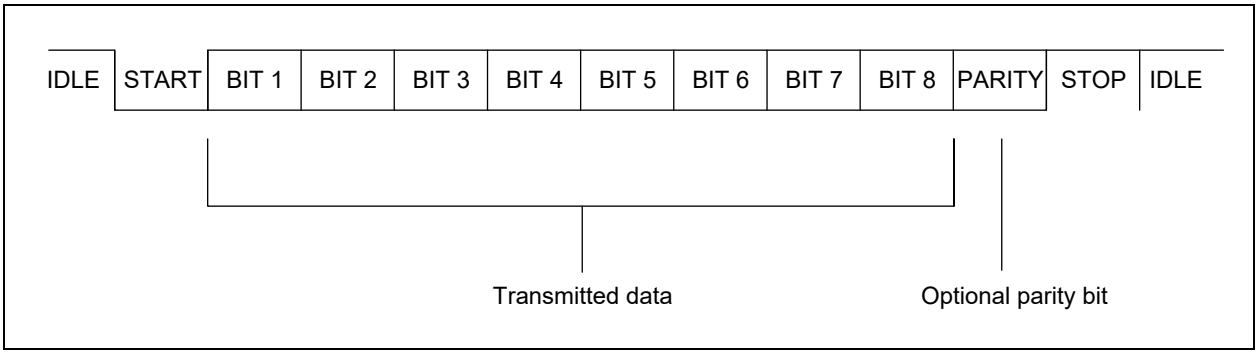
- Parity bit: The parity bit is calculated by the transmitter and is a simple way to error check the received data. Parity can either be even, odd, mark or space.
  - In even parity, the number of 1s in the transmitted data must always be even. This means that if the data itself has an odd number of 1s, the parity bit will be a 1, and if the data itself has an even number of 1s, the parity bit will be 0.
  - In odd parity, the number of 1s in the transmitted data must always be odd. This means that if the data itself has an even number of 1s, the parity bit will be a 1, and if the data itself has an odd number of 1s, the parity bit will be 0.
  - In mark parity, the parity bit is always a 1.
  - In space parity, the parity bit is always a 0.
- Stop bit: The Tx line is held high for one or more bit times after the parity bit.

UART typically uses a Non Return to Zero (NRZ) data encoding. This scheme uses a voltage threshold for logical high and a voltage threshold for logical low. The signal does not return to a neutral state; it only changes when a bit changes.

The exact structure of the data frame can vary, so both the receiver and the transmitter must be configured to use the same data frame. Additionally, since there is no transmitted clock, both the receiver and the transmitter must be configured to use the same baud rate before any communication occurs.

FIGURE 3: UART DATA FRAME

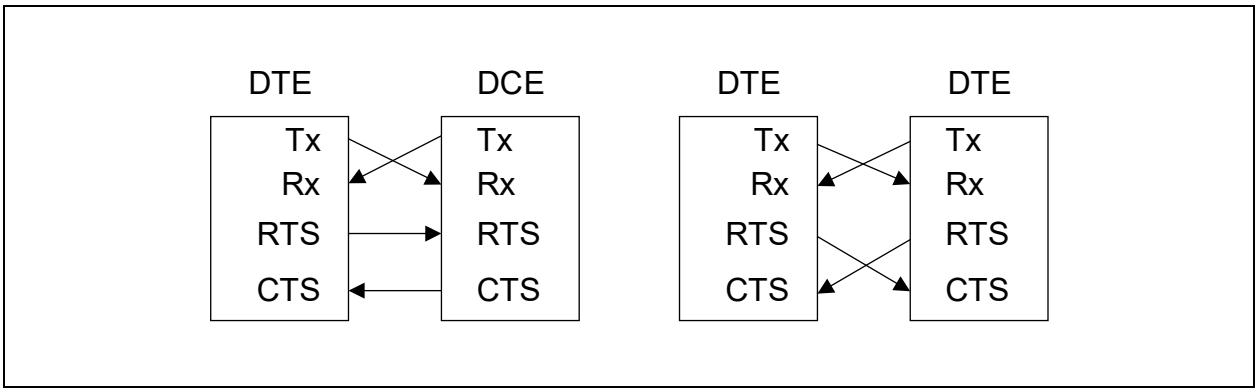


3.2 UART Flow Control

Flow control is used to limit data transfer in order to avoid a buffer overflow problem. There are two main types of flow control: hardware and software.

Hardware flow control is implemented with clear to send (CTS) and ready to send (RTS) signals. The exact connection of these signals depends on the devices being connected, as illustrated in Figure 4.

FIGURE 4: CONNECTING A DTE AND DCE



The DTE acts as the controller. In the case of both devices being a DTE, either can act as the controller.

- *Transmitting Data:* The transmitter first signals to the receiver that it has data to transmit by asserting RTS. It then waits for the receiver to assert CTS. Once both RTS and CTS are asserted, the transmitter begins sending data.

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The transmitter sends one bit at a time starting with the lsb. Once the transmitter is finished, it sends a stop signal and deasserts RTS. The transmitter pauses transmission any time the receiver deasserts CTS.

- *Receiving Data:* When the receiver detects that the transmitter has asserted the RTS signal, it responds by asserting the CTS signal. After the receiver detects a start bit, it starts reading the line for the incoming data. It stores this data in a shift register. Once the shift register is full, it pushes the data into a FIFO register. The system that the receiver is attached to is then responsible for clearing the FIFO register. If the FIFO and shift register are full, the receiver can deassert CTS to allow its system time to read the registers and avoid losing data.
- *Software Flow Control:* The receiver can also send commands to start and stop data transmission through its Tx line. When the receiver transmits an XON byte, the transmitter proceeds to transfer data. When the receiver transmits an XOFF byte, the receiver stops transmitting data. The primary advantage of software flow control is that it requires fewer electrical lines than hardware flow control does. The disadvantage is that there is a potential to lose data while the receiver is transmitting an XOFF byte.

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4.0 SIGNALS

The following signals are defined in ITU-T Rec. V.24 and TIA-232f. At a minimum, a UART connection requires a Tx line, an Rx line and a common ground. If flow control is implemented, RTS and CTS are additionally needed. The rest of the signals are not commonly implemented.

- *Shield:* This is typically connected to ground.
- *Transmitted Data:* This is data sent out from the DTE. This can be transmitted data or software flow control bytes. Both RTS and CTS must be asserted before data can be transmitted.
- *Received Data:* This is data received into the DTE. This can be data or software flow control bytes.
- *Request To Send:* This is a signal controlled by the DTE. When asserted, this lets the DCE know that the DTE is ready to transmit data.
- *Ready For Receiving:* This is a signal controlled by the DTE. When asserted, this lets the DCE know that the DTE is ready to receive data.
- *Clear To Send/Ready for Sending:* This is a signal controlled by the DCE. When asserted, this lets the DTE know that the DCE is ready to receive transmitted data.
- *DCE Ready/Data Set Ready:* This indicates that the DCE is ready to operate. This signal is used in conjunction with Test mode and CTS to indicate to the DTE what signals the DCE is expecting. These states are listed in Table 3.

TABLE 3: DATA SET READY DECODE

Test Mode and CTS State	DSR Asserted	DSR Deasserted
Test Indicator Asserted	DCE is connected and ready to exchange control signals for testing.	—
Test Indicator Deasserted	DCE is connected and ready to exchange control signals.	—
Ready For Sending Asserted	—	DCE is ready to exchange data signals for controlling DCE
Ready For Sending Deasserted	—	DCE is in a disconnected or fault condition.

- *Signal Common:* This is the common ground between the DTE and DCE.
- *Received Line Signal Detector/Data Channel Received Line Signal Detector:* This is the signal controlled by the DCE. When asserted, this indicates the received signals from the DTE are within the DCE-manufacturer-defined limits. When this line is deasserted, the signal is outside of those limits.
- *Secondary Received Line Signal Detector/Backward Channel Received Line Signal Detector:* The functionally is equivalent to Received Line Signal Detector, but with respect to the secondary Received Data.
- *Data Signal Rate Selector (DCE Source):* This is a signal controlled by the DCE. When the DTE supports multiple signaling rates, this signal is used to indicate which to use. When this signal is asserted, the higher signaling rate is used.
- *Data Signal Rate Selector (DTE Source):* This is a signal controlled by the DTE. When the DCE supports multiple signaling rates, this signal is used to indicate which to use. When this signal is asserted, the higher signaling rate is used.
- *Secondary Clear To Send/Backward Channel Ready:* The functionally is equivalent to CTS, but with respect to the Secondary Received Data.
- *Secondary Transmitted Data:* The functionally is equivalent to Transmitted Data, but with respect to a secondary channel.
- *Transmitter Signal Element Timing (DCE Source):* This is a transmitter-specific clock signal provided by the DCE. When the transmitter requires variable timing, the frequency of this signal should be changed in the off state.
- *Transmitter Signal Element Timing (DTE Source):* This is a transmitter-specific clock signal provided by the DTE.
- *Secondary Received Data:* The functionally is equivalent to Received Data.
- *Receiver Signal Element Timing (DCE Source):* This is a receiver-specific clock signal provided by the DCE. When the receiver requires variable timing, the frequency of this signal should be changed in the off state.

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- *Local Loopback:* Controlled by the DTE, this signal indicates to the local DCE that it should transmit any data it receives from the DTE back to the DTE.
- *Secondary Request To Send:* The functionally is equivalent to RTS, but with respect to the Secondary Transmitted Data.
- *DTE Ready/Connect Data Set to Line/Data Terminal Ready:* This is a signal controlled by the DTE. When asserted, this tells the DCE that the DTE wants to place a call and the DCE opens a communication channel. When deasserted, this tells the DCE to close the communication channel. The DCE can hold the communication open or closed as needed.
- *Remote Loopback:* Controlled by the DTE, this signal indicates to the remote DCE that it should transmit any data it receives from the DTE back to the DTE.
- *Ring Indicator/Calling Indicator:* This is a signal controlled by the DCE. When asserted, the DCE is receiving a call.
- *Received Energy Present:* This is a signal controlled by the DCE. This indicates presence of energy on the line.
- *Test Mode/Test Indicator:* This is a signal controlled by the DCE. When asserted, this puts the DTE into Test mode. This is used in conjunction with DSR to determine what to do.

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5.0 INTERFACING WITH PCI1XXX

The PCI1xxx series all utilize **prog#** pins that are multiplexed to a number of different functions. A configurable EEPROM or an internal OTP memory allows these pins to be set to the desired function upon startup. Refer to the data sheet for the pinout.

5.1 Per SKU Default

Table 4 lists how many UARTs are assigned to **prog#** pins by default per SKU. All SKUs support up to four UARTs, but not all SKUs have default **prog#** pins assigned to UART. UARTs can be assigned to **prog#** pins through EEPROM configuration. The following sections detail which **prog#** pins can be assigned for a given UART function.

TABLE 4: PCI1XXX UART OPTIONS

SKU	Default Number of UARTS
PCI12000	0
PCI11010	0
PCI11101	1
PCI11400	0
PCI11414	4

5.2 PCI12000

The PCI12000 does not have any default pins assigned to UART. Table 5 lists the **prog#** pins that can be assigned to the various UART functions.

TABLE 5: PCI12000 PIN MULTIPLEXING

UART	Function	Default Prog#	Alternate Prog#s
UART0	TXD	—	29, 69, 70, 71
	RXD	—	30, 70, 71, 72
	RTS_N	—	31, 64, 72, 75, 81, 83
	CTS_N	—	32, 65, 71, 76, 82
	DTR_N	—	31, 64, 75, 81, 83
	DSR_N	—	29, 32, 65, 76, 82
	DCD_N	—	30
	RI_N	—	31
	WAKE_N	—	31, 68, 69, 75, 78, 85
UART1	TXD	—	31, 69, 77
	RXD	—	32, 70, 78
	RTS_N	—	33, 72, 81
	CTS_N	—	30, 71, 82
	DTR_N	—	33, 71, 81
	DSR_N	—	72, 82
	DCD_N	—	—
	RI_N	—	—
	WAKE_N	—	29, 32, 68, 69, 70, 73, 83, 86

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TABLE 5: PCI12000 PIN MULTIPLEXING (CONTINUED)

UART	Function	Default Prog#	Alternate Prog#s
UART2	TXD	—	64
	RXD	—	65
	RTS_N	—	31
	CTS_N	—	32
	DTR_N	—	31
	DSR_N	—	32
	DCD_N	—	33, 85, 86
	RI_N	—	87
	WAKE_N	—	71, 79, 80, 87
UART3	TXD	—	66
	RXD	—	67
	RTS_N	—	—
	CTS_N	—	—
	DTR_N	—	—
	DSR_N	—	—
	DCD_N	—	85, 86
	RI_N	—	87
	WAKE_N	—	65, 79, 80

5.3 PCI11010

The PCI11010 does not have any default pins assigned to UART. Table 6 lists the **prog#** pins that can be assigned to the various UART functions.

TABLE 6: PCI11010 PIN MULTIPLEXING

UART	Function	Default Prog#	Alternate Prog#s
UART0	TXD	—	3, 17, 29, 69, 70, 71
	RXD	—	18, 30, 70, 71
	RTS_N	—	17, 31, 64, 75, 81, 83
	CTS_N	—	18, 32, 65, 71, 76, 82
	DTR_N	—	17, 31, 64, 75, 81, 83
	DSR_N	—	17, 18, 29, 32, 65, 76, 82
	DCD_N	—	18, 30
	RI_N	—	31
	WAKE_N	—	31, 68, 69, 75, 78
UART1	TXD	—	31, 69, 77, 81
	RXD	—	32, 70, 78, 82
	RTS_N	—	33, 81
	CTS_N	—	30, 71, 82
	DTR_N	—	33, 46, 71, 81
	DSR_N	—	47, 82
	DCD_N	—	48
	RI_N	—	49
	WAKE_N	—	29, 32, 50, 68, 69, 70, 73, 83

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TABLE 6: PCI11010 PIN MULTIPLEXING (CONTINUED)

UART	Function	Default Prog#	Alternate Prog#s
UART2	TXD	—	17, 64, 86
	RXD	—	18, 65, 87
	RTS_N	—	31, 46
	CTS_N	—	32, 47
	DTR_N	—	31, 46
	DSR_N	—	32, 47
	DCD_N	—	0, 1, 33, 60, 61
	RI_N	—	2, 62, 63
	WAKE_N	—	64, 71, 79, 80
UART3	TXD	—	66
	RXD	—	67
	RTS_N	—	48
	CTS_N	—	49
	DTR_N	—	53, 48
	DSR_N	—	49
	DCD_N	—	0, 1, 60, 61
	RI_N	—	2, 62, 63
	WAKE_N	—	65, 79, 80

5.4 PCI11101

The PCI11101 has UART0 assigned to **prog#** pins by default. Table 7 lists these defaults as well as the alternate **prog#** pins.

TABLE 7: PCI11101 PIN MULTIPLEXING

UART	Function	Default Prog#	Alternate Prog#s
UART0	TXD	69	4, 17, 29, 70, 71
	RXD	70	4, 18, 30, 71, 72
	RTS_N	72	5, 17, 19, 31, 64, 75, 81, 83
	CTS_N	71	6, 18, 20, 32, 65, 76, 82
	DTR_N	—	17, 19, 21, 31, 64, 75, 81, 83
	DSR_N	—	17, 18, 20, 29, 32, 65, 76, 82
	DCD_N	—	18, 30
	RI_N	—	19, 31
	WAKE_N	—	6, 20, 31, 68, 69, 75, 78
UART1	TXD	—	5, 31, 69, 77, 81
	RXD	—	6, 32, 70, 78, 82
	RTS_N	—	19, 33, 72, 81
	CTS_N	—	20, 30, 34, 71, 82
	DTR_N	—	19, 33, 46, 71, 81
	DSR_N	—	20, 34, 47, 72, 82
	DCD_N	—	48
	RI_N	—	49
	WAKE_N	—	29, 32, 50, 68, 69, 70, 73, 83

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TABLE 7: PCI11101 PIN MULTIPLEXING (CONTINUED)

UART	Function	Default Prog#	Alternate Prog#s
UART2	TXD	—	17, 64
	RXD	—	18, 65
	RTS_N	—	21, 31, 46
	CTS_N	—	32, 47
	DTR_N	—	21, 31, 46
	DSR_N	—	32, 47
	DCD_N	—	0, 1, 33, 60, 61
	RI_N	—	2, 34, 62, 63
	WAKE_N	—	64, 71, 79, 80
UART3	TXD	—	19, 66
	RXD	—	20, 67
	RTS_N	—	48
	CTS_N	—	49
	DTR_N	—	53, 48
	DSR_N	—	49
	DCD_N	—	0, 1, 34, 60, 61
	RI_N	—	2, 34, 62, 63
	WAKE_N	—	65, 79, 80

5.5 PCI11400

The PCI11400 does not have any default pins assigned to UART. Table 8 lists the **prog#** pins that can be assigned to the various UART functions.

TABLE 8: PCI11400 PIN MULTIPLEXING

UART	Function	Default Prog#	Alternate Prog#s
UART0	TXD	—	3, 4, 17, 29, 69, 70, 71
	RXD	—	4, 18, 30, 70, 71
	RTS_N	—	5, 17, 19, 31, 64, 75, 81
	CTS_N	—	6, 18, 20, 32, 65, 71, 76, 82
	DTR_N	—	7, 17, 19, 31, 64, 75, 81
	DSR_N	—	17, 18, 20, 29, 32, 65, 76, 82
	DCD_N	—	18, 30
	RI_N	—	19, 31
	WAKE_N	—	20, 31, 68, 69, 75, 78
UART1	TXD	—	5, 31, 69, 77, 81
	RXD	—	6, 32, 70, 78, 82
	RTS_N	—	19, 33, 81
	CTS_N	—	20, 30, 34, 71, 82
	DTR_N	—	19, 33, 46, 71, 81
	DSR_N	—	20, 34, 47, 82
	DCD_N	—	48
	RI_N	—	49
	WAKE_N	—	29, 32, 68, 69, 70

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TABLE 8: PCI11400 PIN MULTIPLEXING (CONTINUED)

UART	Function	Default Prog#	Alternate Prog#s
UART2	TXD	—	7, 17, 64
	RXD	—	18, 65
	RTS_N	—	31, 46
	CTS_N	—	32, 47
	DTR_N	—	31, 46
	DSR_N	—	32, 47
	DCD_N	—	0, 1, 33
	RI_N	—	2, 34, 87
	WAKE_N	—	64, 71, 79, 80
UART3	TXD	—	19, 66
	RXD	—	20, 67
	RTS_N	—	48
	CTS_N	—	49
	DTR_N	—	48
	DSR_N	—	49
	DCD_N	—	0, 1, 34
	RI_N	—	2, 34
	WAKE_N	—	65, 79, 80

5.6 PCI11414

The PCI11101 has all four UARTs assigned to **prog#** pins by default. Table 9 lists these defaults as well as the alternate **prog#** pins.

TABLE 9: PCI11414 PIN MULTIPLEXING

UART	Function	Default Prog#	Alternate Prog#s
UART0	TXD	3	4, 17, 29, 69, 70, 71
	RXD	4	18, 30, 70, 71
	RTS_N	17	5, 19, 31, 64, 75, 81, 83
	CTS_N	18	6, 20, 32, 65, 71, 76, 82
	DTR_N	—	7, 17, 19, 21, 31, 64, 75, 81, 83
	DSR_N	—	8, 17, 18, 20, 29, 32, 65, 76, 82
	DCD_N	—	9, 18, 30
	RI_N	—	10, 19, 31
	WAKE_N	—	6, 20, 31, 68, 69, 75, 78, 85
UART1	TXD	5	31, 69, 77, 81, 86
	RXD	6	32, 70, 78, 82, 87
	RTS_N	19	33, 81
	CTS_N	20	30, 34, 71, 82
	DTR_N	—	19, 33, 46, 71, 81
	DSR_N	—	20, 34, 47, 82
	DCD_N	—	48
	RI_N	—	49
	WAKE_N	—	29, 32, 50, 68, 69, 70, 83, 86

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TABLE 9: PCI11414 PIN MULTIPLEXING (CONTINUED)

UART	Function	Default Prog#	Alternate Prog#s
UART2	TXD	7	17, 64, 86
	RXD	8	18, 65, 87
	RTS_N	21	31, 46
	CTS_N	22	32, 47
	DTR_N	—	21, 31, 46
	DSR_N	—	22, 32, 47
	DCD_N	—	0, 1, 33, 60, 61, 85, 86
	RI_N	—	2, 34, 62, 63, 87
	WAKE_N	—	64, 71, 79, 80, 87
UART3	TXD	9	19, 66
	RXD	10	20, 67
	RTS_N	23	48
	CTS_N	24	49
	DTR_N	—	53, 48
	DSR_N	—	24, 49
	DCD_N	—	0, 1, 34, 60, 61, 85, 86
	RI_N	—	2, 34, 62, 63, 87
	WAKE_N	—	65, 79, 80

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6.0 RS-232

6.1 Pins

RS-232 has a standardized pinout for a DB9, DB25 or DB26 connector. The DB25 and DB26 connector pinouts are defined in TIA-232F. The 26th pin on a DB26 connector is unused, and the pinout is otherwise identical to a DB25 connector. The DB9 connector pinout is defined in TIA-574. Table 10 provides these pinouts from the perspective of the DTE.

TABLE 10: RS-232 PINS

Signal Name	DB25/26 Pin#	DB9 Pin#
Shield	1	—
Transmitted Data	2	3
Received Data	3	2
Request To Send	4	7
Ready For Receiving	4	—
Clear To Send	5	8
DCE Ready	6	6
Signal Common	7	5
Received Line Signal Detector	8	1
Secondary Received Line Signal Detector	12	—
Data Signal Rate Selector (DCE Source)	12	—
Secondary Clear To Send	13	—
Secondary Transmitted Data	14	—
Transmitter Signal Element Timing (DCE Source)	15	—
Secondary Received Data	16	—
Receiver Signal Element Timing (DCE Source)	17	—
Local Loopback	18	—
Secondary Request To Send	19	—
DTE Ready	20	4
Remote Loopback	21	—
Signal Quality Detector	21	—
Ring Indicator	22	9
Received Energy Present	22	—
Data Signal Rate Selector (DTE/DCE Source)	23	—
Transmit Signal Element Timing (DTE Source)	24	—
Test Mode	25	—

6.2 Electrical Characteristics

TIA-232F defines a voltage less than –3V as a marking state and a voltage greater than 3V as a spacing state. The range between ±3V is called the transition region and should be considered floating. The voltage measured between the common ground and the transmitter or receiver is not to exceed a magnitude of 25V.

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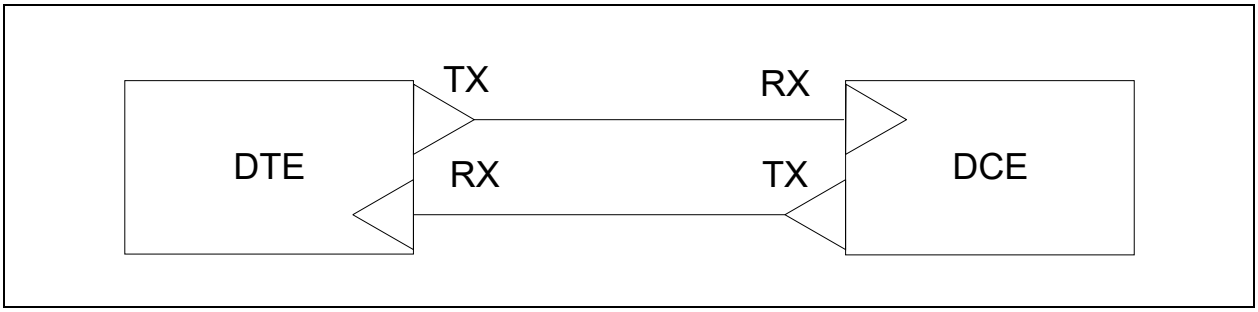
6.3 Bus Configurations

RS-232 uses a point-to-point bus architecture. This allows for one transmitter and one receiver on the bus at any given time. It is also assumed that a DTE connects to a DCE. While this topology worked well for connecting to modems, it requires one DTE for every device, which makes an inefficient standard in systems where communication between multiple devices is required. Figure 5 shows an example of a point-to-point connection.

FIGURE 5: POINT-TO-POINT BUS



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7.0 RS-422

7.1 Pins

There is no standardized connector pinout for RS-422. Each manufacturer has its own connector pinout. It is important to note that the signals used by RS-422 are differential, so there is a plus and minus for Tx and Rx.

7.2 Electrical Characteristics

TIA-422B defines a marking state to be when the voltage of terminal A is less than the voltage of terminal B. Likewise, a spacing state is when the voltage of terminal A is greater than the voltage of terminal B. The difference between the terminals should be at least 200 mV to allow for accurate interpretation at the receiver. The Common-mode voltage is the algebraic mean of the terminal voltages. In RS-422, the Common-mode voltage should be less than or equal to 7V in magnitude. RS-422 is compliant with voltages up to 10V in magnitude. Each terminal should dissipate no more than 3.25 mA.

RS-422 requires a balanced cable for signaling speeds greater than 200 kbit/s. This is to help minimize signal reflections in the cable. To balance a cable, a terminating resistor between 90Ω and 150Ω should be placed between the receiver terminals. Ideally, this resistor should be equal to the characteristic impedance of the interconnecting cable. Additionally, a capacitor can be placed in series with the resistor. The value for this capacitor should be such that the RC time constant is equal to the round trip delay of the cable. A capacitor decreases the maximum speed of the cable but also decreases the power draw of the cable.

TIA-422B was designed with transfer speeds up to 10 Mbit/s in mind. When it comes to distance, an addendum to the specification notes that it is possible to achieve distances of 1.2 km at speeds under 100 kbit/s. Baud rate and cable length share an inverse relationship (that is, the longer the cable, the slower the baud rate). When using a capacitor and resistor to balance a cable, the maximum recommended speed can be calculated with the following equation:

EQUATION 1: MAXIMUM RECOMMENDED SPEED

$$1/(10 * \text{Round trip delay})$$

Round trip delay can be calculated with the following equation:

EQUATION 2: ROUND TRIP DELAY

$$2 * \text{Cable length} * \text{Propagation delay of the cable}$$

Note: It is not recommended to use a cable length greater than 30 meters when using a terminating capacitor.

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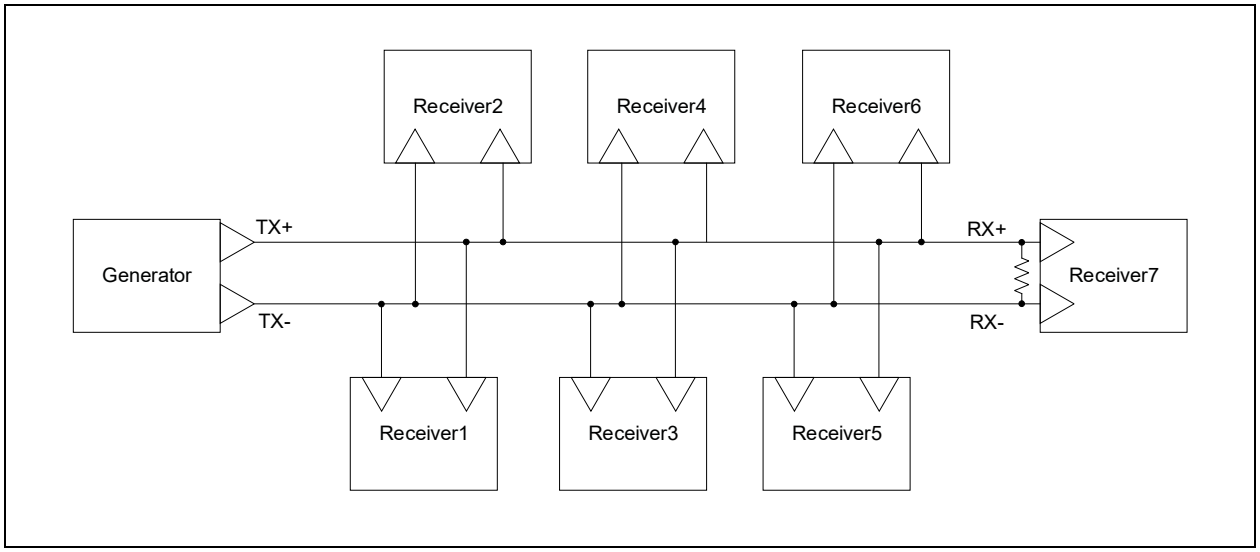
7.3 Bus Configurations

RS-422 uses a multi-drop bus configuration. This allows for one transmitter and multiple receivers. The electrical characteristics of the interconnecting media and the stub lengths limit the number of receivers that can be on this bus. In general, up to 10 receivers can be connected to a single RS-422 bus. Figure 6 shows an example of a multi-drop bus with a generator, seven receivers and a terminating resistor.

FIGURE 6: MULTI-DROP BUS



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8.0 RS-485

Based on RS-422, RS-485 allows for half-duplex communication and has lower voltage maximums. RS-485 is electrically compatible with RS-422 and controllers can be designed to communicate with each other.

8.1 Pins

There is no standardized connector pinout for RS-485. Each manufacturer has its own connector pinout. It is important to note that the signals used by RS-485 are differential, so there is a plus and minus for Tx and Rx.

8.2 Electrical Characteristics

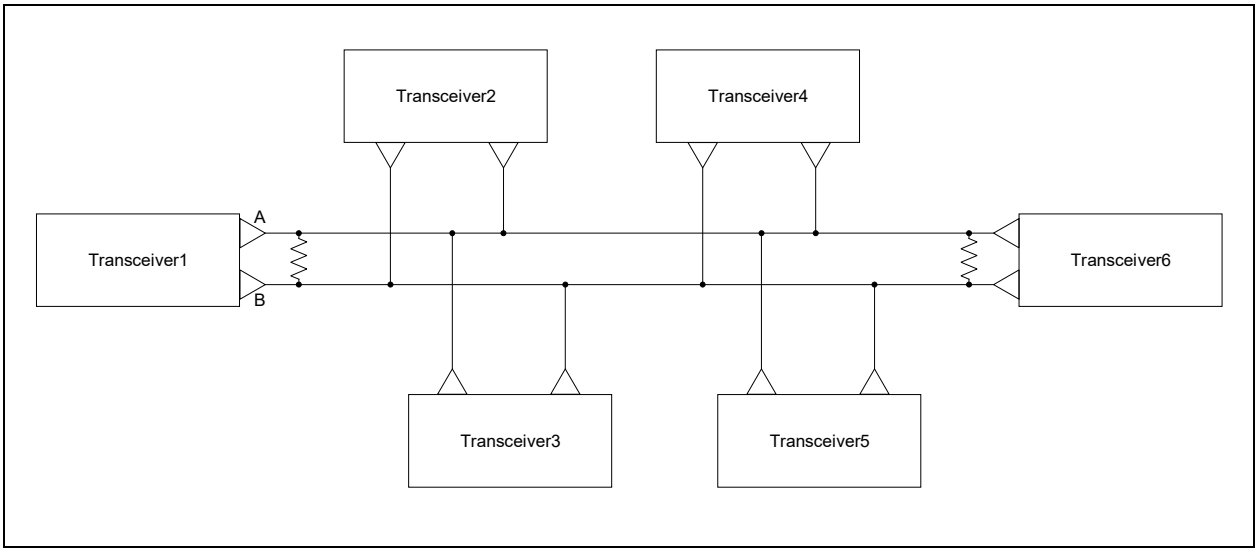
TIA-485A defines a binary ‘1’ as the voltage on terminal A being less than terminal B. Likewise, a binary ‘0’ is when the voltage on terminal A is greater than the voltage on terminal B. Each terminal can have signals ranging from –7V to +12V. The differential voltage between terminals should be at least 200 mV and no more than 6V. The Common-mode voltage is defined as the algebraic mean of the terminal voltages. The Common-mode voltage can range between –6.9V and 11.9V. Each terminal should dissipate no more than 1 mA.

TIA-485A does not specify how to balance cables, other than a recommendation to use a 120Ω terminating resistor. Additionally, the maximum speed and cable are not specified. As with RS-422, speed and distance have an inverse relationship.

8.3 Bus Configurations

RS-485 supports the bus configurations available to RS-232 and RS-422 as well as a multi-point bus architecture. This allows for multiple transmitters and receivers to be connected to the same bus. RS-485 supports a maximum of 32 devices (receivers, transmitters or transceivers) connected to the same bus. The number of devices is limited by expected baud rate, electrical characteristics of the connecting media (including cable length), and any stub lengths. For more guidance on bus design considerations for RS-485, consult TSB-89-A. Figure 7 shows an example half-duplex multi-point bus.

FIGURE 7: MULTI-POINT BUS



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APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004885A (02-07-23)	Initial release	

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NOTES:

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