# SY58609U

## 4.25 Gbps Precision, CML 2:1 MUX with Internal Termination and Fail Safe Input

### Features

- Precision 400 mV CML 2:1 MUX
- Guaranteed AC Performance Over Temperature and Voltage:
  - DC-to >4.25 Gbps Throughput
  - <370 ps Propagation Delay (IN-to-Q)
  - <90 ps Rise/Fall Times
- Fail Safe Input
  - Prevents Outputs from Oscillating when Input is Invalid
- Unique, Patented MUX Input Isolation Design Minimizes Adjacent Channel Crosstalk
- Ultra-low Jitter Design
  - <1 $ps_{RMS}$ Cycle-to-Cycle Jitter
  - <10 $ps_{PP}$ Total Jitter
  - <1 $ps_{RMS}$ Random Jitter
  - <10 $ps_{PP}$ Deterministic Jitter
- High-speed CML Outputs
- 2.5V ±5% or 3.3V ±10% Power Supply Operation
- Industrial Temperature Range: –40°C to +85°C
- Available in 16-lead 3 mm × 3 mm VQFN Package

### Applications

- Data Distribution: OC-48, OC-48+FEC, XAUI
- SONET Clock and Data Distribution
- Fibre Channel Clock and Data Distribution
- Gigabit Ethernet Clock and Data Distribution

### Markets

- Storage
- ATE
- Test and Measurement
- Enterprise Networking Equipment
- High-end Servers
- Access

### General Description

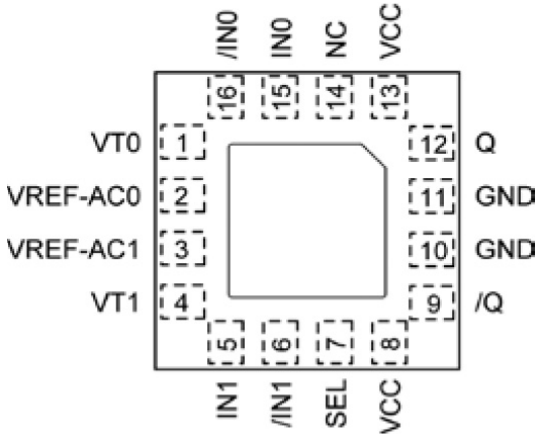
The SY58609U is a 2.5/3.3V, high-speed, fully differential CML 2:1 MUX capable of processing clock signals up to 2.5 GHz and data patterns up to 4.25 Gbps. The SY58609U is optimized to provide a buffered output of the selected input with less than 20 ps of skew and less than 10pspp total jitter.

The differential input includes Microchip's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100 mV (200 mVpp) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an integrated reference voltage ($V_{REF-AC}$) is provided to bias the VT pin. The outputs are 400 mV CML, with extremely fast rise/fall times guaranteed to be less than 90 ps.

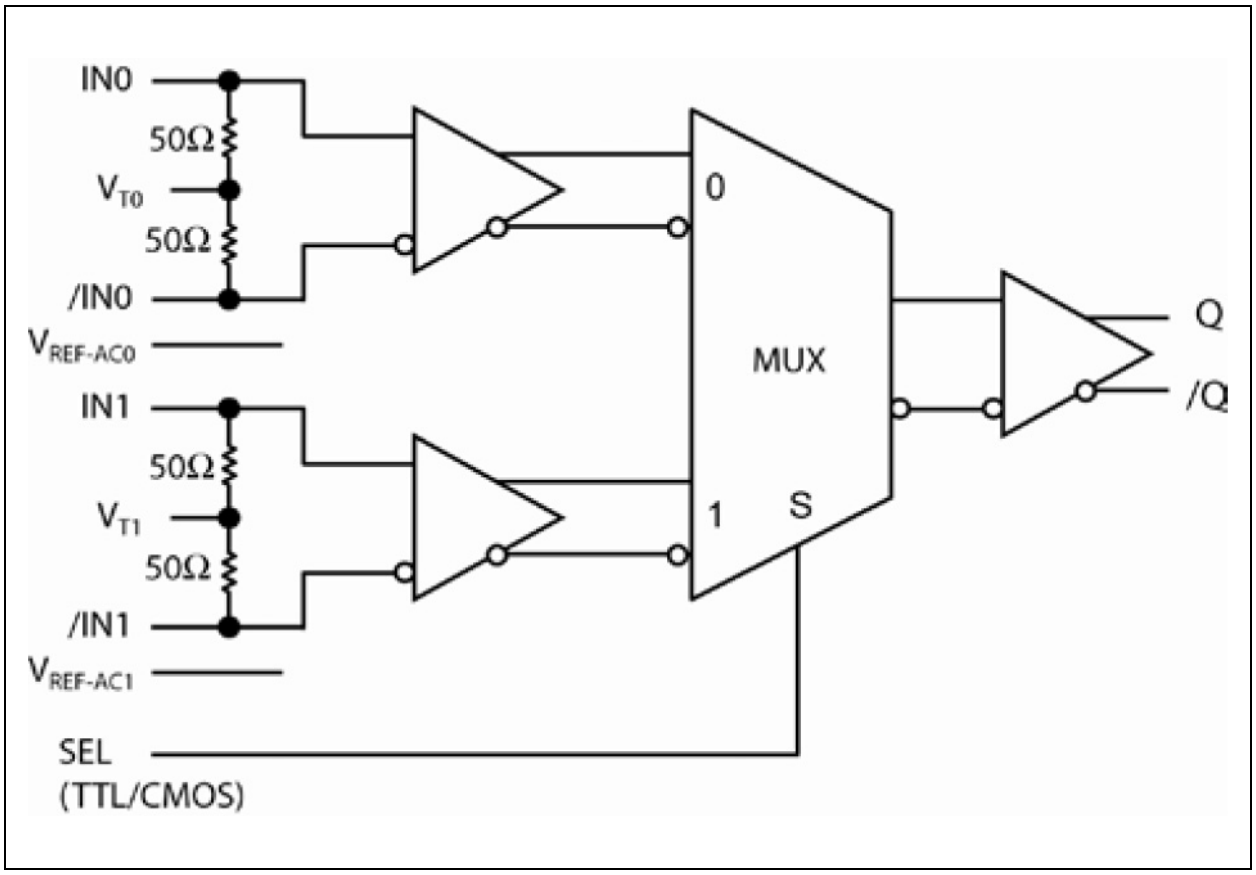
The SY58609U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require LVPECL or LVDS outputs, consider Microchip's SY58610U and SY58611U, 2:1 MUX with 800 mV and 325 mV output swings, respectively. The SY58609U is part of Microchip's high-speed Precision Edge® product line.

### Package Type

**SY58609U**
16-Lead VQFN



### Functional Block Diagram



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings†

Supply Voltage ($V_{CC}$) ..... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$
CML Output Voltage ($V_{OUT}$) ..... $V_{CC}$ – 1.0V to $V_{CC}$ + 0.5V
Current (VT), source or sink on VT pin ..... ±100 mA
Input Current, source or sink current on (IN, /IN) ..... ±50 mA
Current ($V_{REF}$), source or sink current on $V_{REF-AC}$ (Note 4) ..... ±0.5 mA

## Operating Ratings††

Supply Voltage ($V_{CC}$) ..... +2.375V to +3.60V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 1:** Due to the limited drive capability, use for input of the same package only.

**TABLE 1-1: DC ELECTRICAL CHARACTERISTICS**

| All values applicable for when $T_A$ = –40°C to +85°C unless otherwise stated. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Power Supply Voltage Range | $V_{CC}$ | 2.375 | 2.5 | 2.625 | V | — |
| | | 3.0 | 3.3 | 3.6 | | |
| Power Supply Current | $I_{CC}$ | — | 50 | 60 | mA | No load, max. $V_{CC}$ |
| Differential Input Resistance (IN-to-/IN) | $R_{DIFF\_IN}$ | 90 | 100 | 110 | Ω | — |
| Input HIGH Voltage (IN, /IN) | $V_{IH}$ | $V_{CC}$ – 1.6 | — | $V_{CC}$ | V | Note 2 |
| Input LOW Voltage (IN, /IN) | $V_{IL}$ | 0.2 | — | $V_{IH}$ – 0.1 | V | — |
| Input Voltage Swing (IN, /IN) | $V_{IN}$ | 0.1 | — | 1.0 | V | See Figure 8-1, Note 3 |
| Differential Input Voltage Swing (\|IN – /IN\|) | $V_{DIFF\_IN}$ | 0.2 | — | — | V | See Figure 8-2 |
| Input Voltage Threshold that Triggers FSI | $V_{IN\_FSI}$ | — | 30 | 100 | mV | — |
| AC Reference Voltage | $V_{REF-AC}$ | $V_{CC}$ – 1.3 | — | $V_{CC}$ – 1.0 | V | — |
| Voltage from Input to $V_T$ | $V_{T\_IN}$ | — | — | 1.28 | V | — |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**2:** $V_{IH}$ (min.) not lower than 1.2V.

**3:** $V_{IN}$ (max.) is specified when $V_T$ is floating.

**TABLE 1-2: CML OUTPUTS DC ELECTRICAL CHARACTERISTICS**

| $V_{CC}$ = +2.5V ±5% or +3.3V ±10%; $R_L$ = 100Ω across the outputs; and $T_A$ = –40°C to +85°C, unless otherwise stated. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Output High Voltage | $V_{OH}$ | $V_{CC}$ – 0.020 | $V_{CC}$ – 0.010 | $V_{CC}$ | V | $R_L$ = 50Ω to $V_{CC}$ |
| Output Voltage Swing | $V_{OUT}$ | 325 | 400 | 500 | mV | See Figure 8-1 |
| Differential Output Voltage Swing | $V_{DIFF\_OUT}$ | 650 | 800 | 1000 | mV | See Figure 8-2 |
| Output Source Impedance | $R_{OUT}$ | 45 | 50 | 55 | Ω | — |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**TABLE 1-3: LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS**

| $V_{CC}$ = +2.5V ±5% or +3.3V ±10%; $T_A$ = –40°C to +85°C, unless otherwise stated. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Input HIGH Voltage | $V_{IH}$ | 2.0 | — | — | V | — |
| Input LOW Voltage | $V_{IL}$ | — | — | 0.8 | V | — |
| Input HIGH Current | $I_{IH}$ | –125 | — | 30 | µA | — |
| Input LOW Current | $I_{IL}$ | –300 | — | — | µA | — |

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**TABLE 1-4: AC ELECTRICAL CHARACTERISTICS**

| $V_{CC}$ = +2.5V ±5% or +3.3V ±10%; $R_L$ = 100Ω across the outputs; Input $t_r/t_f$ ≤300 ps; and $T_A$ = –40°C to +85°C, unless otherwise stated. (Note 1) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| Maximum Operating Frequency | $f_{MAX}$ | 4.25 | — | — | Gbps | NRZ Data |
| | | 2.5 | 3 | — | GHz | $V_{OUT}$ >200 mV (Clock) |
| Propagation Delay (IN-to-Q) | $t_{pd}$ | 180 | 330 | 450 | ps | $V_{IN}$: 100 mV – 200 mV |
| | | 140 | 270 | 370 | ps | $V_{IN}$: >200 mV |
| SEL-to-Q | $t_{pd}$ | 150 | — | 450 | ps | — |
| Input-to-Input Skew | $t_{SKEW}$ | — | 5 | 20 | ps | Note 2, Note 3 |
| Part-to-Part Skew | | — | — | 150 | ps | Note 4 |
| Data (Random Jitter) | $t_{JITTER}$ | — | — | 1 | $ps_{RMS}$ | Note 5 |
| Data (Deterministic Jitter) | | — | — | 10 | $ps_{PP}$ | Note 6 |
| Clock (Cycle-to-Cycle Jitter) | | — | — | 1 | $ps_{RMS}$ | Note 7 |
| Clock (Total Jitter) | | — | — | 10 | $ps_{PP}$ | Note 8 |
| Output Rise/Fall Time 20% to 80% | $t_r$, $t_f$ | 35 | 50 | 90 | ps | At full output swing. |
| Duty Cycle | α | 47 | — | 53 | % | Differential I/O. |

**Note 1:** High-frequency AC-parameters are guaranteed by design and characterization.

**2:** Input-to-Input skew is the time difference between the two inputs and one output, under identical input transitions.

**3:** Input-to-Input Skew is included in IN-to-Q propagation delay.

**4:** Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature, same transition edge, and no skew at the edges at the respective inputs.

**5:** Random jitter is measured with a K28.7 pattern, measured at ≤ $f_{MAX}$.

**6:** Deterministic jitter is measured at 2.5 Gbps with both K28.5 and 223 – 1 PRBS pattern.

**7:** Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.

**8:** Total jitter definition: With an ideal clock input frequency of ≤ $f_{MAX}$ (device), no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.

**TABLE 1-5: TEMPERATURE SPECIFICATIONS**

| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
|---|---|---|---|---|---|---|
| **Temperature Range** | | | | | | |
| Operating Ambient Temperature | $T_A$ | –40 | — | +85 | °C | — |
| Maximum Operating Junction Temperatuer | $T_{JMAX}$ | — | +125 | — | °C | |
| Lead Temperature | $T_{LEAD}$ | — | +260 | — | °C | Soldering, 20 sec. |
| Storage Temperature | $T_S$ | –65 | — | +150 | °C | — |
| **Package Thermal Resistance** (Note 1) | | | | | | |
| VQFN, Still Air | $\theta_{JA}$ | — | +60 | — | °C/W | — |
| VQFN, Junction-to-Board | $\psi_{JB}$ | — | +33 | — | °C/W | — |

**Note 1:** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. $\psi_{JB}$ and $\theta_{JA}$ values are determined for a 4-layer board in still-air number, unless otherwise stated.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number | Pin Name | Description |
|---|---|---|
| 1, 4 | VT0, VT1 | **Input Termination Center-Tap:** Each side of the differential input pair terminates to the VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” subsection. |
| 2, 3 | VREF-AC0<br>VREF-AC1 | **Reference Voltage:** These outputs bias to $V_{CC}$ – 1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01 µF low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is ±0.5 mA. See “Input Interface Applications” subsection. |
| 5, 6<br>15, 16 | IN1, /IN1<br>IN0, /IN0 | **Differential Inputs:** These input pairs are the differential signal inputs to the device. Inputs accept DC-Coupled differential signals as small as 100 mV (200 mVpp). Each pin of the pairs internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30 mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state. See “Input Interface Applications” subsection. |
| 7 | SEL | **Single-Ended Input:** This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic HIGH state if left open. The input-switching threshold is $V_{CC}/2$. |
| 8, 13 | VCC | **Positive Power Supply:** Bypass with 0.1 uF \|\| 0.01 uF low ESR capacitors as close to the VCC pins as possible. |
| 9, 12 | /Q, Q | **CML Differential Output Pair:** Differential buffered output copy of the selected input signal. The output swing is typically 400 mV. Normally terminate with 100Ω across Q and /Q. Unused output pair may be left floating with no impact on jitter. See “CML Output Termination” subsection. |
| 10, 11 | GND | **Ground.** Exposed pad must be connected to a ground plane that is the same potential as the ground pins. |
| 14 | NC | **No connect.** |

## 3.0 TYPICAL CHARACTERISTICS

$V_{CC}$ = 2.5V; GND = 0V; $V_{IN}$ = 100 mV; $R_L$ = 100Ω across the outputs; and $T_A$ = 25°C, unless otherwise stated.

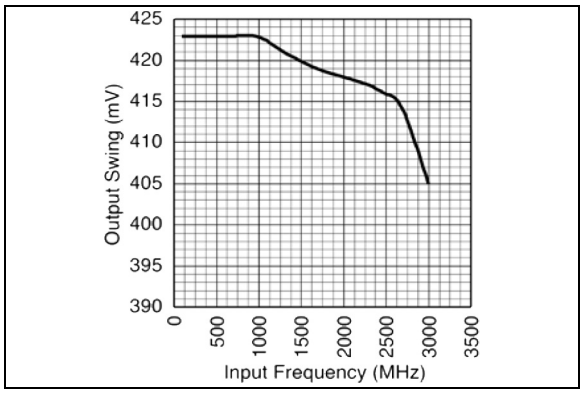



**FIGURE 3-1: FREQUENCY RESPONSE.**

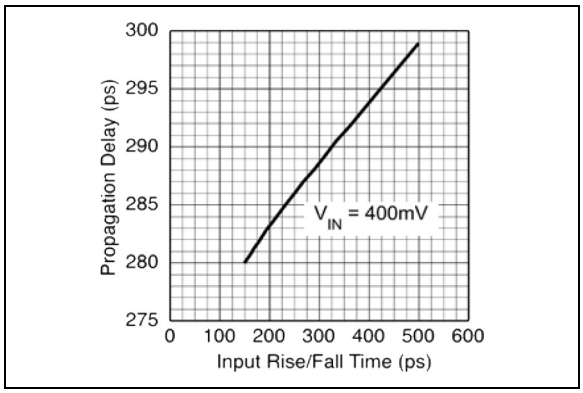



**FIGURE 3-4: PROPAGATION DELAY VS. INPUT RISE/FALL TIME.**

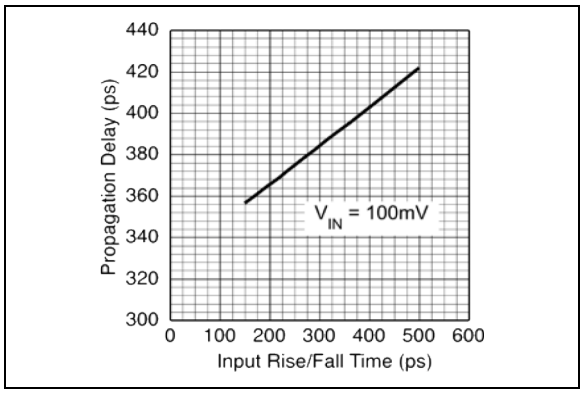



**FIGURE 3-2: PROPAGATION DELAY VS. INPUT RISE/FALL TIME.**

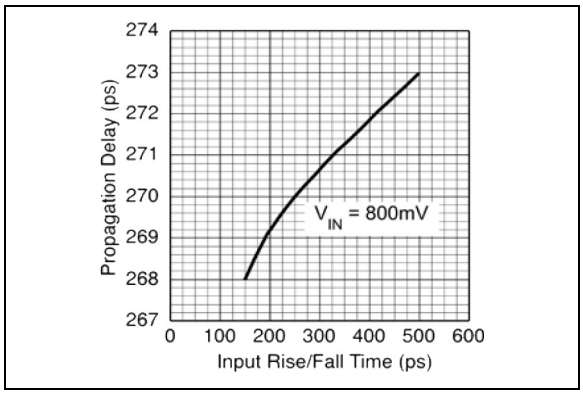



**FIGURE 3-5: PROPAGATION DELAY VS. INPUT RISE/FALL TIME.**

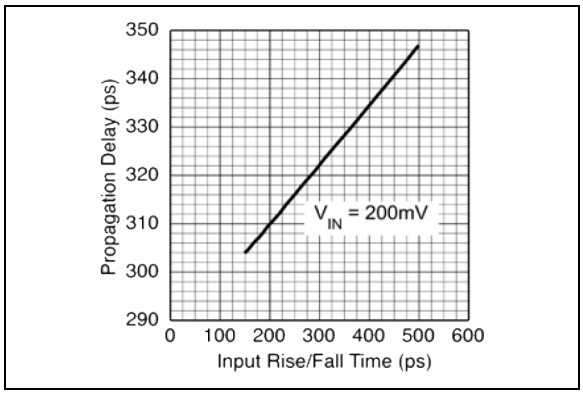



**FIGURE 3-3: PROPAGATION DELAY VS. INPUT RISE/FALL TIME.**

## 4.0 TYPICAL WAVEFORMS (FUNCTIONAL CHARACTERISTICS)

$V_{CC}$ = 2.5V; GND = 0V; $V_{IN}$ = 325 mV; $R_L$ = 100Ω across the outputs; and $T_A$ = 25°C, unless otherwise stated.

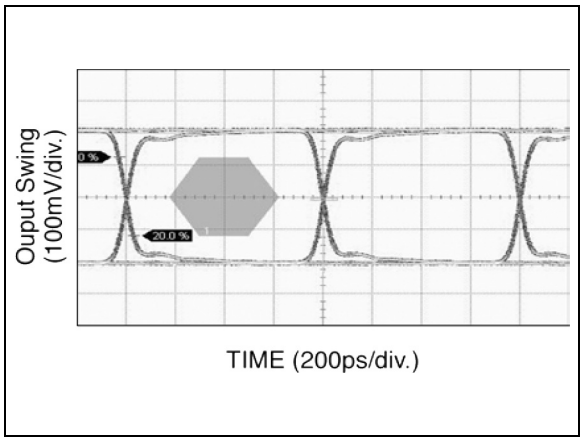



**FIGURE 4-1: 1.25 GBPS DATA.**

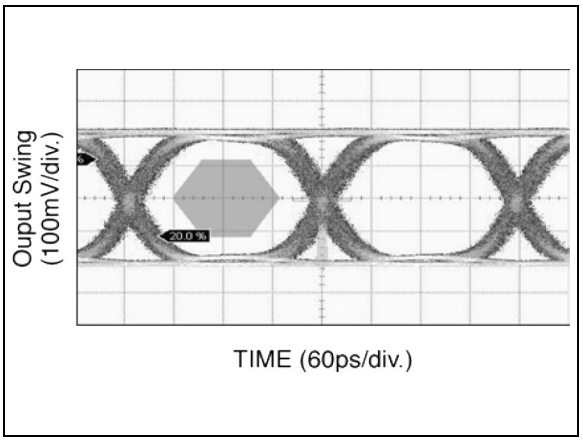



**FIGURE 4-4: 4.25 GBPS DATA.**

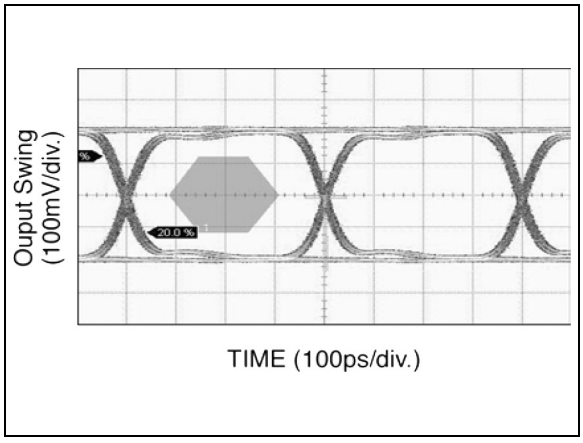



**FIGURE 4-2: 2.5 GBPS DATA.**

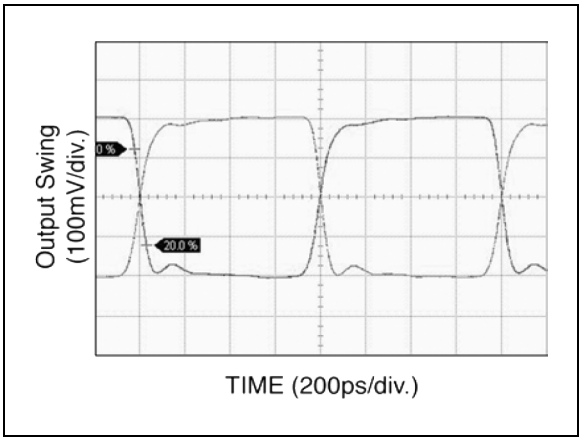



**FIGURE 4-5: 625 MHZ CLOCK.**

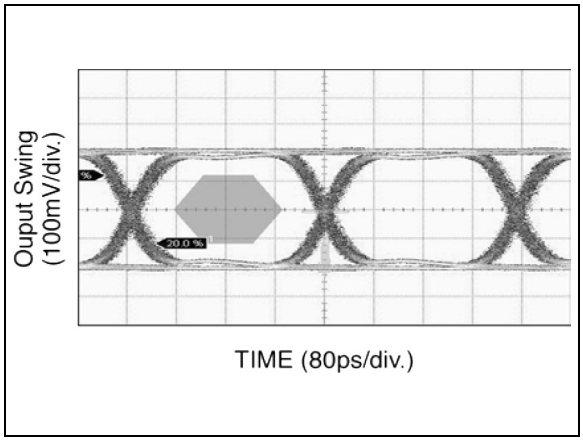



**FIGURE 4-3: 3.2 GBPS DATA.**

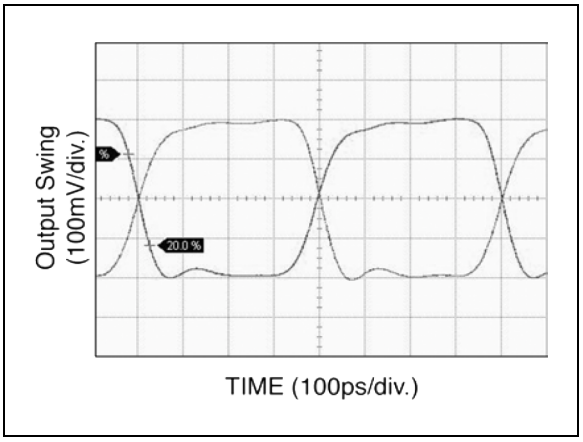



**FIGURE 4-6: 1.25 GHZ CLOCK.**

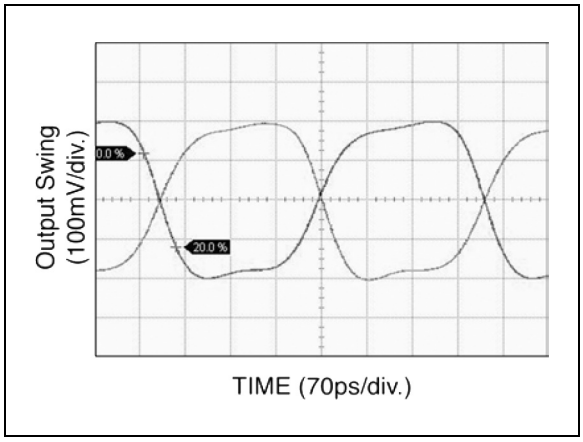



**FIGURE 4-7: 2 GHZ CLOCK.**

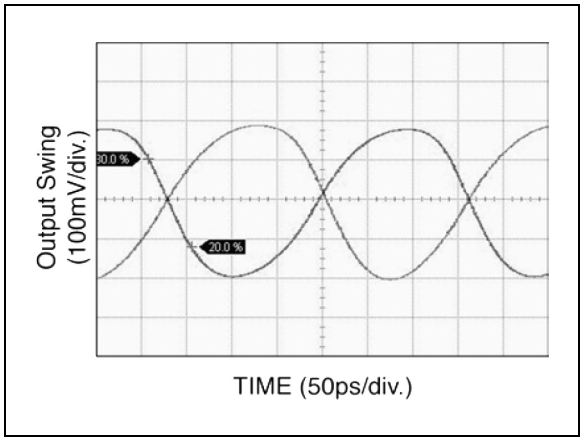



**FIGURE 4-8: 3 GHZ CLOCK.**

## 5.0 CML OUTPUT TERMINATION

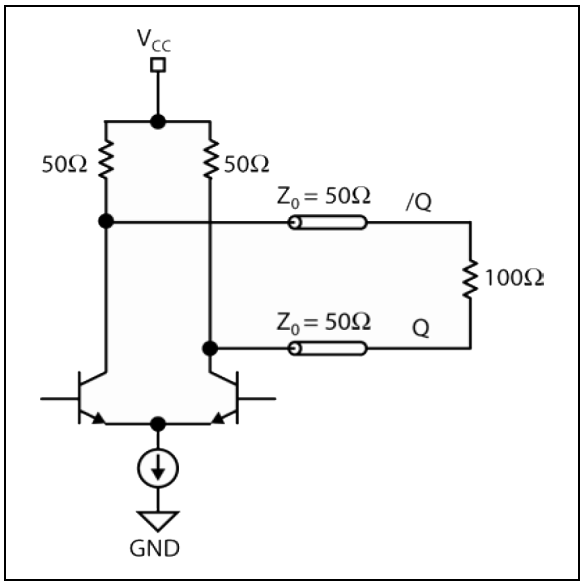



**FIGURE 5-1: CML DC-COUPLED TERMINATION.**

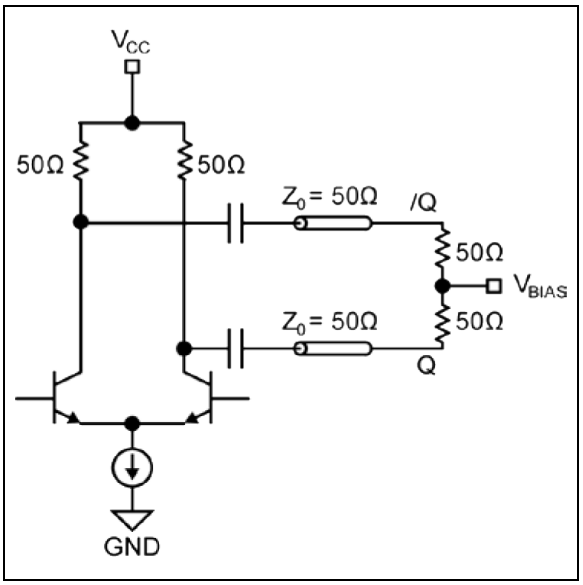



**FIGURE 5-3: CML AC-COUPLED TERMINATION.**

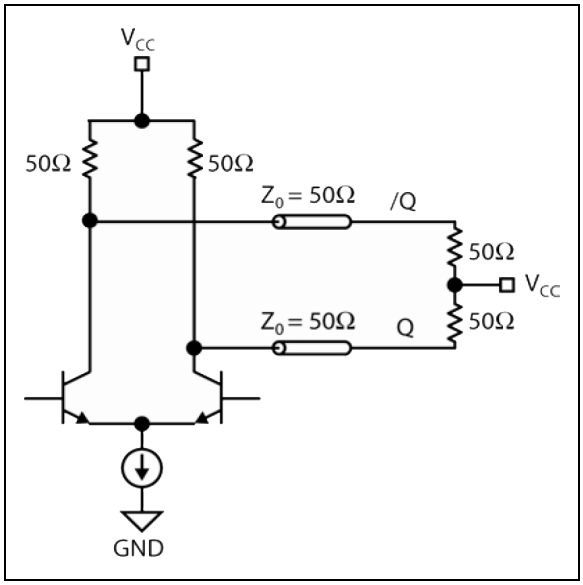



**FIGURE 5-2: CML DC-COUPLED TERMINATION.**

## 6.0 FUNCTIONAL DESCRIPTION

### 6.1 Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100mVPK (200mVPP), typically 30mVPK. Maximum frequency of the SY58609U is limited by the FSI function.

### 6.2 Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to “Typical Characteristics” for detailed information.

## 7.0 TIMING DIAGRAMS

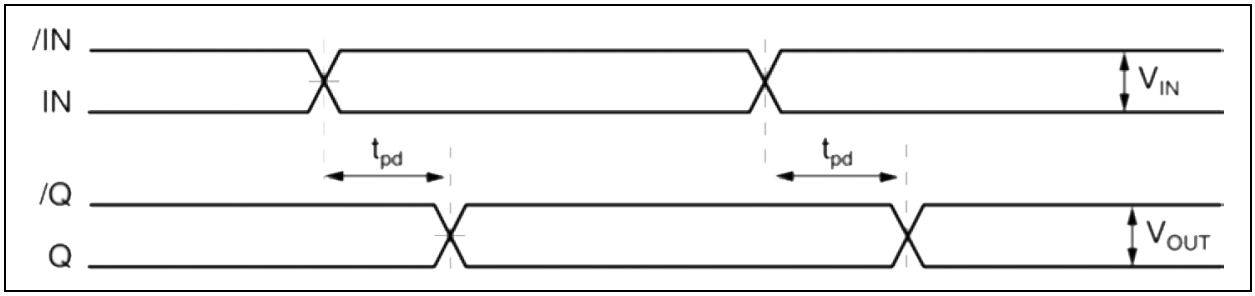



**FIGURE 7-1: TIMING DIAGRAM: PROPAGATION DELAY.**

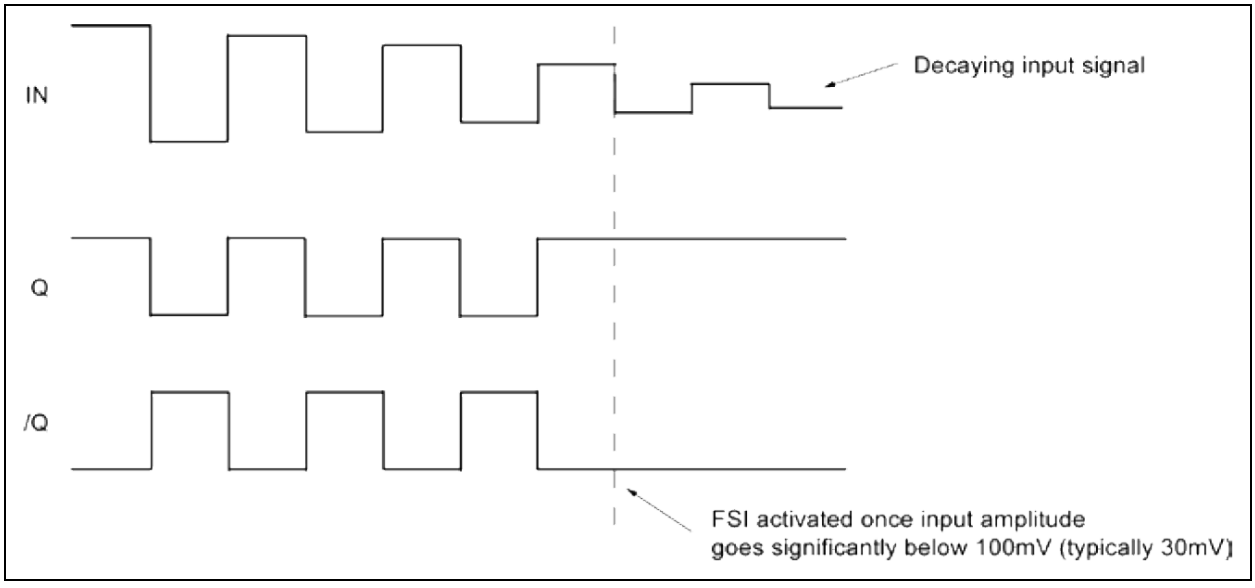



**FIGURE 7-2: TIMING DIAGRAM: FAIL-SAFE FEATURE.**

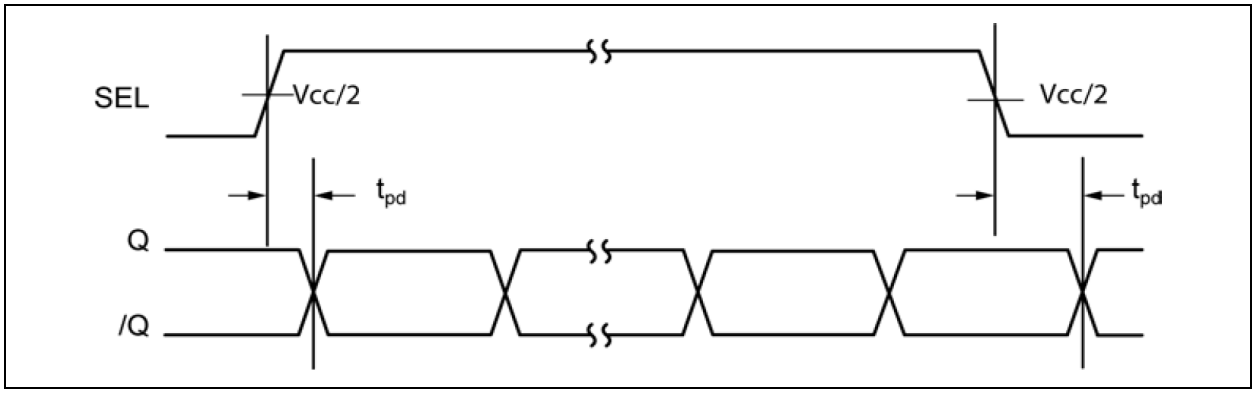



**FIGURE 7-3: TIMING DIAGRAM: SEL-TO-Q DELAY.**

## 8.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

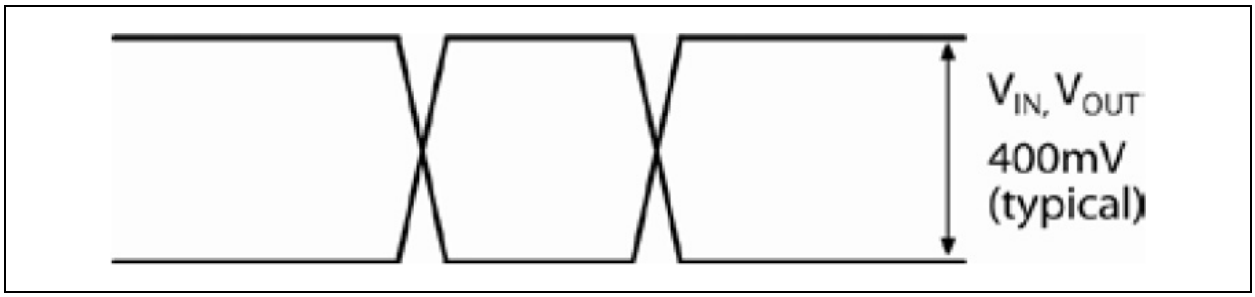



**FIGURE 8-1: SINGLE-ENDED VOLTAGE SWING.**

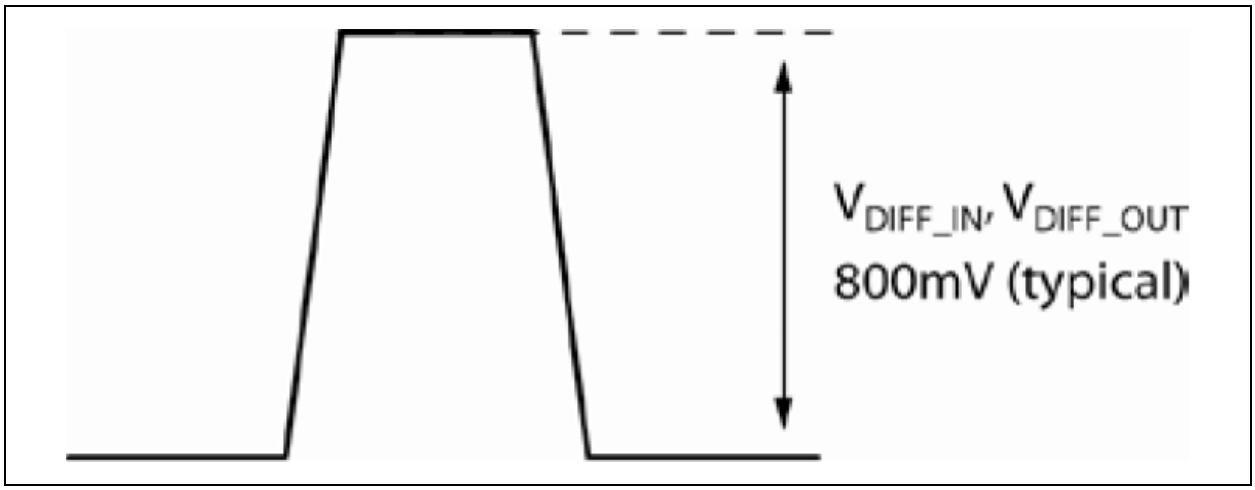



**FIGURE 8-2: DIFFERENTIAL VOLTAGE SWING.**

## 9.0 INPUT AND OUTPUT STAGE

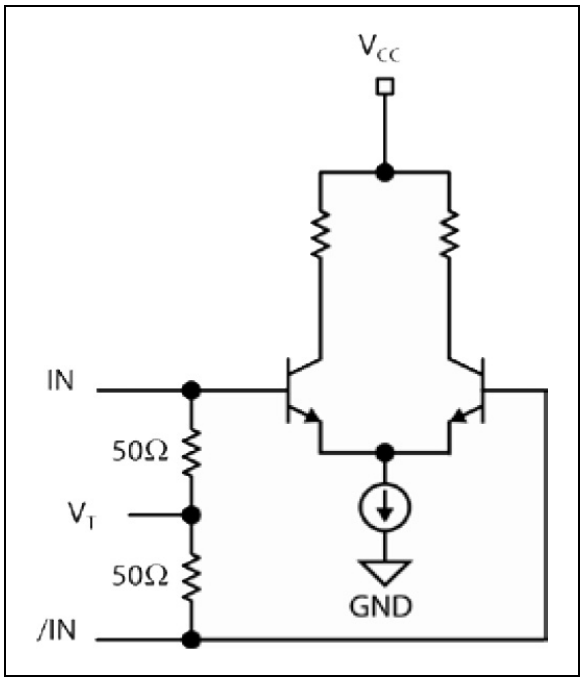



**FIGURE 9-1: SIMPLIFIED DIFFERENTIAL INPUT BUFFER.**

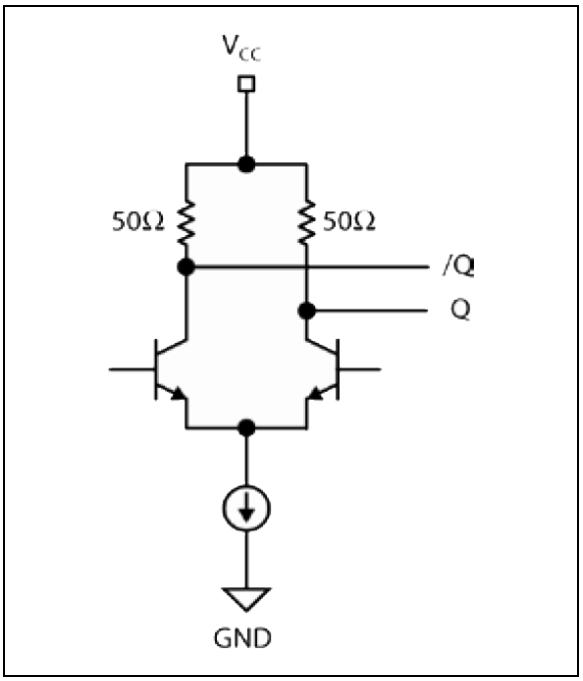



**FIGURE 9-2: SIMPLIFIED CML OUTPUT BUFFER.**

## 10.0 INPUT INTERFACE APPLICATIONS

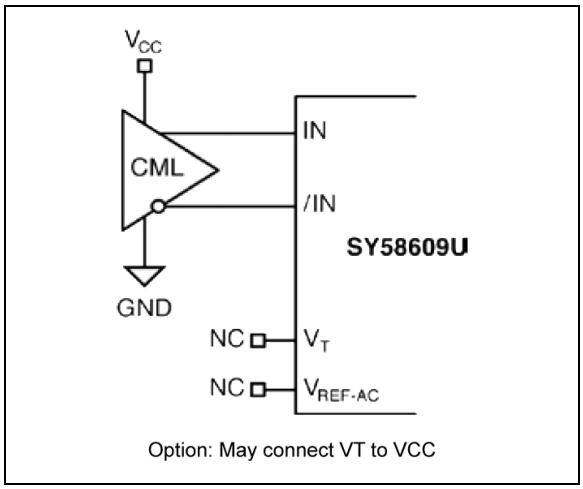



**FIGURE 10-1: DC-COUPLED CML INPUT INTERFACE.**

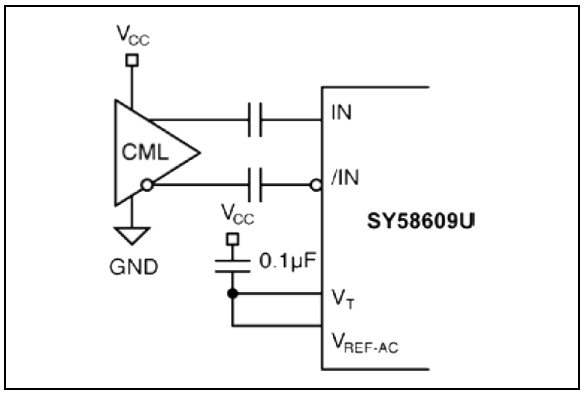



**FIGURE 10-2: AC-COUPLED CML INPUT INTERFACE.**

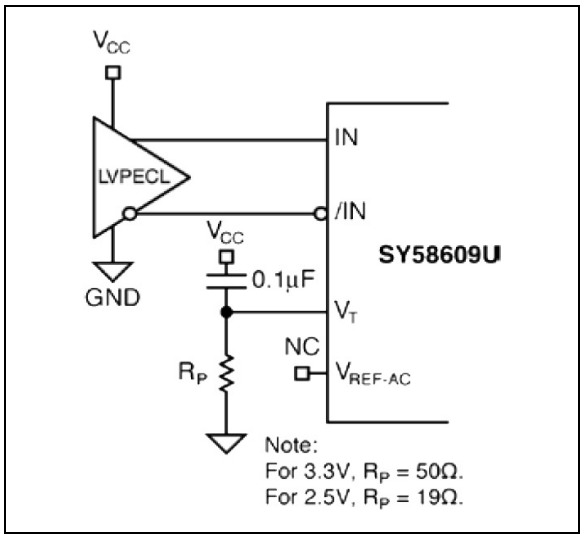



**FIGURE 10-3: DC-COUPLED LVPECL INPUT INTERFACE.**

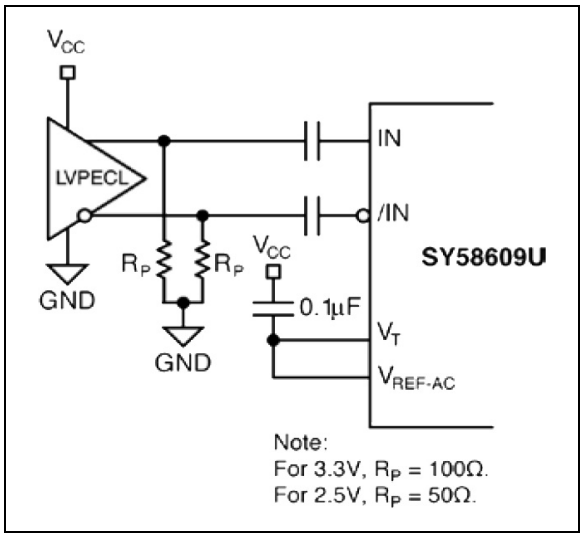



**FIGURE 10-4: AC-COUPLED LVPECL INPUT INTERFACE.**

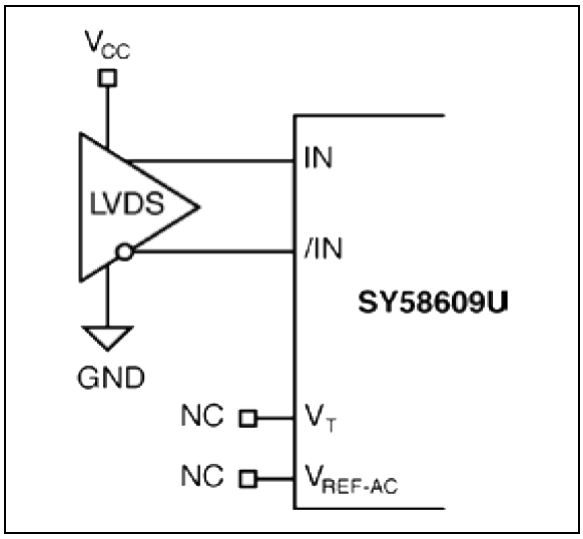
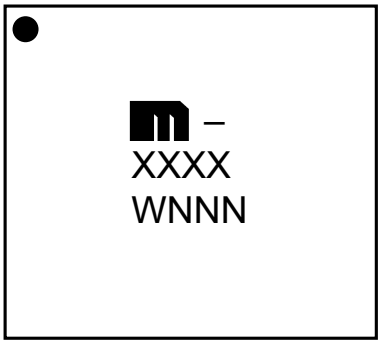



**FIGURE 10-5: DC-COUPLED LVDS INPUT INTERFACE.**

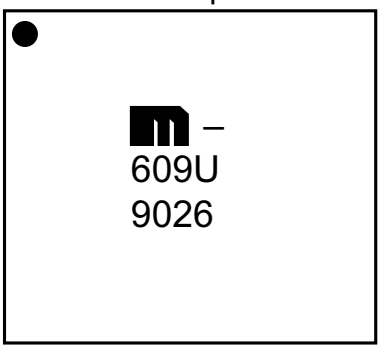
## 11.0 PACKAGING INFORMATION

### 11.1 Package Marking Information

16-Lead VQFN*




Example*



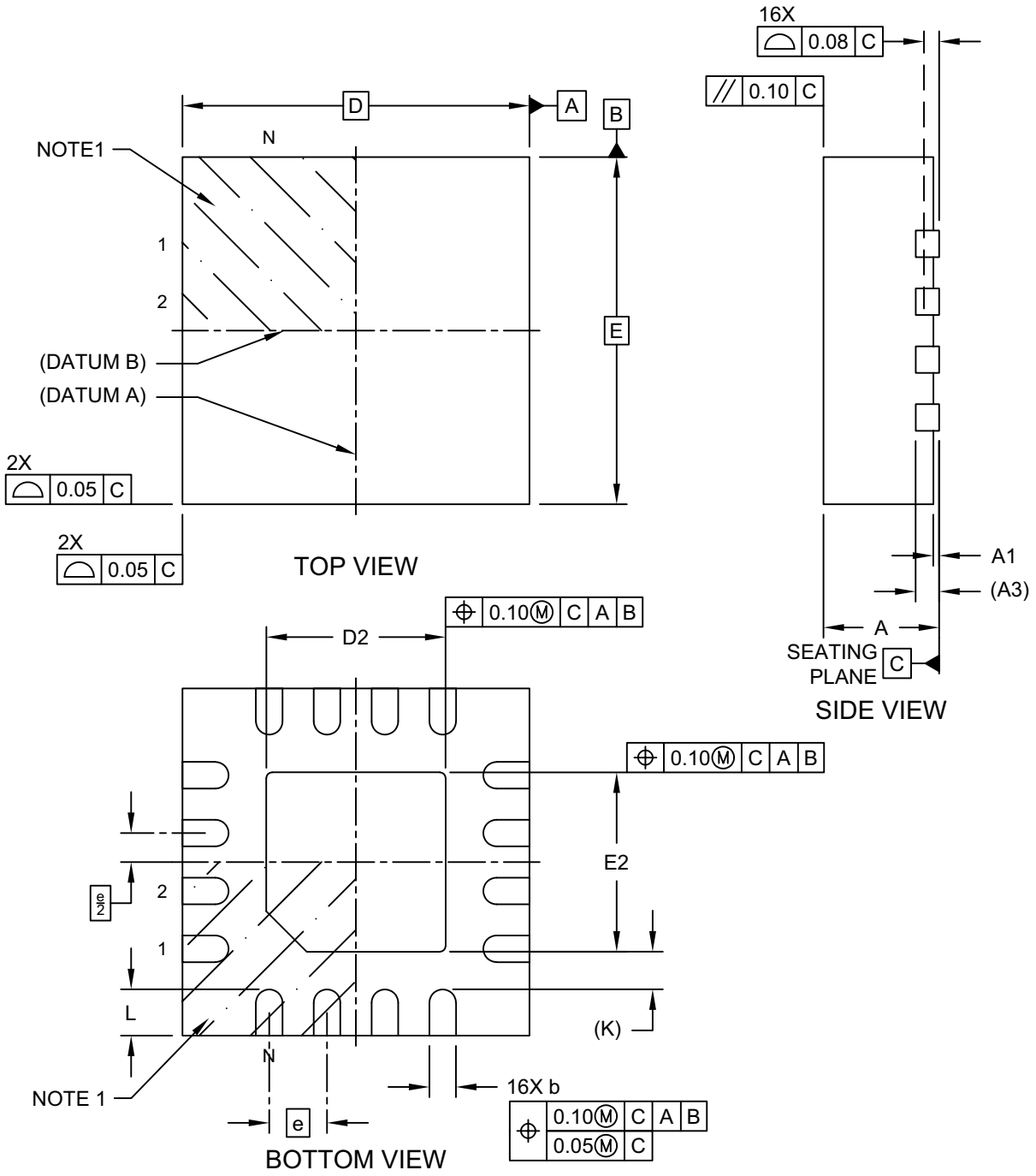

| | | |
|---|---|---|
| **Legend:** | XX...X | Product code or customer-specific information |
| | W | Week code |
| | NNN | Alphanumeric traceability code (week) |
| | * | This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package. |
| | ● | Pin one index is identified by a dot |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

## 16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

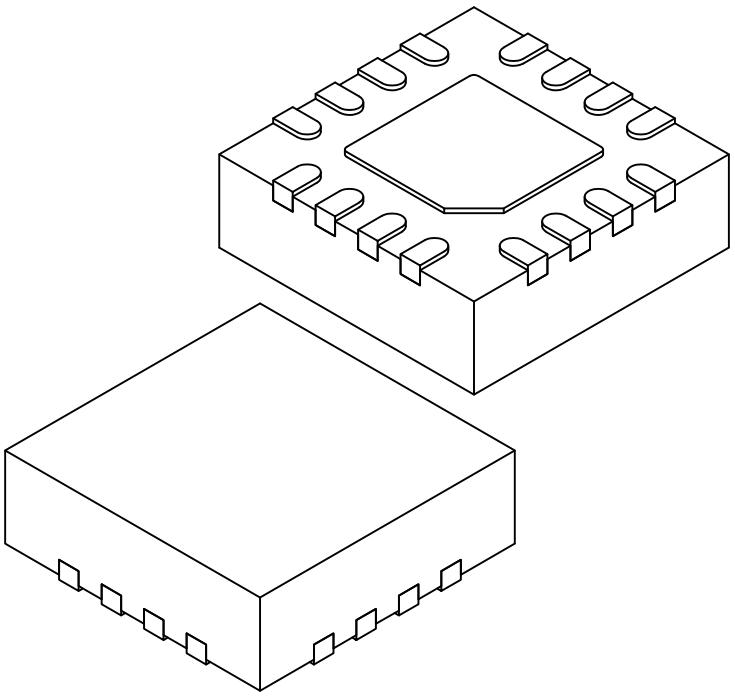
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

## 16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 16 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.203 REF | |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.50 | 1.55 | 1.60 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.50 | 1.55 | 1.60 |
| Terminal Width | b | 0.18 | 0.23 | 0.28 |
| Terminal Length | L | 0.35 | 0.40 | 0.45 |
| Terminal-to-Exposed-Pad | K | | 0.33 REF | |

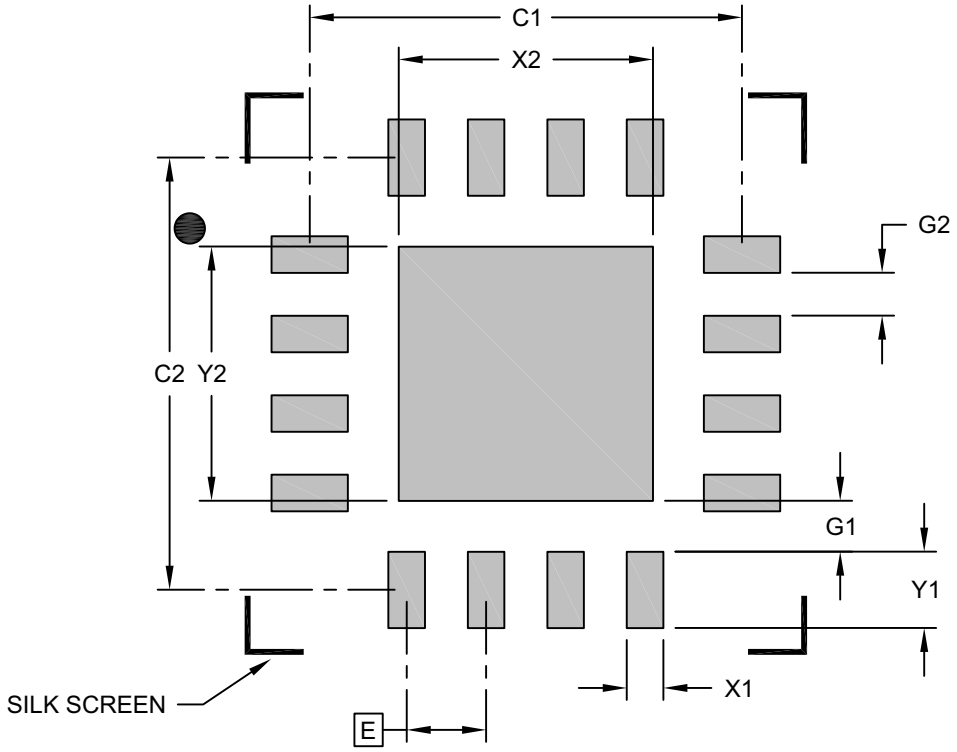
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

## 16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Center Pad Width | X2 | | | 1.60 |
| Center Pad Length | Y2 | | | 1.60 |
| Contact Pad Spacing | C1 | | 2.72 | |
| Contact Pad Spacing | C2 | | 2.72 | |
| Contact Pad Width (Xnn) | X1 | | | 0.23 |
| Contact Pad Length (Xnn) | Y1 | | | 0.48 |
| Contact Pad to Center Pad (Xnn) | G1 | 0.32 | | |
| Contact Pad to Contact Pad (Xnn) | G2 | 0.27 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision A (March 2024)

- Converted Micrel data sheet for SY58609U to Microchip format as DS20006873A.
- Minor text changes throughout.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | X | X | X | -XX |
|---|---|---|---|---|
| Device | Supply Voltage Range | Package | Temperature Range | Special Processing |

| | | | |
|---|---|---|---|
| **Device:** | SY58609 | = | 4.25 Gbps Precision, CML 2:1 MUX with Internal Termination and Fail Safe Input |
| **Voltage Option:** | U | = | 2.5V/3.3V |
| **Package:** | M | = | 16-Lead VQFN |
| **Temperature Range:** | G | = | –40°C to 85°C |
| **Special Processing:** | <blank> | = | 100/Tube |
| | TR | = | 1,000/Reel |

**Examples:**

a) **SY58609UMG**

2.5V/3.3V, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY58609UMG-TR**

2.5V/3.3V, 16-Lead VQFN, –40°C to 85°C, 1,000/Reel

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