Watchdog Timer and Power-Saving Modes

This section of the manual contains the following major topics:

Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices. Please consult the note at the beginning of the **"Special Features"** and **"Power-Saving Features"** chapters in the current device data sheet to check whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com.

1.0 INTRODUCTION

This section describes the Watchdog Timer (WDT) and Power-Saving Modes implemented in dsPIC33/PIC24 devices. The dsPIC33/PIC24 device family offers a number of built-in capabilities that allow user applications to select the best balance of performance and low-power consumption.

The WDT resets the device in the event of a software malfunction. It can also be used to wake the device from Sleep or Idle mode.

2.0 POWER-SAVING MODES

Power-saving features implemented in dsPIC33/PIC24 devices include the following:

- System Clock Management
- Instruction-Based Power-Saving Modes
- Doze Mode
- Peripheral Module Disable

2.1 System Clock Management

Reducing the system clock frequency results in power-saving that is roughly proportional to the frequency reduction. The dsPIC33/PIC24 devices provide an on-the-fly clock switching feature that allows the user application to optimize power consumption by dynamically changing the system clock frequency. For details, refer to **"Oscillator"** (DS70580).

2.2 Instruction-Based Power-Saving Modes

The dsPIC33/PIC24 devices can operate in two instruction-based power-saving modes. These modes can be entered by executing a special `PWRSAV` instruction.

Note:	Execution of `PWRSAV` instruction is ignored while any of the NVM operations are in progress.

If an interrupt coincides with the execution of a `PWRSAV` instruction, the interrupt is delayed until the device fully enters Sleep or Idle mode. If the interrupt is a wake-up event, it will then wake-up the device and execute.

- **Sleep Mode**: In Sleep mode, the CPU, the system clock source and the peripherals that operate on the system clock source are disabled. This is the lowest-power mode for the device.

  The SLEEP status flag bit in the Reset Control register (RCON<4>) is set when the device enters Sleep mode.

- **Idle Mode**: In Idle mode, the CPU is disabled, but the system clock source continues to operate. The peripherals continue to operate but can optionally be disabled.
  The IDLE status flag bit in the Reset Control register (RCON<3>) is set when the device enters Idle mode.

The SLEEP and IDLE status bits are cleared on Power-on Reset (POR) and Brown-out Reset (BOR). These bits can also be cleared in software. For more information on resets, refer to **"Reset"** (DS70602).

The assembly syntax of the PWRSAV instruction is shown in Example 2-1.

Example 2-1: PWRSAV Assembly Syntax

```
PWRSAV  #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE     ; Put the device into IDLE mode
```

Note 1: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

2: Sleep mode does not change the state of the I/O pins.

2.2.1 SLEEP MODE

Sleep mode is the lowest current-consumption state. The characteristics of Sleep mode include the following:

- The Primary Oscillator (POSC) and internal FRC Oscillator are disabled
- The Secondary Oscillator (SOSC) continues to run if the Secondary Oscillator Enable bit (LPOSCEN) in the Oscillator Control register (OSCCON<1>) is set. For details, refer to **"Oscillator"** (DS70580).
- The WDT, clock source and LPRC Oscillator continue to run if the Watchdog Timer is enabled. The WDT, if enabled, is automatically cleared prior to entering Sleep mode. For details, see **Section 3.0 "Watchdog Timer"**.
- If the Voltage Regulator Standby Enable bit (VREGS) is cleared in the Reset Control register (RCON<8>), the internal voltage regulator enters the Standby state. The voltage regulator consumes a reduced amount of current in the Standby state.
- If the Flash Memory Voltage Regulator Standby Enable bit (VREGSF) in the Reset Control register (RCON<11>) is cleared, the voltage regulator that powers the Flash memory enters the Standby state. The Flash voltage regulator consumes a reduced amount of current in the Standby state.
- The peripherals operating with the system clock are disabled
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode, because the system clock is disabled

To minimize current consumption in Sleep mode, do the following:

- Ensure that I/O pins do not drive resistive loads
- Ensure that I/O pins configured as inputs are not floating
- Disable the SOSC
- Disable the WDT
- Enable the voltage regulator to enter Standby state in Sleep mode

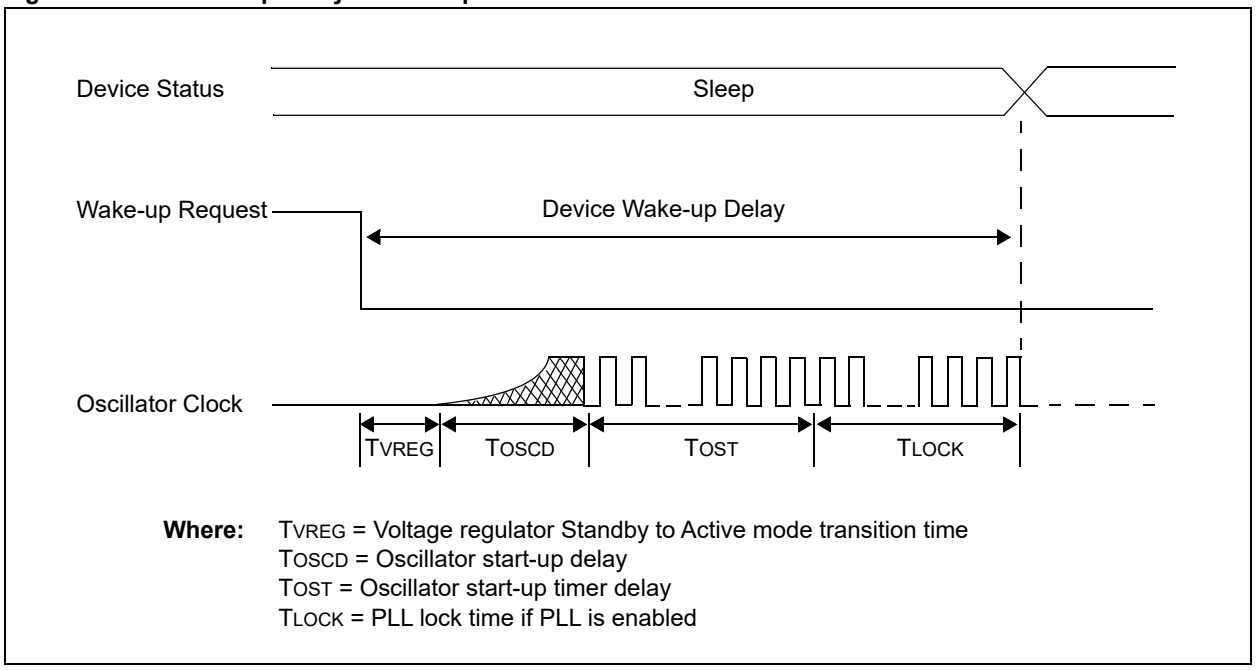
When the device exits Sleep mode, it restarts with the current clock source as indicated by the Current Clock Source Selection bits (COSC<2:0>) in the Oscillator Control register (OSCCON<14:12>).

2.2.1.1 Delay on Wake-up from Sleep

Figure 2-1 shows the wake-up delay from Sleep mode. This delay consists of the voltage regulator delay and the oscillator delay:

- **Voltage Regulator Delay**: This is the time delay for the voltage regulator to transition from Standby state to Active state. This delay is required only if Standby mode is enabled for the voltage regulator.
- **Oscillator Delay**: The time delay for the clock to be ready for various clock sources is shown in Table 2-1. For details, refer to **"Oscillator"** (DS70580).

Figure 2-1: Wake-up Delay from Sleep Mode



Where: TVREG = Voltage regulator Standby to Active mode transition time
TOSCD = Oscillator start-up delay
TOST = Oscillator start-up timer delay
TLOCK = PLL lock time if PLL is enabled

Table 2-1: Oscillator Delay(1,2,3)

Oscillator Source	Oscillator Start-up Delay	Oscillator Start-up Timer	PLL Lock Time	Total Delay
FRC, FRCDIV16, FRCDIVN	TOSCD	—	—	TOSCD
FRCPLL	TOSCD	—	TLOCK	TOSCD + TLOCK
XT	TOSCD	TOST	—	TOSCD + TOST
HS	TOSCD	TOST	—	TOSCD + TOST
EC	—	—	—	—
XTPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
HSPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
ECPLL	—	—	TLOCK	TLOCK
SOSC	TOSCD	TOST	—	TOSCD + TOST
LPRC	TOSCD	—	—	TOSCD

Note 1: TOSCD = Oscillator start-up delay. Crystal Oscillator start-up time varies with crystal characteristics, load capacitance, etc.

2: TOST = Oscillator start-up timer delay.

3: TLOCK = PLL lock time, if PLL is enabled.

Note: Refer to the **"Electrical Characteristics"** chapter of the specific device data sheet for TVREG, TOST and TLOCK specifications, and also for the TOSCD specifications when using the internal FRC or internal LPRC Oscillator.

2.2.2 IDLE MODE

Idle mode has the following characteristics:

- The CPU stops executing instructions
- The system clock source remains active
- The WDT is automatically cleared
- If the WDT or FSCM is enabled, the LPRC remains active
- The peripheral modules, by default, continue to operate normally from the system clock source
- Peripherals can optionally be shut down using their Stop-in-Idle control bit (SIDL), which is located in bit position 13 of the control register for most peripheral modules. The generic bit-field name format is “xxxSIDL” (where, “xxx” is the mnemonic name of the peripheral device).

When the device exits Idle mode, the CPU starts executing instructions within eight system clock cycles.

2.2.3 WAKE-UP FROM SLEEP AND IDLE

Sleep and Idle modes exit on the following events:

- An enabled interrupt event
- A WDT time-out
- Reset from any source (Power-on Reset, Brown-out Reset and $\overline{\text{MCLR}}$)

2.2.3.1 Wake-up on Interrupt

An enabled interrupt event wakes up the device from Sleep or Idle mode, and then the following occurs:

- If the assigned priority for the interrupt is less than or equal to the current CPU priority, the device wakes up and continues code execution from the instruction following the `PWRSAV` instruction that initiated Sleep mode
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device wakes up and the CPU exception process begins. Code execution continues from the first instruction of the ISR.

2.2.3.2 Wake-up on WDT Time-out

If enabled, the Watchdog Timer continues to run during Sleep mode or Idle mode. When the WDT time-out occurs, the device wakes up and code execution continues from where the `PWRSAV` instruction was executed.

The Watchdog Time-out Flag bit (WDTO) in the Reset Control register (RCON<4>) is set to indicate that the wake-up event is due to a WDT time-out.

2.2.3.3 Wake-up on Reset

A Reset from any source (Power-on Reset, Brown-out Reset and $\overline{\text{MCLR}}$) causes the device to exit Sleep or Idle mode and begin executing from the Reset vector.

2.3 Doze Mode

The preferred strategy for reducing power consumption is to change clock speed and invoke Idle or Sleep mode. However, there may be circumstances where this strategy is not practical. The following effects must be considered:

- Manipulating the system clock speed alters the communication peripheral baud rate and can introduce communication errors
- Using an instruction-based power-saving mode (Idle/Sleep) completely stops processor execution

Doze mode provides an alternative method to reduce power consumption. In Doze mode, the peripherals are clocked at the system clock frequency, whereas the CPU is clocked at a reduced speed.

Doze mode is enabled by setting the Doze Enable bit (DOZEN) in the Clock Divisor register (CLKDIV<11>). The ratio between peripheral and CPU clock speed is determined by the Doze Ratio bits (DOZE<2:0>) in the Clock Divisor register (CLKDIV<14:12>). There are eight possible configurations, ranging from 1:1 to 1:128, with 1:1 being the default.

The CPU automatically returns to full-speed operation on any interrupt when the Recover On Interrupt bit (ROI) is set in the Clock Divisor register (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

2.4 Peripheral Module Disable

All peripheral modules (except for I/O ports) in dsPIC33/PIC24 devices have a control bit that can be selectively disabled to reduce power consumption. These bits, known as the Peripheral Module Disable bits (PMD), are generically named “xxxMD” (where “xxx” is the mnemonic version of the module’s name). These bits are located in the PMDx Special Function Registers (SFRs). The PMD bit must be set (= 1) to disable the module. The PMD bit completely shuts down the peripheral, effectively powering down all circuits and removing all clock sources. All peripherals are enabled by default. Refer to the specific device data sheet for PMD register details.

3.0 WATCHDOG TIMER

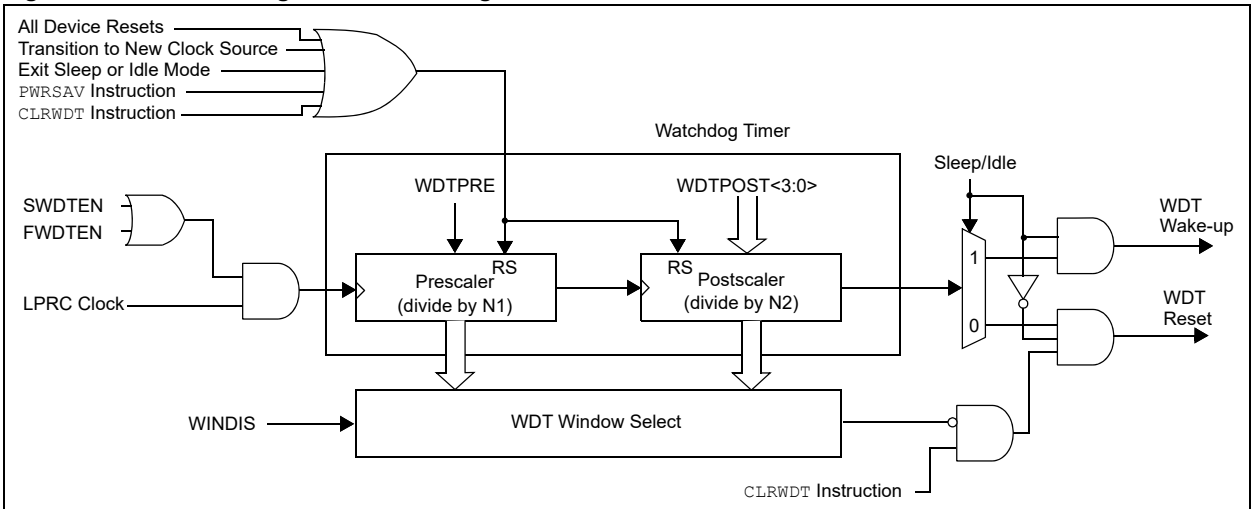
The Watchdog Timer has the following characteristics:

- 16 configurable time-out periods
- 5-bit or 7-bit prescaler
- 16-bit postscaler
- Hardware and software enabled
- Accelerated test interface
- Windowed WDT option

The Watchdog Timer is a free-running timer. The primary function of the Watchdog Timer is to reset the device in the event of a software malfunction. It can also be used to wake the device from Sleep or Idle mode.

The Watchdog Timer consists of a configurable 5-bit or 7-bit prescaler and a configurable postscaler clocked with the Low-Power RC (LPRC) Oscillator. The watchdog time-out period is selected by configuring the prescaler and postscaler dividers. A block diagram of the Watchdog Timer is shown in Figure 3-1.

Figure 3-1: Watchdog Timer Block Diagram



Note: For prescaler divider ratio (N1) and postscaler divider ratio (N2), see Table 3-1.

3.1 Prescaler/Postscaler

The nominal Watchdog Timer clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT time-out period (TWDT) of 1 ms in 5-bit mode, or 4 ms in 7-bit mode.

A variable postscaler divides the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any form of device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware
- When a `PWRSAV` instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a `CLRWDT` instruction during normal execution

Note: The `CLRWDT` and `PWRSAV` instructions clear the prescaler and postscaler counts.

3.2 Watchdog Timer Operation

When enabled, the Watchdog Timer increments until it overflows or times out. A WDT time-out forces a device Reset, except during Sleep or Idle modes. To prevent a WDT time-out Reset, the software must periodically clear the Watchdog Timer using the `CLRWDT` instruction.

The WDT is also cleared when the device enters Sleep or Idle modes after executing the `PWRSAV` instruction. If the WDT times out during Sleep or Idle modes, the device wakes up and continues code execution from where the `PWRSAV` instruction was executed.

In either case, the Watchdog Time-out Flag bit (WDTO) in the Reset Control register (RCON<4>) is set to indicate that the device Reset or wake-up event is due to a WDT time-out.

3.2.1 ENABLING AND DISABLING THE WDT

The WDT is enabled or disabled by the Watchdog Enable bit (FWDTEN) in the WDT Configuration register (FWDT<7>). When the FWDTEN bit is set, the WDT is always enabled. This is the default value for an erased device.

If the WDT bit is disabled in the FWDT register, the user application can optionally enable the WDT by setting the Software Watchdog Enable bit (SWDTEN) in the Reset Control register (RCON<5>).

The SWDTEN control bit is cleared on any form of device Reset. The SWDTEN bit allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not cleared automatically after a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

Note:	The WDT Configuration register (FWDT) values are written during device programming. For details on the WDT Configuration register, refer to **"Device Configuration"** (DS70000618).

3.2.2 WATCHDOG TIMER WINDOW

The Watchdog Timer has an optional Windowed mode enabled by programming the WINDIS bit (FWDT<6>). In the Windowed mode (WINDIS = `0`), the WDT should be cleared within the last 25% of the Watchdog time-out period, as shown in Figure 3-2. Some devices also have the option of a programmable WDT window, where the WDT should be cleared based on the programmable watchdog window select bits (WDTWIN<1:0>) setting as shown in Figure 3-3. The bit settings are as follows:

- `11` = WDT window is 25% of the WDT period
- `10` = WDT window is 37.5% of the WDT period
- `01` = WDT window is 50% of the WDT period
- `00` = WDT window is 75% of the WDT period

If the Watchdog Timer is cleared before the allowed window, a system Reset is generated immediately.

The Windowed mode is useful for resetting the device during unexpectedly quick or slow execution of a critical portion of the code.

Figure 3-2: Windowed WDT

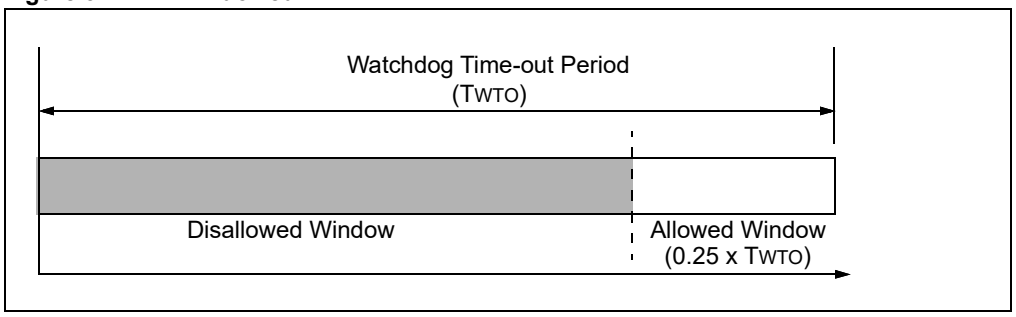
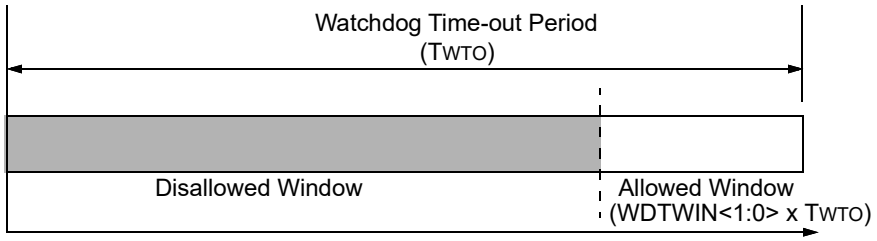


Figure 3-3: Programmable Windowed WDT



Note: The programmable windowed WDT feature is available on selected devices. Refer to the specific device data sheet for availability of this feature.

3.3 Watchdog Time-out Period Selection

The watchdog time-out period is selected by programming the prescaler and postscaler dividers.

The prescaler divider ratio is determined by the Prescaler Selection bit (WDTPRE) in the WDT Configuration register (FWDT<4>).

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler divider ratio is determined by the Postscaler Selection bits (WDTPOST<3:0>) in the WDT Configuration register (FWDT<3:0>), which provides 16 settings (from 1:1 to 1:32,768).

The WDT time-out period can be calculated using Equation 3-1, and the WDT time-out period with window option can be calculated using Equation 3-2. The WDT period configurations for WDT time-out period and WDT time-out period with window option are provided in Table 3-1.

Equation 3-1: WDT Time-out Period

$$T_{WTO} = (N1) \times (N2) \times (T_{LPRC})$$

Where:

$N1$ = Prescaler divider ratio (see Table 3-1)

$N2$ = Postscaler divider ratio (see Table 3-1)

T_{LPRC} = LPRC clock period

Equation 3-2: WDT Time-out Period with Window Option

$$T_{WTO} = (N1) \times (N2) \times (T_{LPRC}) \times (WDTWIN<1:0>)$$

Where:

$N1$ = Prescaler divider ratio (see Table 3-1)

$N2$ = Postscaler divider ratio (see Table 3-1)

T_{LPRC} = LPRC clock period

Table 3-1: WDT Period Configurations

Postscaler Settings (WDTPOST<3:0>)	Postscaler Ratio (N2)(1)	5-bit Prescaler Time-out Period(2,3)	5-bit Prescaler Time-out Window(5)	7-bit Prescaler Time-out Period(2,4)	7-bit Prescaler Time-out Window(5)
0000	1:1	1 ms	0.75 ms	4 ms	3 ms
0001	1:2	2 ms	1.5 ms	8 ms	6 ms
0010	1:4	4 ms	3 ms	16 ms	12 ms
0011	1:8	8 ms	6 ms	32 ms	24 ms
0100	1:16	16 ms	12 ms	64 ms	48 ms
0101	1:32	32 ms	24 ms	128 ms	96 ms
0110	1:64	64 ms	48 ms	256 ms	192 ms
0111	1:128	128 ms	96 ms	512 ms	384 ms
1000	1:256	256 ms	192 ms	1.024s	0.768s
1001	1:512	512 ms	384 ms	2.048s	1.536s
1010	1:1024	1.024s	0.768s	4.096s	3.072s
1011	1:2048	2.048s	1.536s	8.192s	6.144s
1100	1:4096	4.096s	3.072s	16.384s	12.288s
1101	1:8192	8.192s	6.144s	32.768s	24.576s
1110	1:16384	16.384s	12.288s	65.536s	49.152s
1111	1:32768	32.768s	24.576s	131.072s	98.304s

Note 1: The postscaler clock is derived from the 5-bit or 7-bit prescaler.

2: Time-out period is based on a sample 32 kHz input clock.

3: The WDT prescaler ratio of 1:32 N1 (WDTPRE = 0) gives a 5-bit prescaler.

4: The WDT prescaler ratio of 1:128 N1 (WDTPRE = 1) gives a 7-bit prescaler.

5: WDTWIN = 00. The WDT window is 75% of the selected WDT period.

> **Note:** The WDT time-out period is directly related to the LPRC Oscillator frequency (32 kHz nominal). Refer to the specific device data sheet for details about the accuracy of the LPRC frequency over temperature and voltage variations.

3.4 Watchdog Timer Reset

The Watchdog Timer is reset in the following circumstances:

- On any device Reset
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the WDT is enabled in software
- On the completion of a clock switch
- By a CLRWDT instruction during normal execution or during the last 25% of the WDT time-out period if WINDIS is '0'

> **Note:** If a WDT time-out occurs while a Run-Time Self-Programming (RTSP) erase or programming operation is in progress, the device will be reset only after the RTSP operation is complete.

3.5 Operation of Watchdog Timer in Sleep and Idle Modes

If enabled, the Watchdog Timer continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes up and code execution continues from where the PWRSAV instruction was executed.

The Watchdog Timer is useful for low-power system designs because it can be used to periodically wake the device from Sleep mode to check the system status and provide action, if necessary. The SWDTEN bit (RCON<5>) is very useful in this respect. If the WDT is disabled during normal operation (FWDTEN = 0), the SWDTEN bit can be used to turn on the WDT just before entering Sleep mode.

4.0 DESIGN TIPS

Question 1: ***The device Resets even though I have inserted a `CLRWDT` instruction in my main software loop.***

Answer: Make sure that the software loop that contains the `CLRWDT` instruction meets the minimum specification of the WDT (not the typical value). Also, make sure that interrupt processing time has been accounted for.

Question 2: ***What should my software do before entering Sleep or Idle mode?***

Answer: Make sure that the sources intended to wake the device have their interrupt enable bits set. In addition, make sure that the particular source of an interrupt can wake the device. Some sources do not function when the device is in Sleep mode.

If the device is to be placed in Idle mode, make sure that the “stop-in-idle” control bit for each peripheral device is properly set. These control bits determine whether the peripheral will continue operation in Idle mode. See the individual peripheral sections of this manual for further details.

Question 3: ***How can I tell which peripheral woke the device from Sleep or Idle mode?***

Answer: You can poll the Interrupt Flag bits for each enabled interrupt source to determine the source of wake-up.

5.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Watchdog Timer and Power-Saving Modes include the following:

Title	Application Note #
Low-Power Design Using PICmicro® Microcontrollers	AN606

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33/PIC24 family of devices.

6.0 REVISION HISTORY

Revision A (September 2009)

This is the initial released version of this document.

Revision B (December 2010)

This revision includes the following updates:

- Added a note at the beginning of the section, which provides information on complementary documentation
- Updated the dsPIC33E references in the entire document as dsPIC33E/PIC24E.
- Added a reference to the VREGSF bit to the bulleted list in **Section 2.2.1 “Sleep Mode”**
- Added a note box with detail regarding RTSP to **Section 3.4 “Watchdog Timer Reset”**
- Added a note box with reference to the specific device data sheet chapter for TVREG, TOST, TLOCK, and TOSCD specifications after **Section Table 2-1: “Oscillator Delay(1,2,3)”**
- Additional formatting changes and minor updates to text have been incorporated throughout the document

Revision C (May 2011)

This revision includes the following updates:

- Updated the third bulleted paragraph in **Section 2.2.1 “Sleep Mode”**
- Added the Watchdog Timer characteristics in **Section 3.0 “Watchdog Timer”**
- Updated cross-references in Equation 3-1
- Removed the WDT prescaler and postscaler divider settings tables
- Added **Section 3.1 “Prescaler/Postscaler”**
- Added Figure 3-3
- Added Equation 3-2
- Added Table 3-1
- Additional formatting changes and minor updates to text have been incorporated throughout the document

Revision D (February 2023)

This revision includes the following updates:

- Applied current Family Reference Manual format
- Updated all dsPIC33E/PIC24E references to dsPIC33/PIC24
- Updated **Section 3.1 “Prescaler/Postscaler”**

NOTES:

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