

KSZ8061 Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the KSZ8061 family of devices, which includes the following:

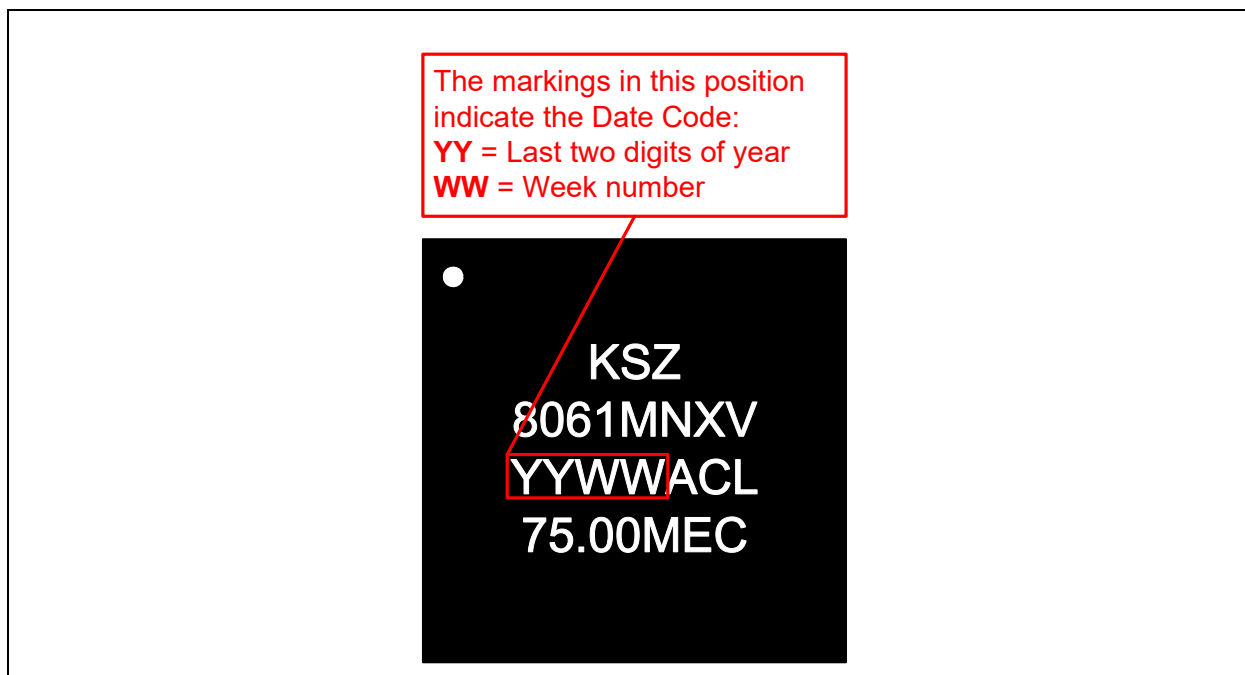
- KSZ8061RNBV
- KSZ8061RNBW
- KSZ8061RNDV
- KSZ8061RNDW
- KSZ8061MNXI
- KSZ8061MNXV
- KSZ8061MNGW

The silicon errata discussed in this document are for silicon with date codes listed in [Table 1](#). The date code can be determined by the device's top marking as indicated in [Figure 1](#). A summary of KSZ8061 silicon errata is provided in [Table 2](#).

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Date Code
KSZ8061RNBV, KSZ8061RNBW, KSZ8061RNDV, KSZ8061RNDW, KSZ8061MNXI, KSZ8061MNXV, KSZ8061MNGW	1447 and newer

FIGURE 1: TOP MARKING DATE CODE INDICATION



Note: The purpose of [Figure 1](#) is to detail the top markings of an example part and highlight the location of the date code. Other top marking values may differ (lot codes, location of manufacture, etc.).

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary
1.	Potential link-up failure when Ethernet cable is connected slowly
2.	Register 15h (RXER Counter) increments with error-free 100BASE-TX received packets
3.	Random stuck logic zero signals on MII/RMII receiving channel
4.	Delay Lock Loop fail to lock to the proper setting

Silicon Errata Issues

Module 1: Potential link-up failure when Ethernet cable is connected slowly

DESCRIPTION

Link-up may not occur properly when the Ethernet cable is initially connected. This issue occurs more commonly when the cable is connected slowly, but it may occur any time a cable is connected.

This issue occurs in the auto-negotiation circuit, and will not occur if auto-negotiation is disabled (which requires that the two link partners be set to the same speed and duplex).

END USER IMPLICATIONS

When this issue occurs, link is not established. Subsequent cable plug/unplug cycles will not correct the issue.

Work Around

There are four approaches to work around this issue:

1. This issue can be prevented by setting bit 15 in MMD device address 1, register 2, prior to connecting the cable or prior to setting the Restart Auto-Negotiation bit in register 0h. The MMD registers are accessed via the indirect access registers Dh and Eh, or via the Micrel EthUtil utility as shown here:
 - If using the EthUtil utility (usually with a Micrel KSZ8061 Evaluation Board), type the following commands:

```
> address 1
> mmd 1
> iw 2 b61a
```
 - Alternatively, write the following registers to write to the indirect MMD register:

```
Write register Dh, data 0001h
Write register Eh, data 0002h
Write register Dh, data 4001h
Write register Eh, data B61Ah
```
2. The issue can be avoided by disabling auto-negotiation in the KSZ8061, either by the strapping option, or by clearing bit 12 in register 0h. Care must be taken to ensure that the KSZ8061 and the link partner will link with the same speed and duplex. Note that the KSZ8061 defaults to full-duplex when auto-negotiation is off, but other devices may default to half-duplex in the event of failed auto-negotiation.
3. The issue can be avoided by connecting the cable prior to powering-up or resetting the KSZ8061, and leaving it plugged in thereafter.
4. If the above measures are not taken and the problem occurs, link can be recovered by setting the Restart Auto-Negotiation bit in register 0h, or by resetting or power cycling the device. Reset may be either hardware reset or software reset (register 0h, bit 15).

PLAN

This erratum will not be corrected in a future revision.

Module 2: Register 15h (RXER Counter) increments with error-free 100BASE-TX received packets

DESCRIPTION

After power-up/reset, the reserved register bit setting for the RXER Counter register is not set to the correct default value. The incorrect bit setting causes the RXER Counter register to increment for 100BASE-TX received packets without symbol errors.

END USER IMPLICATIONS

After power-up/reset, the RXER Counter register does not accurately count received packets with symbol errors, as the counter also increments for error-free receive packets.

Work Around

After device power-up/reset, change MMD Device Address 1h, Register 1Dh from 0010h (default value) to 0110h (new value) by changing bit 8 from the default value of 0 to the new value of 1. This will correct the bit setting for the RXER Counter.

Write the following registers to write to the indirect MMD Device Address Register:

Write register Dh, data 0001h // Set up register address to MMD Device Address 1h

Write register Eh, data 001Dh // Select Register 1Dh of MMD Address 1h

Write register Dh, data 4001h // Set up data to be written to MMD Device Address 1h, Register 1Dh

Write register Eh, data 0110h // Write the new data value to MMD Device Address 1h, Register 1Dh

Note, this workaround increases the RX latency by 40ns.

PLAN

This erratum will not be corrected in a future revision.

Module 3: Random stuck logic zero signals on MII/RMII receiving channel

DESCRIPTION

RMII/MII signal failure may occur in fixed latency mode following a link up with a powered link partner (auto-negotiation or force mode).

END USER IMPLICATIONS

When this issue occurs, a link will still be established but the device's output signal RXC, RXDV, RXDx (MII or RMII mode) are stuck at logic zero. No link partner communications can occur.

Work Around

Configure the device to variable latency mode by setting the register 18h Bit 10 to "1".

PLAN

This erratum will not be corrected in a future revision.

Module 4: Delay Lock Loop fail to lock to the proper setting

DESCRIPTION

The Delay Lock Loop (DLL) used in the receiver can lock to an incorrect value, causing the data to be sampled incorrectly.

END USER IMPLICATIONS

When Auto-Negotiation (AN) is disabled (also known as force mode), there is a chance the PHY will not link and will need to manually re-train the DLL until a link is established. There are three force link-up modes with a link partner where the issue can occur: AN-FORCE, FORCE-AN, and FORCE-FORCE.

Work Around

When Auto-Negotiation is disabled, the following link status algorithm is recommended:

- Read Bit 4 (EN_DET) of register 1Eh – Monitor the energy status of the PHY MDI lines.
- Wait 0.5-3 seconds after Bit 4 is asserted.
- Read Bit 8 (LINK_STATUS) of register 1Eh – Monitor the Link Status of the PHY.
- If the Link Status is high, proceed to normal operation. If the Link Status is low, force the PHY to re-train.
 - Write 0020h to register 11h – This stops the PHY from attempting to Link.
 - Write 0x2100 (for FORCE-FORCE) or 0x3100 (for AN-FORCE or FORCE-AN) to register 0 – This configures the PHY to the proper speed and link setting.
 - Wait 0.5 seconds for PHY DLL block to reset.
 - Write 0x0000 to register 11h – This restarts the PHY attempting to link.
- Repeat until Link Status goes high.

PLAN

This erratum will not be corrected in a future revision.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000688C (07-29-21)	Module 3. and 4.	Added new errata.
DS80000688B (03-29-18)	Module 2.	Added new erratum.
DS80000688A (01-07-16)	All	Initial release

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