SmartFusion® 2 SoC FPGAs

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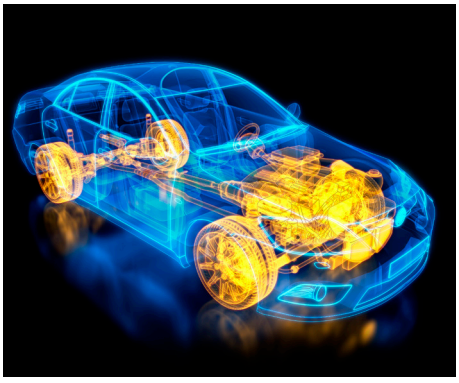
SmartFusion2 SoC FPGAs

More Resources in Low-Density Devices with the Lowest Power, Proven Security and Exceptional Reliability

These devices are ideal for general-purpose functions such as Gigabit Ethernet or dual PCI® Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. Microchip FPGAs are used by customers in the communications, industrial, medical, defense and aviation markets.

- Communications
- Industrial
- Defense
- Automotive



SmartFusion2 Advantages

More Resources in Low-Density Devices

- Arm® Cortex®-M3 with embedded flash
- PCIe Gen2 support in 10K LE
- Comprehensive microcontroller subsystem

With Clear Advantages

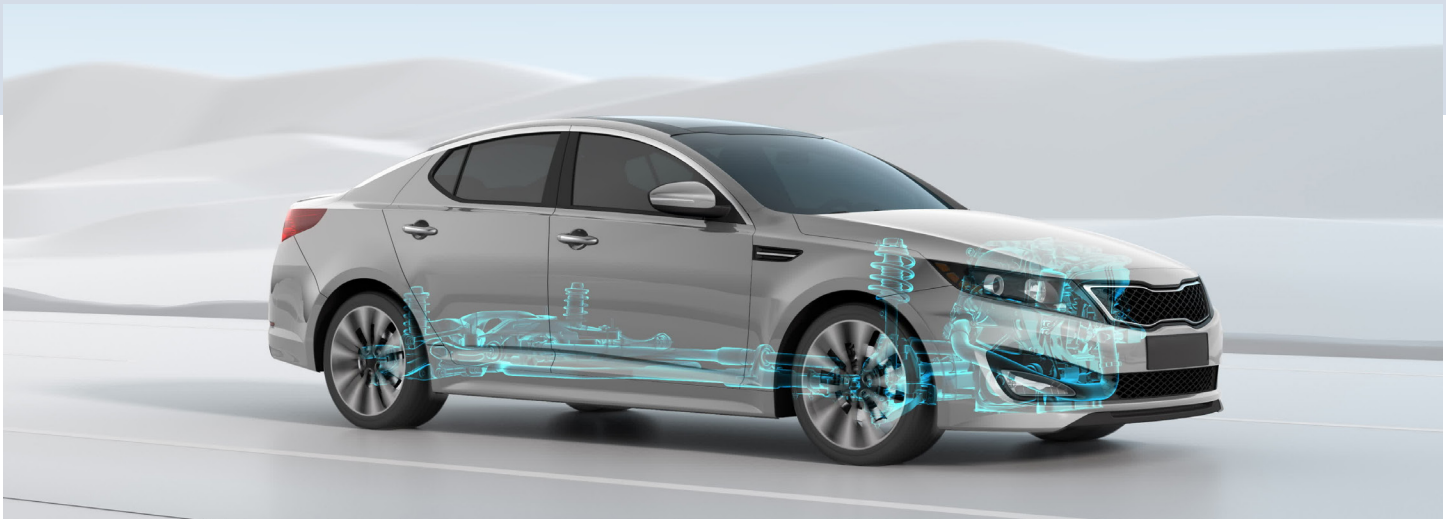
- Lowest Power
  - Reduces total power by up to 50%
  - 70 mW per 5G SERDES (PCIe Gen2)
- Proven Security
  - Protection from overbuilding and cloning
  - Secure boot for FPGA and processors
- Exceptional Reliability
  - SEU immune zero FIT flash FPGA configuration
  - Reliable safety-critical and mission-critical systems

Integration

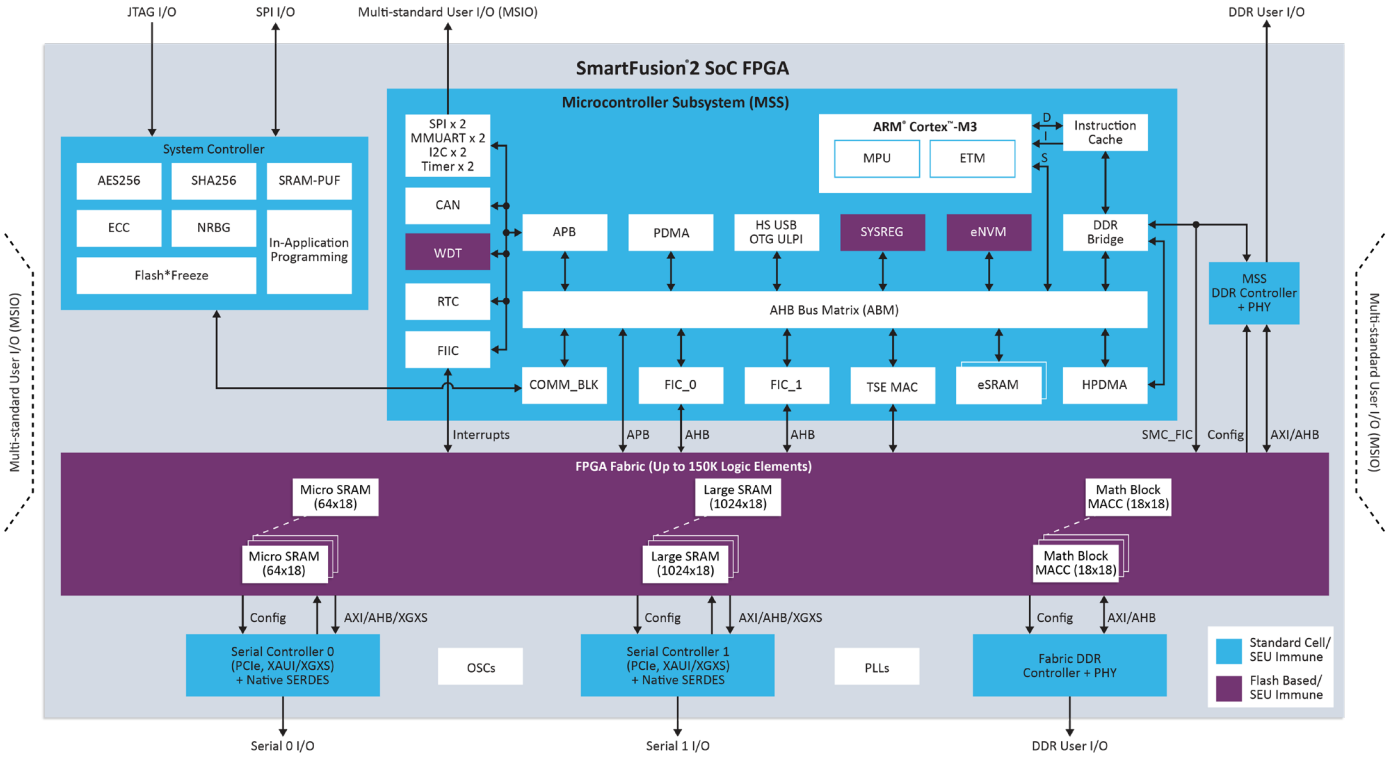
Low Power

Reliability

Security



- SmartFusion2 FPGA Architecture
- SmartFusion2 SoC FPGAs
- SmartFusion2 SoC FPGAs offer 5K–150K LEs with a 166 MHz Arm Cortex-M3 processor, including ETM and instruction cache with on-chip eSRAM and eNVM, and a complete microcontroller subsystem with extensive peripherals, including CAN, TSE and USB.
- Up to 16× transceiver lanes
- PCIe Gen2, XAUI/XGXS+, generic (EPCS) mode at 3.2G
- Up to 150K LEs, 5 Mb SRAM, 4 Mb eNVM
- Hard 667 Mbps DDR2/3 controllers
- Integrated DSP processing blocks
- Power as low as 7 mW standby, typical
- DPA-hardened, AES256, SHA256, on-demand NVM data integrity check
- SEU-protected-tolerant memories: eSRAMs, DDR bridges



AES Advanced Encryption Standard

AHB Advanced High-Performance Bus

APB Advanced Peripheral Bus

AXI Advanced eXtensible Interface

COMM_BLK Communication Block

DDR Double Data Rate

DPA Differential Power Analysis

ECC Elliptical-Curve Cryptography

EDAC Error Detection and Correction

ETM Embedded Trace Macrocell

FDDR DDR2/3 Controller in FPGA Fabric

FIC Fabric Interface Controller

FIIC Fabric Interface Interrupt Controller

HS USB OTG High-Speed USB (2.0) On-The-Go

IAP In-Applications Programming

MACC Multiple-Accumulate

MDDR DDR2/3 Controller in MSS

MMUART Multi-Mode UART

MPU Memory Protection Unit

MSS Microcontroller Subsystem

SECDED Single Error Correct Double Error Detect

SEU Single Event Upset

SHA Secure Hashing Algorithm

SMC_FIC Soft Memory Controller

TSE Tiple Speed Ethernet (10/100/1000 Mbps)

ULPI UTMI + Low Pin Interface

UTMI USB 2.0 Transceiver Macrocell Interface

WDT Watchdog Timer

XAUI 10 Gbps Attachment Unit Interface

XGMII 10 Gigabit Media Independent Interface

XGXS XGMII Extended Sublayer

PCI EXPRESS®

HI-SPEED CERTIFIED USB On-The-Go

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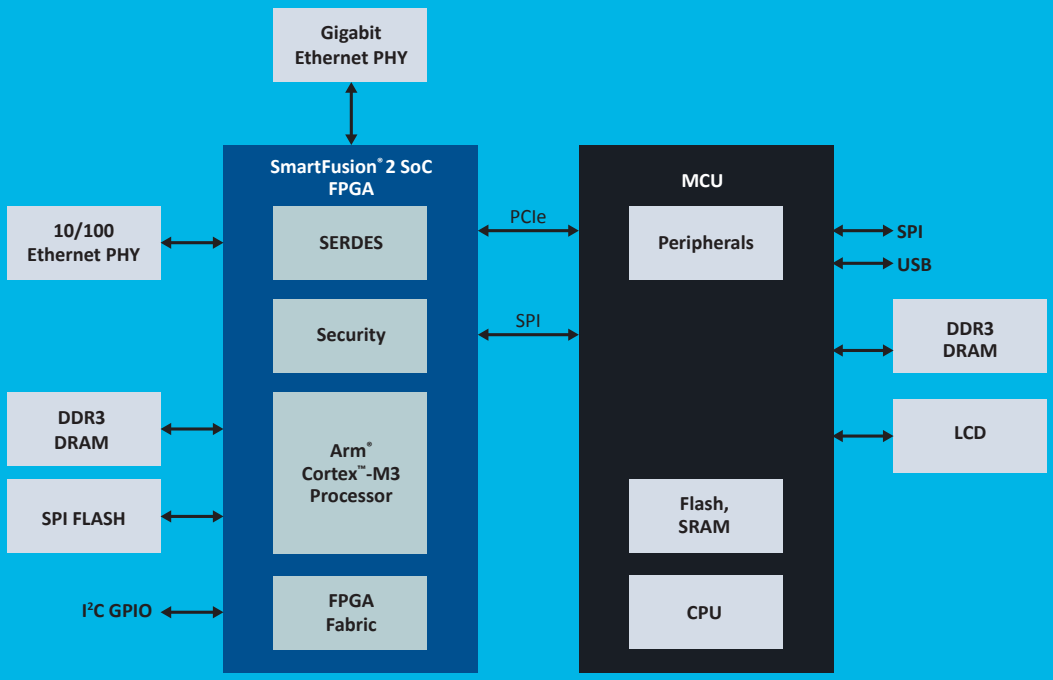
Cortex Intelligent Processors by ARM®

General-Purpose Applications

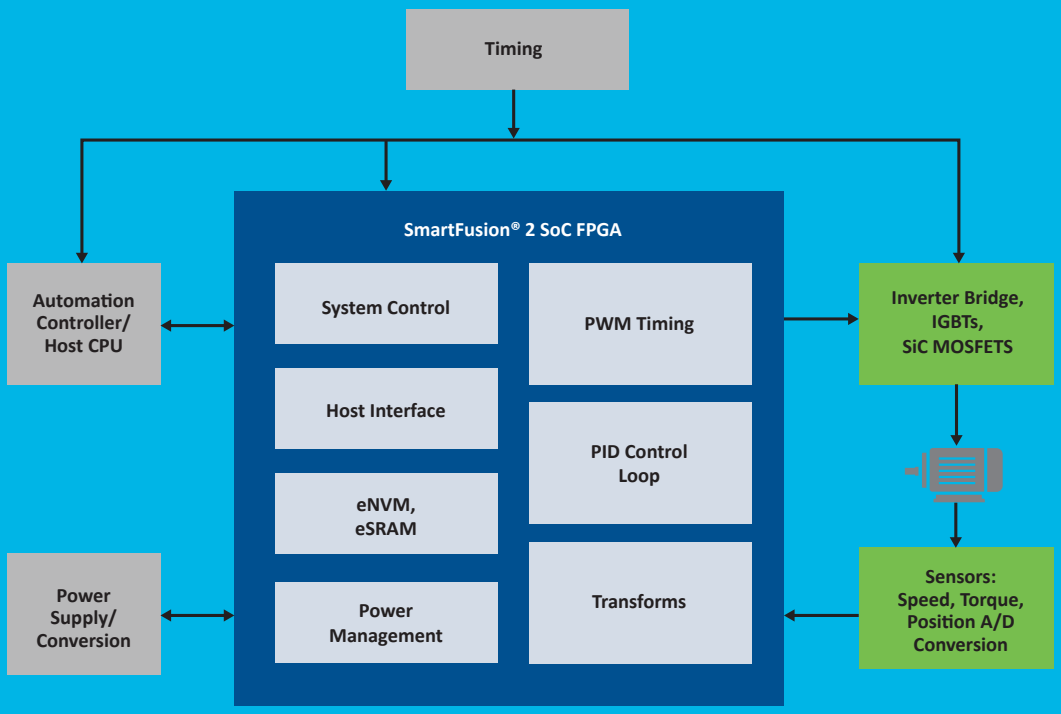
PCIe 1G Control Plan

- PCIe Gen2 in 10K LE devices with I/O expansion



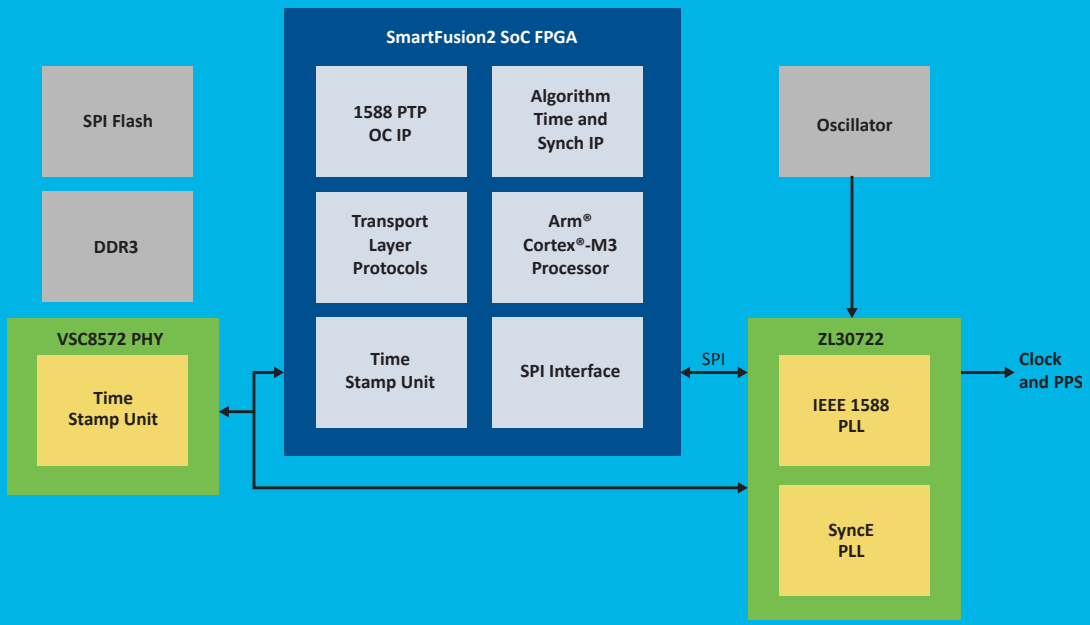
Multi-Axis Motor Control

- Deterministic and secure multi-axis/high-RPM solutions
- Motor-control IP and development kit



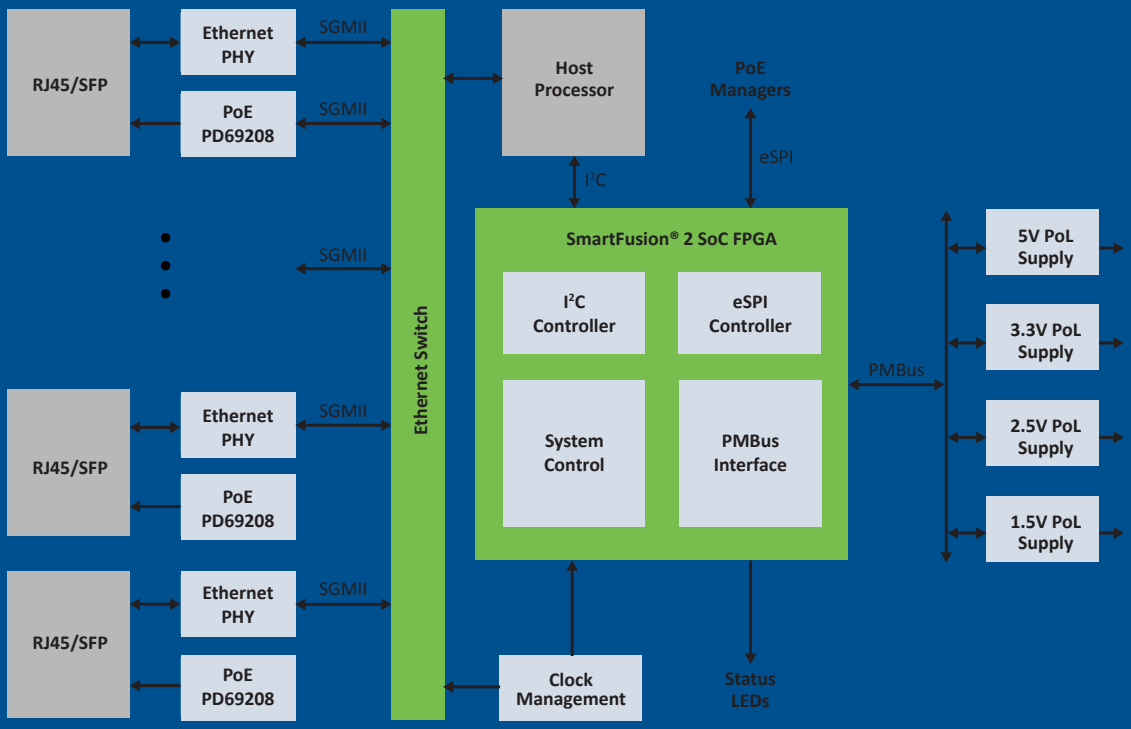
IEEE 1588 Parent/Child

- IEEE 1588 and small form factor, Cortex-M3, low power



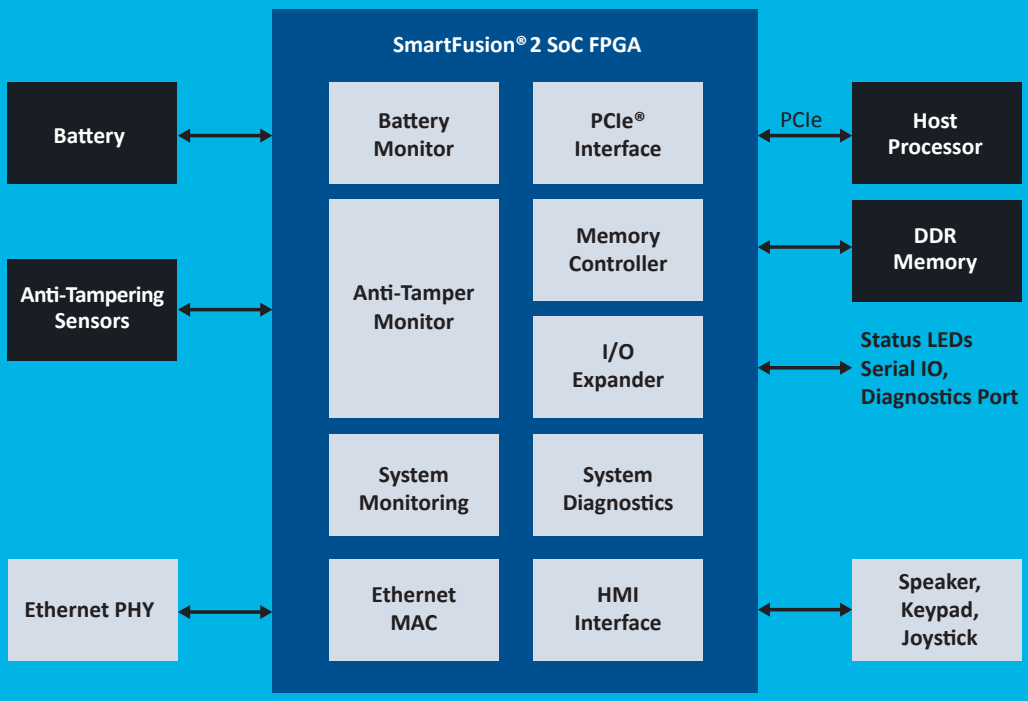
Board Initialization

- PMBus, instant-on and MSS peripherals



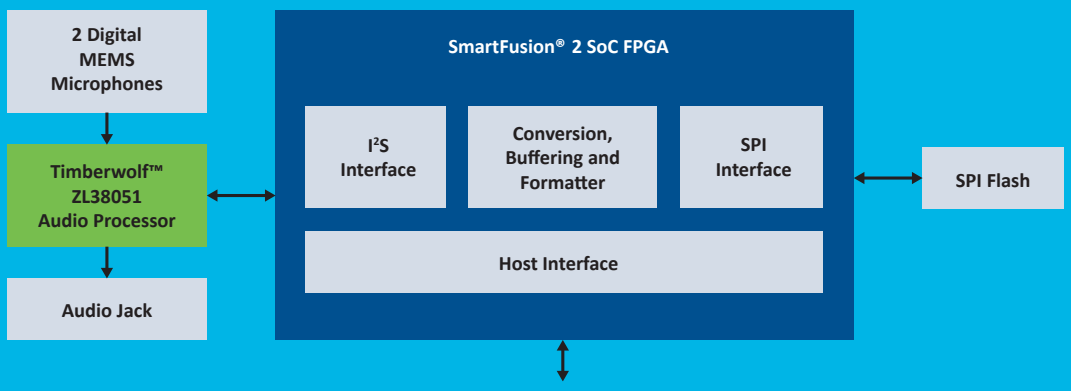
Secure Connectivity: Gaming

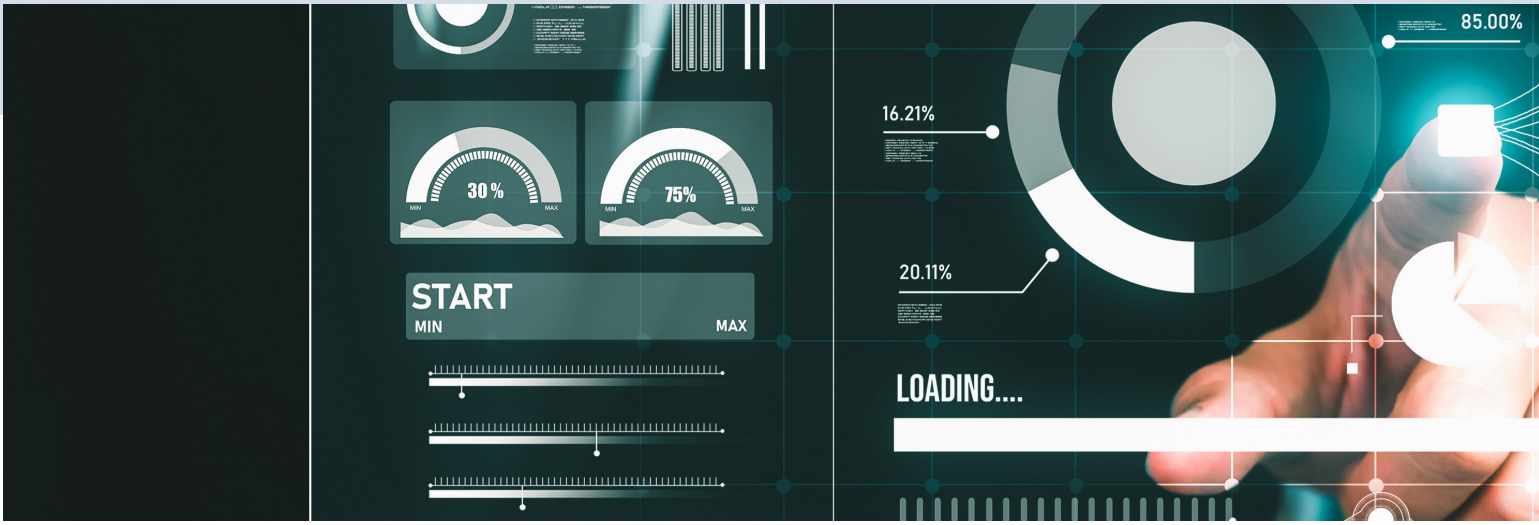
- Security, anti-tamper and Ethernet MAC low power



Audio Processing, Storage and Retrieval

- I^2S and SPI bridge allows multiple audio recordings and playbacks



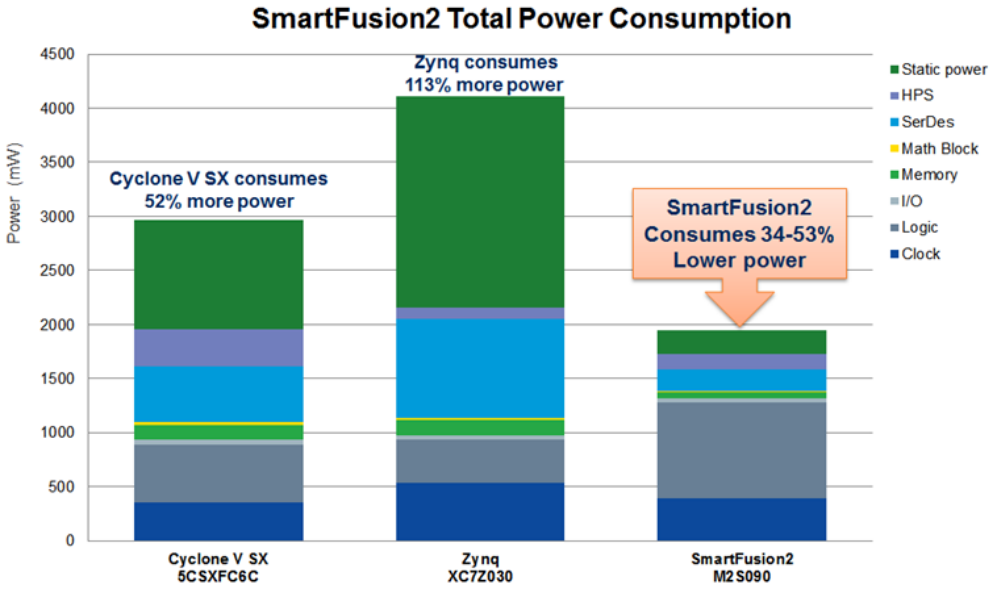


Clear Advantages

Low Power

SmartFusion2 Reduces Total Power

- Flash FPGAs deliver lowest power without sacrificing performance
- 70 mW per 5G SERDES (PCIe Gen2)
- Flash*Freeze ultra-low-power mode 12 mW



Proven Security

Protect Systems from Over-building and Cloning

- HSMs protection from overbuilding
- DPA countermeasures protect bitstream from cloning
- Only FPGA vendor with validated DPA countermeasures
- Secure boot for FPGAs and processors

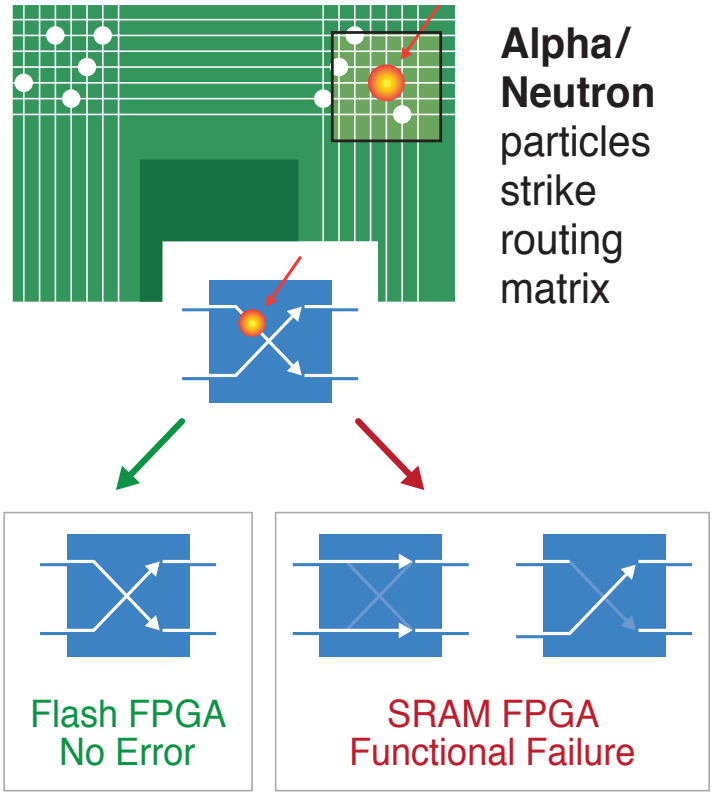
LICENSED DPA COUNTERMEASURES™

DPA™

Exceptional Reliability

- Error-free SEU immune fabric configuration
- No scrubbing required
- All SoC memory SEU-protected
- Built-in error detection and correction
- SEU-tolerant implementation
- Devices deployed in safety-critical and mission-critical systems

SRAM Configuration Failures



SmartFusion2 Design Resources

Design Resources

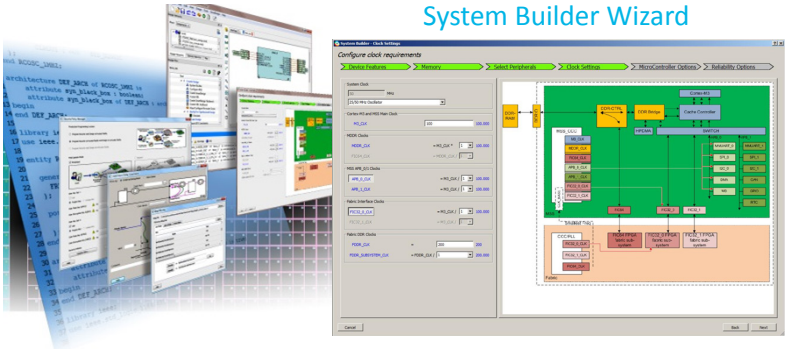
The Libero® SoC Design Suite enables high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microchip's power-efficient SmartFusion2, IGLOO®2, and RTG4™ FPGAs. The suite integrates industry-standard Synopsys Synplify Pro® synthesis and Siemens EDA (Mentor Graphics) simulation tools with best-in-class constraints management, debug capabilities, and secure production programming support.

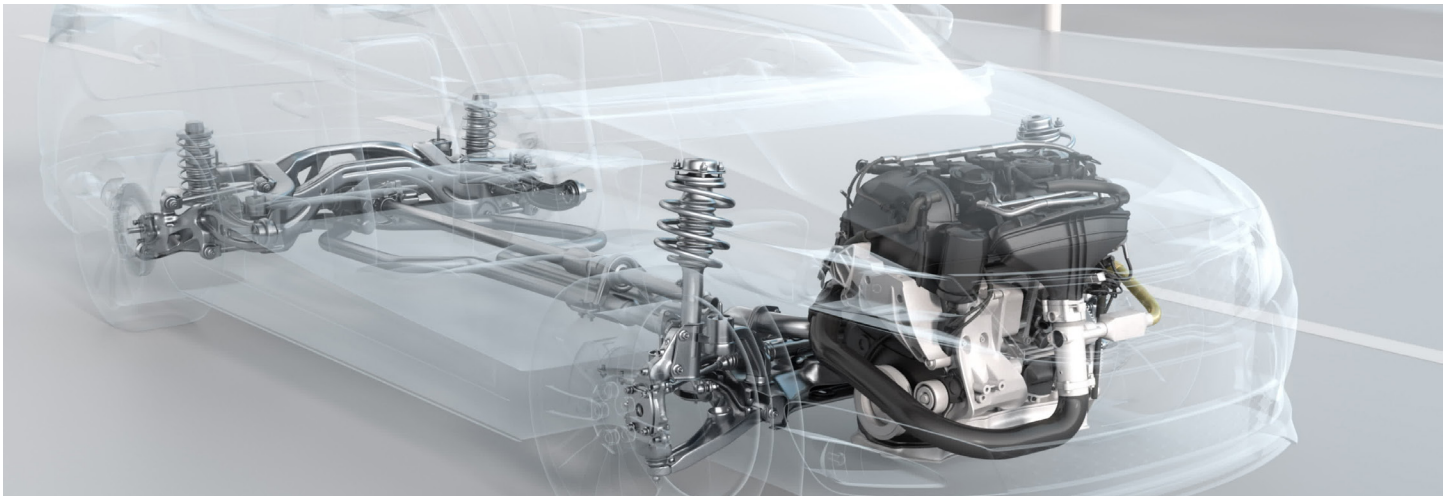
Libero SoC Design Suite provides a comprehensive design flow including traditional FPGA design flow, embedded design flow and graphical configurators. FPGA design flow is the standard VLSI design flow starting from design entry till programing and debug. The embedded design flow enables development of embedded processing solutions for high performance and high reliability applications using low-power SoC FPGAs and FPGAs. It provides comprehensive development environment to build embedded solutions using hard core and soft core processors. Graphical configurators provide a user friendly design entry approach for various peripherals, applications and solutions.

For more information, please see the following website: https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions

Software IDE Features	SoftConsole	Keil MDK	IAR Embedded Workbench®
Free Versions	Stand alone with Microchip	32K Code Limited	32K Code Limited
Available from Vendor	N/A	Full Version	Full Version
Compiler	GNU GCC	RealView® C/C++	IAR Arm® Compiler
Debugger	GDB Debug	µVision Debugger	C-SPY® Debugger
Instruction Set Simulator	No	µVision Simulator	Yes
Debug Hardware	FlashPro4/5/6	ULINK®2 or ULINK-ME	J-LINK™ or J-LINK Lite
Trace Capability	No	ULINKpro	JTAGjet-Trace

System Builder Wizard





Intellectual Property

Microchip enhances your design productivity by providing an extensive suite of proven and optimized IP cores for use with Microchip FPGAs. Our extensive suite of IP cores covers all key markets and applications. Our cores are organized into Microchip-developed DirectCores and third-party-developed CompanionCores. Most DirectCores are available for free within our Libero tool suite and include common communications interfaces, peripherals and processing elements. https://www.microchip.com/en-us/products/fpgas-and-plds/ip-core-tools

Functionality	DirectCore Examples
Connectivity	UART, 16550, 429, PCI, JESD204B
DSP	CIC, FFT, FIR, CORDIC, RS
Memory Controller	FIFO, DDR, QDR, SDR, MemCtrl, MMC
Processor	8051, 8051s, ARM7TDMI, RISC-V
Ethernet	MII, RGMII, GMII, SGMII, TSE
Security	DES, 3DES, AES, SHA

Functionality	CompanionCore Examples
Connectivity	CAN, CAN FD, PCIe, VME
DSP	FFT, JPEG, RS, DVBMOD
Memory Controller	SDRAMDDR, Flash, SD
Processor	80188, 80186, LEON3, 6809
Security	MD5, ARC4, RNG, ZUC, AES, SHA, 802.1ae (MACSec)

SmartFusion2 Product Family

	Features	M2S005	M2S010	M2S025	M2S050	M2S060	M2S090	M2S150
Logic/DSP	Maximum Logic Elements (4LUT + DFF)	6,060	12,084	27,696	56,340	56,520	86,316	146,124
	Math Blocks (18x18)	11	22	34	72	72	84	240
	Fabric Interface Controllers (FICs)	1			2	1		2
	PLLs and CCCs	2		6				8
	Security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
	Cortex®-M3 + Instruction Cache	Yes						
MSS	eNVM (KBytes)	128	256				512	
	eSRAM (KBytes)	64						
	eSRAM (KBytes) Non-SECDED	80						
	CAN, 10/100/1000 Ethernet, HS USB	1 Each						
	Multi-Mode UART, SPI, I²C Timer	2 Each						
Fabric Memory	LSRAM 18K Block	10	21	31	69		109	236
	uSRAM 1K Blocks	11	22	34	72		112	240
	Total RAM (Kbits)	191	400	592	1,314		2,074	4,488
High Speed	DDR Controllers (count x width)	1 x 18			2 x 36	1 x 18		2 x 36
	SERDES Lanes	0	4		8	4		16
	PCIe® End Point	0	1		2			4
User I/O	MSIO (3.3V)	115	123	157	139	279	309	292
	MSIOD (2.5V)	28	40		62	40		106
	DDRIO (2.5V)	66	70		176	76		176
	Total User I/Os	209	233	267	377	395	425	574

I/Os Per Package

	Package Options																							
Package type	FCSG158		FCSG325		VFG256		FCSG536		VFG400		FCVG484		TQG144		FGG484		FGG676		VFG784		FGG896		FCG1152	
Pitch (mm)	0.5		0.5		0.8		0.5		0.8		0.8		0.5		1.0		1.0		0.8		1.0		1.0	
Length × Width (mm)	9 × 9		11 × 11		14 × 14		16 × 16		17 × 17		19 × 19		20 × 20		23 × 23		27 × 27		23 × 23		31 × 31		35 × 35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005 (S)					161	–			171	–			84	–	209	–								
M2S010 (T/TS)[1,2]					138	2			195	4			84	–	233	4								
M2S025 (T/TS)[1]	82	1	180	2	138	2			207	4					267	4								
M2S050 (T/TS)[1]			200	2					207	4					267	4					377	8		
M2S060 (T/TS)[1]			200	2					207	4					267	4	287	4	395	4				
M2S090 (T/TS)[1,3,4]			180	4											267	4	425	4						
M2S150 (T/TS)[5]							293	4			248	4											574	16

1. Mil Temp 010/025/050/060/090 devices are only available in the FG(G)484 package. Mil temp 150 device is available in FC(G)1152 and FCV484
2. M2S010S device is only available in TQG144 package. M2GL010 (T/TS) devices are not available in TQ(G)144 package.
3. 090 FCS(G)325 is 11x13.5 pkg dimension.

Highlighted devices can migrate vertically in the same package

Automotive Grade2 parts (-40°C to +125°C Tjn)

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