Parallel Master Port (PMP)

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.

Please consult the note at the beginning of the **"Parallel Master Port (PMP)"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

This document supersedes the following dsPIC33/PIC24 Family Reference Manual sections:

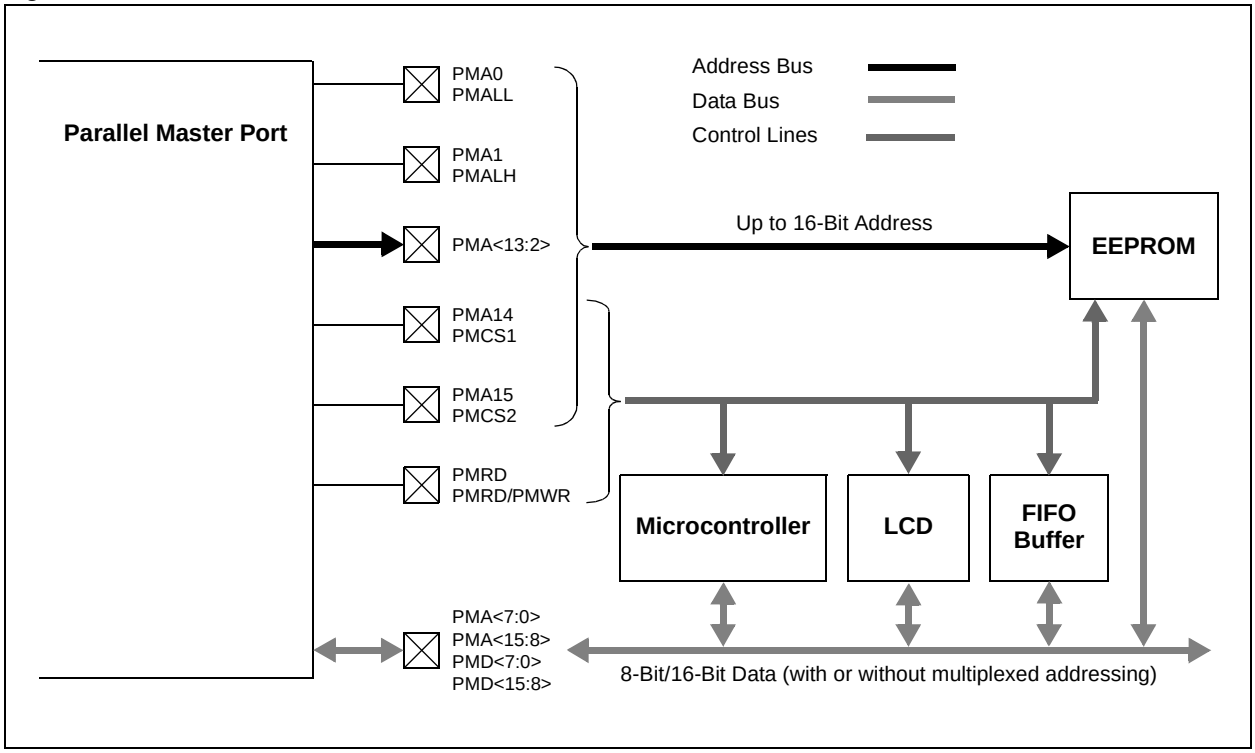
DS Number	Section Number	Title
DS39713	13	PIC24F FRM, Parallel Master Port (PMP)

1.0 INTRODUCTION

The Parallel Master Port (PMP) is a parallel 8-bit/16-bit I/O module specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interfaces to parallel peripherals vary significantly, the PMP module is highly configurable. The key features of the PMP module include:

- Master and Slave Operating Modes
- Up to 16 Programmable Address Lines
- Up to Two Chip Select Lines
- Programmable Strobe Options:
  - Individual read and write strobes or read/write strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
  - Address support
  - 4 bytes deep, auto-incrementing buffer
- Schmitt Trigger or TTL Input Buffers
- Programmable Wait States
- Dual Buffer Mode with Separate Read and Write Registers
- Read Initiate Control

Figure 1-1: PMP Module Pinout and Connections to External Devices



2.0 CONTROL REGISTERS

Table 2-1 provides a brief summary of all PMP module-related registers. Corresponding registers appear after the summary with a detailed description of each bit.

Table 2-1: PMP Special Function Register Summary

Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PMCON	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP
PMCONH	—	—	—	—	—	—	—	—	RDSTART	—	—	—	—	—	DUALBUF	—
PMMODE	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>	
PMADDR	CS2(1)	CS1(1)	ADDR<13:0>													
	ADDR15	ADDR14														
PMDOUT1	DATAOUT<15:0>															
PMDOUT2	DATAOUT<31:16>															
PMDIN1	DATAIN<15:0>															
PMDIN2	DATAIN<31:16>															
PMAEN	PTEN<15:0>															
PMSTAT	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
PMWADDR	WCS2(2)	WCS1(2)	WADDR<13:0>													
	WADDR15	WADDR14														
PMRADDR	RCS2(3)	RCS1(3)	RADDR<13:0>													
	RADDR15	RADDR14														
PMRDIN	RDATAIN<15:0>															

Legend: — = unimplemented, read as '0'.

Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

2: The use of these pins as PMA15/PMA14 or WCS2/WCS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

3: The use of these pins as PMA15/PMA14 or RCS2/RCS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

Register 2-1: PMCON: Parallel Master Port Control Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
CSF<1:0>(1)		ALP(1)	CS2P(1)	CS1P(1)	—	WRSP	RDSP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** Parallel Master Port Enable bit
1 = PMP is enabled
0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** PMP Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = All 16 bits of address are multiplexed with the 16 bits of data (PMPA<15:0>/PMPD<15:0>) using two phases
10 = All 16 bits of address are multiplexed with the lower 8 bits of data (PMPA<15:8>/PMPA<7:0>/PMPD<7:0>) using three phases
01 = Lower 8 bits of address are multiplexed with lower 8 bits of data (PMPA<7:0>/PMPD<7:0>)
00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffers

bit 9 **PTWREN:** PMP Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** PMP Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port is enabled
0 = PMRD/PMWR port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(1)
11 = Reserved
10 = PMCS2 and PMCS1 function as Chip Select
01 = PMCS2 functions as Chip Select, PMCS1 functions as address bit
00 = PMCS2 and PMCS1 function as address bits

bit 5 **ALP:** Address Latch Polarity bit(1)
1 = Active-high ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)
0 = Active-low (PMALL and PMALH)

bit 4 **CS2P:** Chip Select 2 Polarity bit(1)
1 = Active-high
0 = Active-low

Note 1: These bits have no effect when their corresponding pins are used as address lines.

Register 2-1: PMCON: Parallel Master Port Control Register (Continued)

bit 3 **CS1P:** Chip Select 1 Polarity bit(1)
1 = Active-high
0 = Active-low

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master Mode 2 (MODE<1:0> (PMMODE<9:8>) = 00, 01, 10):
1 = Write strobe is active-high (PMWR)
0 = Write strobe is active-low ($\overline{\text{PMWR}}$)
For Master Mode 1 (MODE<1:0> (PMMODE<9:8>) = 11):
1 = Enables strobe active-high (PMENB)
0 = Enables strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave Modes and Master Mode 2 (MODE<1:0> (PMMODE<9:8>) = 00, 01, 10):
1 = Read strobe is active-high (PMRD)
0 = Read strobe is active-low ($\overline{\text{PMRD}}$)
For Master Mode 1 (MODE<1:0> (PMMODE<9:8>) = 11):
1 = Read/write strobe is active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe is active-low ($\overline{\text{PMRD}}$/$\overline{\text{PMWR}}$)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

Register 2-2: PMCONH: Parallel Master Port Control High Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W/HC-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
RDSTART(1)	—	—	—	—	—	DUALBUF	—
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **RDSTART:** Start a Read on PMP Bus bit(1)
- 1 = Starts a read cycle on the PMP bus
- 0 = No effect

bit 6-2 **Unimplemented:** Read as ‘0’

bit 1 **DUALBUF:** PMP Dual Read/Write Buffers Enable bit (valid in Master mode only)
- 1 = PMP uses separate registers for reads and writes (PMRADDR, PMDINx, PMWADDR, PMDOUTx)
- 1 = PMP uses legacy registers (PMADDR, PMDATA)

bit 0 **Unimplemented:** Read as ‘0’

Note 1: This bit is cleared by HW at the end of the read cycle when BUSY (PMMODE<15>) = 0.

Register 2-3: PMMODE: Parallel Master Port Mode Register

R/HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAITB<1:0>(1)		WAITM<3:0>(1)				WAITE<1:0>(1)	
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **BUSY:** Busy bit (Master mode only)
1 = Port is busy
0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Reserved, do not use
10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable Slave mode only)
01 = Interrupt generated at the end of the read/write cycle
00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
11 = Slave mode read and write buffers auto-increment (MODE<1:0> (PMMODE<9:8>) = 00 only)
10 = Decrements ADDR<15:0> by 1 every read/write cycle(2,4)
01 = Increments ADDR<15:0> by 1 every read/write cycle(2,4)
00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-Bit Mode bit
1 = 16-Bit Mode: A read or write to the Data register invokes a single 16-bit transfer
0 = 8-Bit Mode: A read or write to the Data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** PMP Mode Select bits
11 = Master Mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>)(3)
10 = Master Mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>)(3)
01 = Enhanced Slave mode, controls signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)
00 = Legacy Parallel Slave Port, controls signals (PMRD, PMWR, PMCS and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)
11 = Data Wait of 4 TP; multiplexed address phase of 4 TP
10 = Data Wait of 3 TP; multiplexed address phase of 3 TP
01 = Data Wait of 2 TP; multiplexed address phase of 2 TP
00 = Data Wait of 1 TP; multiplexed address phase of 1 TP **(default)**

Note 1: When WAITM<3:0> = 0000, the WAITBx and WAITEx bits are ignored and forced to 1 TP (peripheral clock) cycle for a write operation; WAITBx = 1 TP cycle, WAITEx = 0 TP cycles for a read operation.

2: Address bits, A15 and A14, are not subject to auto-increment/decrement if configured as Chip Select, CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

4: The PMADDR register is always incremented/decremented by 1 regardless of the transfer data width.

Register 2-3: PMMODE: Parallel Master Port Mode Register (Continued)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits(1)
1111 = Wait of 16 TP
•
•
•
0001 = Wait of 2 TP
0000 = Wait of 1 TP **(default)**

bit 1-0 **WAITE<1:0>:** Data Hold After Read/Write Strobe Wait States bits(1)
11 = Wait of 4 TP
10 = Wait of 3 TP
01 = Wait of 2 TP
00 = Wait of 1 TP **(default)**
For Read Operations:
11 = Wait of 3 TP
10 = Wait of 2 TP
01 = Wait of 1 TP
00 = Wait of 0 TP **(default)**

Note 1: When WAITM<3:0> = 0000, the WAITBx and WAITEx bits are ignored and forced to 1 TP (peripheral clock) cycle for a write operation; WAITBx = 1 TP cycle, WAITEx = 0 TP cycles for a read operation.
2: Address bits, A15 and A14, are not subject to auto-increment/decrement if configured as Chip Select, CS2 and CS1.
3: These pins are active when MODE16 = 1 (16-bit mode).
4: The PMADDR register is always incremented/decremented by 1 regardless of the transfer data width.

Register 2-4: PMADDR: Parallel Master Port Address Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS2(1)	CS1(1)	ADDR<13:8>					
ADDR15(1)	ADDR14(1)						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADDR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CS2:** Chip Select 2 bit(1)
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive (ADDR15 function is selected)

bit 15 **ADDR15:** Target Address bit 15(1)

bit 14 **CS1:** Chip Select 1 bit(1)
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive (ADDR14 function is selected)

bit 14 **ADDR14:** Target Address bit 14(1)

bit 13-0 **ADDR<13:0>:** Target Address bits

Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

Register 2-5: PMDOUT1: Parallel Master Port Data Output Low Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **DATAOUT<15:0>:** Output Data Port bits
These bits are for 8-bit read operations in Slave mode and write operations for Dual Buffer Master mode.

Register 2-6: PMDOUT2: Parallel Master Port Data Output High Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAOUT<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **DATAOUT<31:16>:** Output Data Port bits
These bits are for 8-bit write operations in Slave mode.

Register 2-7: PMDIN1: Parallel Master Port Data Input/Output Low Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAIN<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **DATAIN<15:0>:** Input/Output Data Port bits

These bits are for 8-bit or 16-bit read/write operations in Master mode and are the input data port for 8-bit write operations in Slave mode.

Register 2-8: PMDIN2: Parallel Master Port Data Input/Output High Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAIN<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATAIN<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **DATAIN<31:16>:** Input/Output Data Port bits

These bits are for 8-bit write operations in Slave mode.

Register 2-9: PMAEN: Parallel Master Port Pin Enable Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN<15:14>		PTEN<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN<7:2>						PTEN<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **PTEN<15:14>:** PMCSx Strobe Enable bits
1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1(1)
0 = PMA15 and PMA14 function as port I/Os

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/Os

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
0 = PMA1 and PMA0 pads function as port I/Os

Note 1: The use of these pins as address or Chip Select lines is selected by the CSF<1:0> bits (PMCON<7:6>).

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

Register 2-10: PMSTAT: Parallel Master Port Status Register (Slave modes only)

R-0	R/W-0	U-0	U-0	R-0	R-0	R-0	R-0
IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
bit 15							bit 8

R-1	R/W-0	U-0	U-0	R-1	R-1	R-1	R-1
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the writable Input Buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
0 = No overflow occurred
This bit is set (= 1) in hardware; it can only be cleared (= 0) in software.

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IB<3:0>F:** Input Buffer x Status Full bits
1 = Input buffer contains data that has not been read (reading buffer will clear this bit)
0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty output byte buffer (must be cleared in software)
0 = No underflow occurred
This bit is set (= 1) in hardware; it can only be cleared (= 0) in software.

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OB<3:0>E:** Output Buffer x Status Empty bits
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains data that has not been transmitted

Register 2-11: PMWADDR: Parallel Master Port Write Address Register(2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCS2(1)	WCS1(1)	WADDR<13:8>					
WADDR15(1)	WADDR14(1)						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WADDR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **WCS2:** Chip Select 2 bit(1)
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive (WADDR15 function is selected)

bit 15 **WADDR15:** Target Write Address bit 15(1)

bit 14 **WCS1:** Chip Select 1 bit(1)
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive (WADDR14 function is selected)

bit 14 **WADDR14:** Target Write Address bit 14(1)

bit 13-0 **WADDR<13:0>:** Target Write Address bits

Note 1: The use of these pins as PMA15/PMA14 or WCS2/WCS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

2: This register is only used when the DUALBUF bit (PMCONH<1>) is set to '1'.

Register 2-12: PMRADDR: Parallel Master Port Read Address Register(2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RCS2(1)	RCS1(1)	RADDR<13:8>					
RADDR15(1)	RADDR14(1)						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RADDR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **RCS2:** Chip Select 2 bit(1)
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive (RADDR15 function is selected)

bit 15 **RADDR15:** Target Read Address bit 15(1)

bit 14 **RCS1:** Chip Select 1 bit(1)
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive (RADDR14 function is selected)

bit 14 **RADDR14:** Target Read Address bit 14(1)

bit 13-0 **RADDR<13:0>:** Target Read Address bits

Note 1: The use of these pins as PMA15/PMA14 or RCS2/RCS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

2: This register is only used when the DUALBUF bit (PMCONH<1>) is set to '1'.

Register 2-13: PMRDIN: Parallel Master Port Read Input Data Register(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RDATAIN<15:8>(2)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RDATAIN<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RDATAIN<15:0>:** Port Read Input Data bits(2)

Note 1: This register is only used when the DUALBUF bit (PMCONH<1>) is set to '1' and exclusively for reads. If the DUALBUF bit is '0', the PMDIN1 register (Register 2-7) is used for reads instead of PMRDIN.

2: Only used when MODE16 = 1.

3.0 MASTER PORT MODES

In Master modes, the PMP module provides an 8-bit data bus, up to 16 bits of address, and all the necessary control signals to operate a variety of external parallel devices, such as memory devices, peripherals and slave devices. To use the PMP as a master, the module must be enabled (ON = 1) and the mode must be set to one of the two possible Master modes (PMMODE<9:8> = 10 or 11).

There are a variety of parallel devices, each with a corresponding control method. Consequently, the PMP module is designed to accommodate diverse configurations. This flexibility is supplied through the following features:

- 8-Bit and 16-Bit Data Modes on an 8-Bit Data Bus
- Configurable Address/Data Multiplexing
- Up to Two Chip Select Lines
- Up to 16 Selectable Address Lines
- Address Auto-Increment and Auto-Decrement
- Selectable Polarity on All Control Lines
- Configurable Wait States at Different Stages of the Read/Write Cycle

3.1 Parallel Master Port Configuration Options

3.1.1 CHIP SELECTS

Up to two Chip Select lines, PMCS1 and PMCS2, are available for the Master modes of the PMP. The two Chip Select lines are multiplexed with the Most Significant bits (MSbs) of the address bus (PMA14 and PMA15). When a pin is configured as a Chip Select, it is not included in any address auto-increment/decrement. The function of the Chip Select signals is configured using the Chip Select Function bits, CSF<1:0> (PMCON <7:6>). The CS1 and CS2 bits must be set in PMADDR (PMADDR<15:14>) to enable the corresponding Chip Select.

3.1.2 PORT PIN CONTROL

The PMPTTL, PTWREN and PTRDEN bits (PMCON<10:8>), and the PTENx bits (PMAEN<15:0>) allow the user to conserve PMP pins for other functions, and allow flexibility to control the external address. When any one of these bits is set, the associated PMP function is present on its associated pin; when clear, the associated pin reverts to its defined I/O port function.

For the PMA<13:2> pins, setting the corresponding PTENx bit enables the pin as an address pin and drives the corresponding data contained in the PMADDR register. For the pins configured as Chip Select (PMCS1 or PMCS2) with PTEN14 or PTEN15 set, the Chip Select pins drive the inactive state (configured through the CSxP bits in PMCON) when a read/write operation is not being performed. For the pins configured as address latches, the PTEN0 and PTEN1 bits also control the PMALL and PMALH signals. When multiplexing is used, the associated address latch signals should be enabled.

3.1.3 ADDRESS MULTIPLEXING

In either of the Master modes (MODE<1:0>), the user can configure the address bus to be multiplexed together with the data bus by using the ADRMUX<1:0> bits. There are four Address Multiplexing modes available, as shown in Table 3-1. For sample timings of the different Multiplexing modes, see **Section 3.6 “Master Mode Timing”**.

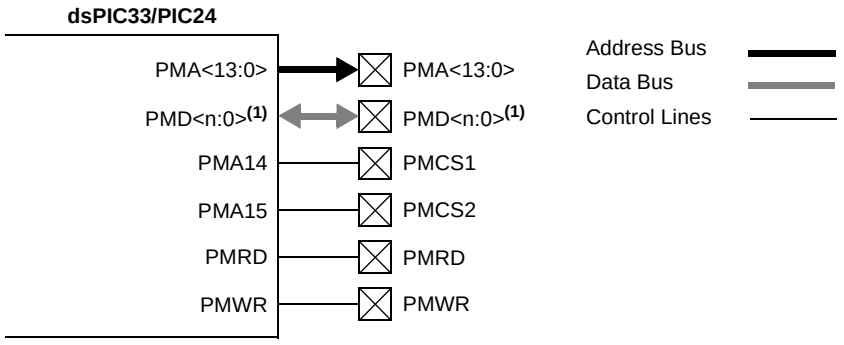
Table 3-1: Master Port Address Multiplexing

ADRMUX<1:0>	Addressing Mode
00	Demultiplexed
01	Partially Multiplexed
10	Fully Multiplexed, 8-Bit
11	Fully Multiplexed, 16-Bit

3.1.3.1 Demultiplexed Mode

In Demultiplexed mode (ADRMUX<1:0> = 00), data and address information are completely separated. Data bits are presented on PMD<7:0> and address bits are presented on PMA<15:0>, as shown in Figure 3-1. Without any additional Wait states enabled, a read/write operation takes one TCY.

Figure 3-1: Demultiplexed Addressing Mode (ADRMUX<1:0> = 00)

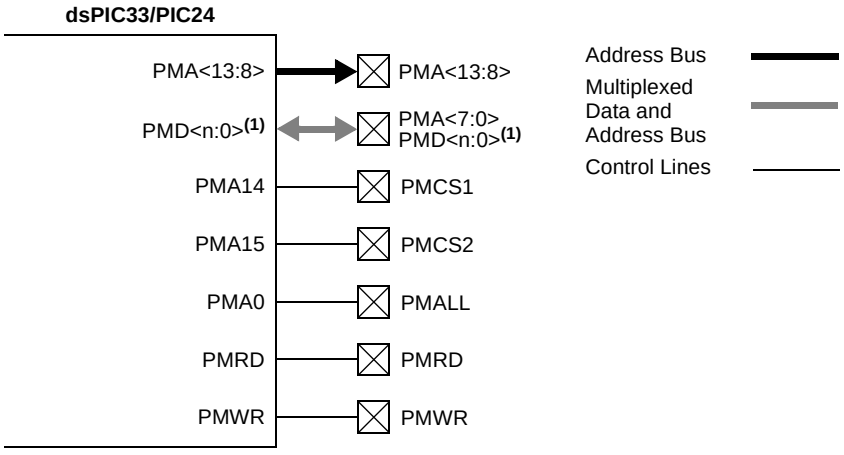


Note 1: Data width is dependent on state of MODE16 bit (PMMODE<10>).

3.1.3.2 Partially Multiplexed Mode

In Partially Multiplexed mode (ADRMUX<1:0> = 01), the lower eight bits of the address are multiplexed with the data pins on PMD<7:0>, as shown in Figure 3-2. The upper eight bits of the address are unaffected and are presented on PMA<15:8>. The PMA0 pin is used as an address latch and presents the Address Latch Low enable strobe (PMALL). The read and write sequences are extended by a complete CPU cycle, during which, the address is presented on the PMD<7:0> pins. This means that without any additional Wait states enabled, a read/write operation takes two TCY.

Figure 3-2: Partially Multiplexed Addressing Mode (ADRMUX<1:0> = 01))



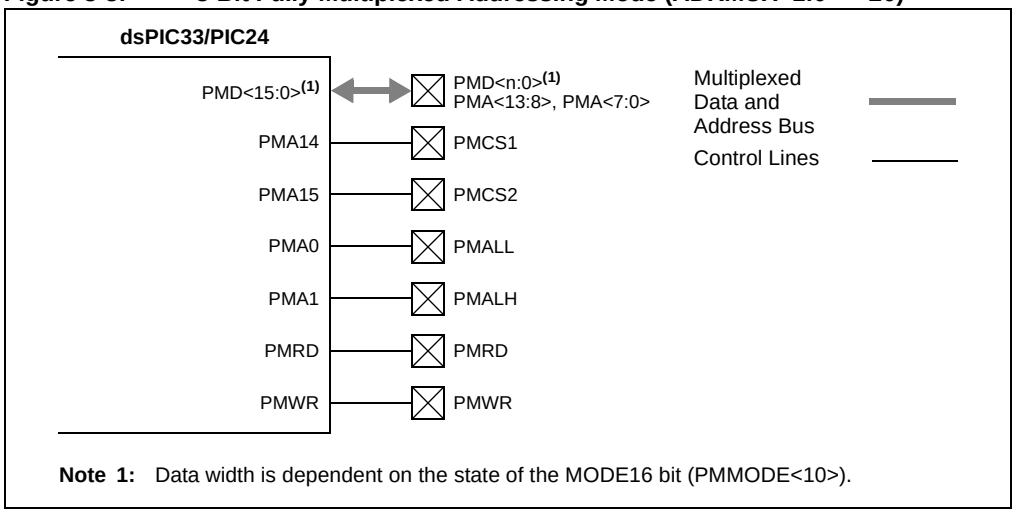
Note 1: Data width is dependent on the state of the MODE16 bit (PMMODE<10>).

3.1.3.3 Fully Multiplexed, 8-Bit Mode

In 8-Bit Fully Multiplexed mode (ADRMUX<1:0> = 10), the entire 16 bits of the address are multiplexed with the data pins on PMD<7:0>, as shown in Figure 3-3. The PMA0 and PMA1 pins are used to present Address Latch Low (PMALL) enable and Address Latch High (PMALH) enable strobes, respectively.

The read and write sequences are extended by two complete CPU cycles. During the first cycle, the lower eight bits of the address are presented on the PMD<7:0> pins with the PMALL strobe active. During the second cycle, the upper eight bits of the address are presented on the PMD<7:0> pins with the PMALH strobe active. In the event the upper address bits are configured as Chip Select pins, the corresponding address bits are automatically forced to '0'. Without any additional Wait states enabled, a read/write operation takes three TCY.

Figure 3-3: 8-Bit Fully Multiplexed Addressing Mode (ADRMUX<1:0> = 10)

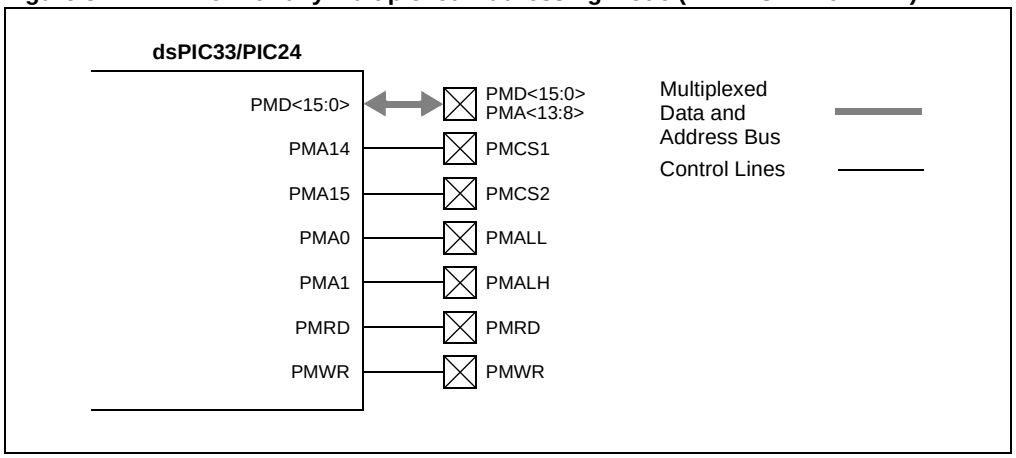


Note 1: Data width is dependent on the state of the MODE16 bit (PMMODE<10>).

3.1.3.4 Fully Multiplexed, 16-Bit Mode

In 16-Bit Fully Multiplexed mode (ADRMUX<1:0> = 11), the entire 16 bits of the address are multiplexed with the data pins on PMD<15:0>, as shown in Figure 3-4. An Address Latch Low enable strobe (PMPALL) is presented on the PMA0 pin and an Address Latch High enable strobe (PMPALH) is presented on the PMA1 pin. The read and write sequences are extended by a complete CPU cycle, during which, all sixteen bits of the address are presented on the PMD<15:0> pins with the PMPALL and PMPALH strobes active at the same time. In the event the upper address bits are configured as Chip Select pins, the corresponding address bits are automatically forced to '0'.

Figure 3-4: 16-Bit Fully Multiplexed Addressing Mode (ADRMUX<1:0> = 11)



3.1.4 8-BIT AND 16-BIT DATA MODES

The PMP supports data width of both 8 and 16 bits. The data width is selected by the MODE16 bit (PMMODE<10>). The 16-bit operations are always handled in a multiplexed fashion, with the Least Significant Byte (LSB) of data being presented first, because the data path into and out of the module is only eight bits wide.

3.1.5 READ/WRITE CONTROL

The PMP module supports two distinct read/write signaling methods. In Master Mode 1, the read and write strobes are combined into a single control line, PMRD/PMWR; a second control line, PMENB, determines when a read/write action is to be performed. In Master Mode 2, separate read and write strobes (PMRD and PMWR) are supplied on separate pins. Chip Selects are optionally available in both modes.

3.1.6 CONTROL LINE POLARITY

All control signals (PMRD, PMWR, PMENB, PMAL and PMCSx) can be individually configured for either positive or negative polarity. Configuration is controlled by separate bits in the PMCON register. Note that the polarity of control signals that share the same output pin (for example, PMWR and PMENB) is controlled by the same bit; the configuration depends on which Master Port mode is used. Additionally, the polarity of both PMALH and PMALL are controlled by a single bit.

3.1.7 AUTO-INCREMENT/DECREMENT

When the module is operating in one of the Master modes, the INCM<1:0> bits (PMMODE<12:11>) control the behavior of the address value. The address can be made to automatically increment or decrement after each read and write operation. The address increments when each operation is completed and the BUSY bit goes to '0'. If the Chip Select signals are disabled and configured as address bits, the bits will participate in the increment and decrement operations; otherwise, the CS2 and CS1 bit values will be unaffected.

3.1.8 WAIT STATES

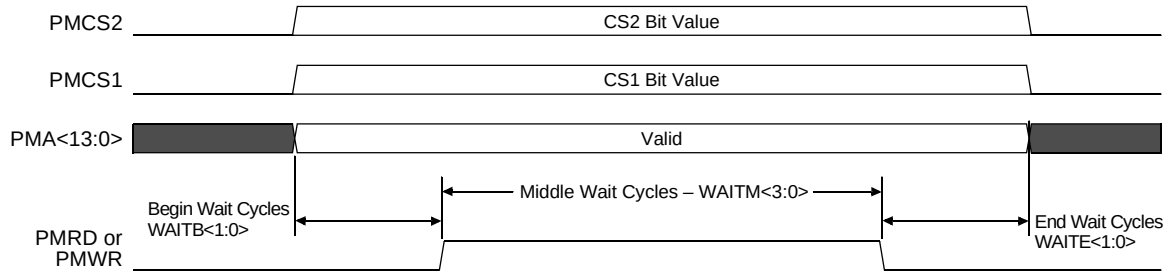
In Master mode, the user has control over the duration of the read, write and address cycles by configuring the module Wait states as multiples of TCY. Three portions of the cycle (the beginning, middle and end) are configured using the corresponding WAITBx, WAITMx and WAITEx bits in the PMMODE register. For the WAITB<1:0> and WAITE<1:0> bits to control the beginning and end cycle Wait times, the WAITM<3:0> must be configured for something other than '0000'.

The WAITB<1:0> bits (PMMODE<7:6>) set the number of Wait states at the beginning of the cycle. The Wait states are applied between data setup and the PMRD or PMWR strobes in Master Mode 2, or the PMENB strobe in Master Mode 1, as shown in Figure 3-5. When the address bus is multiplexed with the data bus (ADRMUX<1:0> (PMCON<12:11>) = 01, 10 or 11), the WAITBx state is added to the length of each part of the address phase.

The four WAITMx bits (PMMODE<5:2>) set the number of Wait cycles for the PMRD or PMWR strobes in Master Mode 1 or for the PMENB strobe in Master Mode 2. When this Wait state setting is '0', WAITBx and WAITEx have no effect.

The two WAITEx bits (PMMODE<1:0>) set the number of Wait cycles for the data hold time after the PMRD or PMWR strobes in Master Mode 1 or after the PMENB strobe in Master Mode 2.

Figure 3-5: Wait State Configuration in Master Modes 1 and 2



Note: For the WAITB<1:0> and WAITE<1:0> bits to control the beginning and end cycle Wait times, the WAITM<3:0> bits must be configured for something other than '4'b0000'.

3.1.9 PIN FUNCTIONS BASED ON OPERATING MODE

Depending on the options selected, many of the physical pins of the PMP module can perform different functions in different Master modes. In some modes, certain pins may become available for device I/Os or other device features. Table 3-2 summarizes the pin functions. Table 3-3 summarizes the differences in control and address pin functions based on the selected Master mode, Address Multiplexing mode and the number of Chip Selects enabled. Table 3-4 lists how data and addressing are multiplexed in different Data Width and Address Multiplexing modes.

Table 3-2: Control Signal Pin Functions

Pin Function	Function Description
PMRD	Read Strobe
PMWR	Write Strobe
PMRD/~PMWR	Combined Read/Write Strobe
PMENB	PMRD/~PMWR Active
PMCS1	Chip Select 1
PMCS2	Chip Select 2
PMALL	Address Latch Low Byte
PMALH	Address Latch High Byte
PMA0	Address Bit 0
PMA1	Address Bit 1

Note: For a PMP pin to function as a general I/O pin, its corresponding port control bit must also be configured correctly. See **Section 3.1.2 "Port Pin Control"** for more information.

Table 3-3: PMP Address and Control Pin Functions in All Master Modes

PMP Pin Name	Pin Functions in Address Multiplexing Modes (ADRMUX<1:0>) and Chip Selects (CSF<1:0>)								
	Demultiplexed (00)			Partial (01)			Full (10)		
	0 CS (00)	1 CS (01)	2 CS (10)	0 CS (00)	1 CS (01)	2 CS (10)	0 CS (00)	1 CS (01)	2 CS (10)
Master Mode 1 (Shared Read/Write Strobe), 8-Bit and 16-Bit Data Modes									
PMRD	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR	PMRD/PMWR
PMWR	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB	PMENB
PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2
PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1
PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	I/O	I/O	I/O
PMA<7:2>	PMA<7:2>	PMA<7:2>	PMA<7:2>	I/O	I/O	I/O	I/O	I/O	I/O
PMA1	PMA1	PMA1	PMA1	I/O	I/O	I/O	PMALH	PMALH	PMALH
PMA0	PMA0	PMA0	PMA0	PMALL	PMALL	PMALL	PMALL	PMALL	PMALL
Master Mode 2 (Separate Read and Write Strobes), 8-Bit and 16-Bit Data Modes									
PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD	PMRD
PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR	PMWR
PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2	PMA15	PMCS2	PMCS2
PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1	PMA14	PMA14	PMCS1
PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	PMA<13:8>	I/O	I/O	I/O
PMA<7:2>	PMA<7:2>	PMA<7:2>	PMA<7:2>	I/O	I/O	I/O	I/O	I/O	I/O
PMA1	PMA1	PMA1	PMA1	I/O	I/O	I/O	PMALH	PMALH	PMALH
PMA0	PMA0	PMA0	PMA0	PMALL	PMALL	PMALL	PMALL	PMALL	PMALL

Table 3-4: PMP Data Pin Functions for All Master Modes

PMP Data Mode (MODE16)	Pin Functions for PMD<7:0> in Address Multiplexing Modes (ADRMUX<1:0>)			
	Demultiplexed (00)	Partial (01)	8-Bit Full (10)	16-Bit Full (11)
8-Bit (0)	PMD<7:0>	PMA<7:0>, PMD<7:0>	PMA<7:0>, PMA<15:8>, PMD<7:0>	PMA<15:0>, PMD<7:0>
16-Bit (1)	PMD<7:0> PMD<15:8>	PMA<7:0>, PMD<7:0>, PMD<15:8>	PMA<7:0>, PMA<15:8>, PMD<7:0>, PMD<15:8>	PMA<15:0>, PMD<15:0

3.2 Read Operation

To perform a read on the parallel port, the user application reads the low byte of the PMDIN1 register. This causes the PMP to output the desired values on the Chip Select lines and the address bus. Then, the read line (PMRD) is strobed and the read data is placed into the low byte of the PMDIN1 register.

If the 16-bit mode is enabled (MODE16 = 1), the read of the low byte for the PMDIN1 register will initiate two bus reads. The first read data byte is placed into the lower byte of the PMDIN1 register and the second read data is placed into the upper byte of PMDIN1.

Note that the read data obtained from the PMDIN1 register is actually the read value from the previous read operation. Therefore, the first user application read will be a dummy read to initiate the first bus read and fill the Read register. Also, the requested read value will not be ready until the BUSY bit is observed low. Thus, in a back-to-back read operation, the data read from the register will be the same for both reads. The next read of the register will yield the new value.

To summarize this section, perform two reads of the PMDIN1 register to read a random byte/word – the second read gives the actual data. To perform a sequential read: perform one dummy read, followed by the required number of actual reads of the PMDIN1 register.

3.2.1 WRITE INITIATED PMP READ

By writing the RDSTART (PMCONH<7>) bit to a '1', a PMP read can be initiated in the same way as performing a read of the PMDOUTx/PMDINx registers. This can be used as the first read in a series of reads, since the data from the first read of the PMP must be thrown away.

3.3 Write Operation

To perform a write onto the parallel bus, the user writes to the low byte of the PMDIN1 register. This causes the module to first output the desired values on the Chip Select lines and the address bus. The lower byte of the data written into the PMDIN1 register is placed onto the PMD<7:0> data bus. Then, the write line (PMWR) is strobed.

If the 16-bit mode is enabled (MODE16 = 1), the write to the low byte of the PMDIN1 register will initiate two bus writes. The first write will consist of the data contained in the lower byte of PMDIN1. The second write will contain the upper byte of PMDIN1.

3.4 Dual Buffer Mode

Dual Buffer mode changes the registers used to initiate a read or a write on the PMP bus. It is enabled by setting the DUALBUF bit (PMCONH<1>). Instead of using PMADDR and PMDIN1/2 for Master mode initiated PMP transactions, the read and write operations use a different set of registers. To initiate a read, the user will access the PMRADDR and PMRDIN registers. To initiate a PMP write, the user will access the PMWADDR and PMDOUT1/2 registers. Other than the register change, all other Master mode operations will look the same on the PMP bus.

3.5 Parallel Master Port Status

3.5.1 THE BUSY BIT

In addition to the PMP interrupt, the BUSY bit (PMMODE<15>) is provided to indicate the status of the module. This bit is only used in Master mode.

While any read/write operation is in progress, BUSY is set for all but the very last CPU cycle of the operation. In effect, if a single-cycle read/write operation is requested, BUSY is not active. This allows back-to-back transfers. It is only helpful if Wait states are enabled or multiplexed address/data is selected.

While the bit is set, any request by the user application to initiate a new operation will be ignored (i.e., writing or reading the lower byte of the PMDIN1 register will not initiate a read or a write). The user application needs to try again after the BUSY flag is cleared.

3.5.2 INTERRUPTS

When the PMP module interrupt is enabled for Master mode, the module will interrupt on every completed read/write cycle. Otherwise, the BUSY bit is available to query the status of the module.

3.6 Master Mode Timing

This section provides timing examples that represent the common Master mode configuration options. These options vary from 8-bit to 16-bit data, fully demultiplexed to fully multiplexed addresses. All figures use Master Mode 2 (MODE<1:0> = 10). Data width is dependent on the state of the MODE16 bit (PMMODE<10>). See Table 3-4 to evaluate PMD<n:0>.

Table 3-5: Master Mode Timing Diagram Summary

Address Multiplexing	Operation	Figure
Demultiplexed	Read	3-6
Demultiplexed	Write	3-7
Partially Multiplexed	Read	3-8
Partially Multiplexed	Write	3-9
8-Bit Fully Multiplexed	Read	3-10
8-Bit Fully Multiplexed	Write	3-11
16-Bit Fully Multiplexed	Read	3-12
16-Bit Fully Multiplexed	Write	3-13

Figure 3-6: Read Timing, Demultiplexed Address

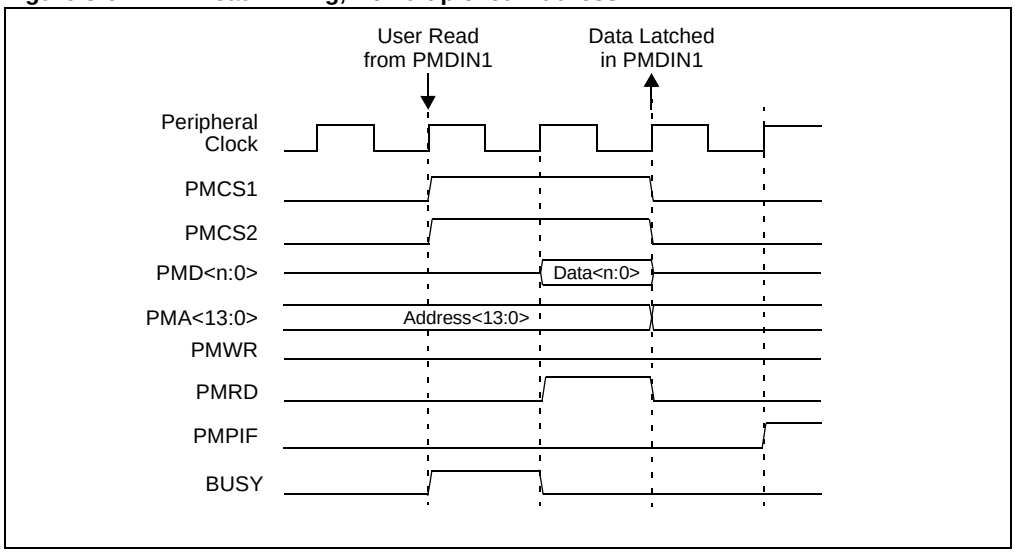


Figure 3-7: Write Timing, Demultiplexed Address

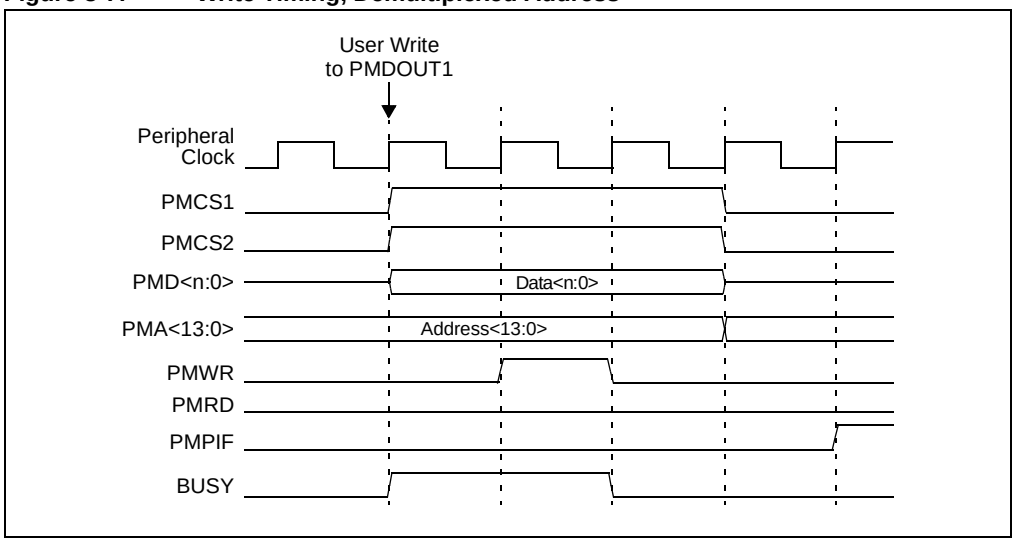


Figure 3-8: Read Timing, Partially Multiplexed Address (ADRMUX<1:0> = 01)

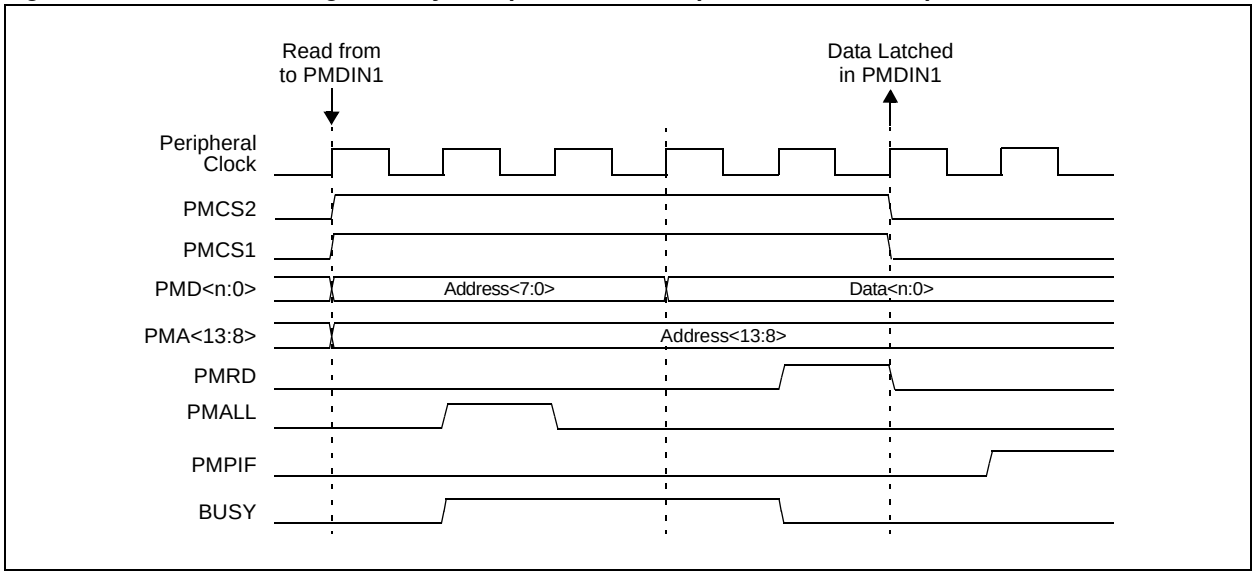


Figure 3-9: Write Timing, Partially Multiplexed Address (ADRMUX<1:0> = 01)

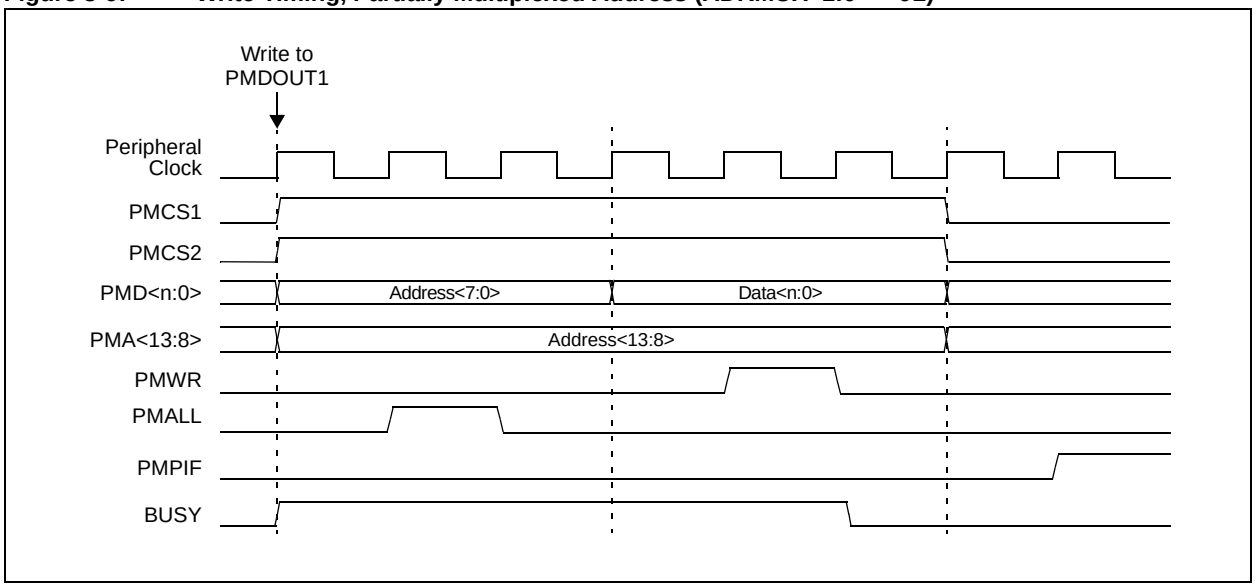


Figure 3-10: Read Timing, 8-Bit Fully Multiplexed Address (ADRMUX<1:0> = 10)

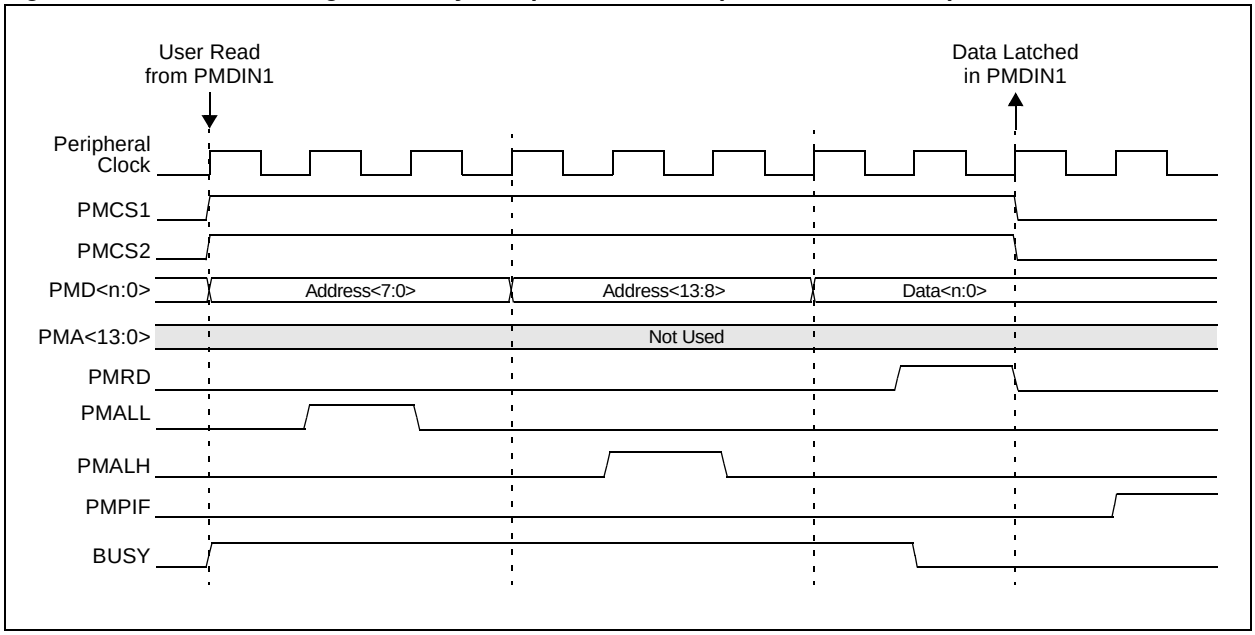


Figure 3-11: Write Timing, 8-Bit Fully Multiplexed Address (ADRMUX<1:0> = 10)

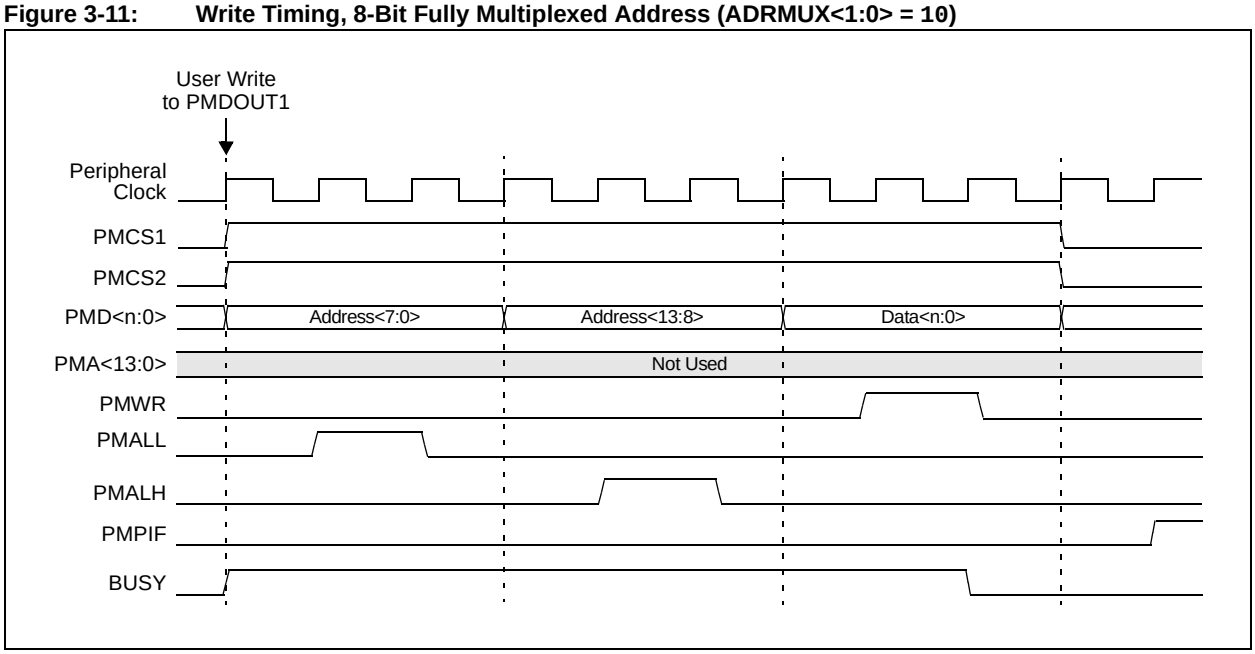


Figure 3-12: Read Timing, 16-Bit Fully Multiplexed Address (ADRMUX<1:0> = 11)

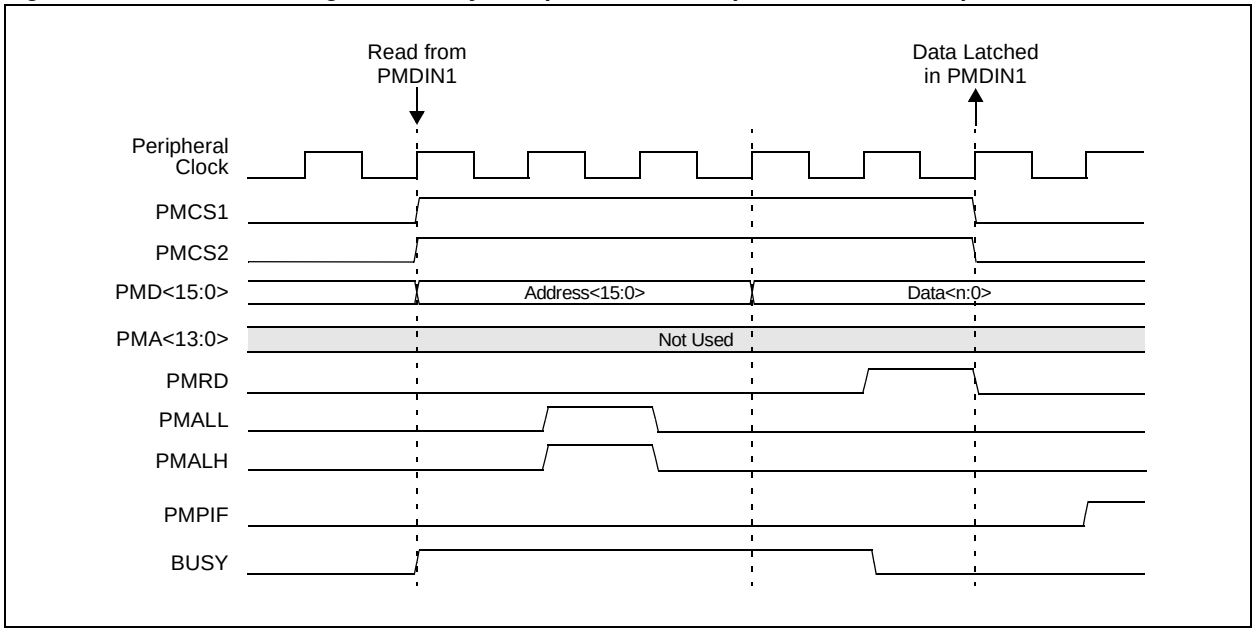
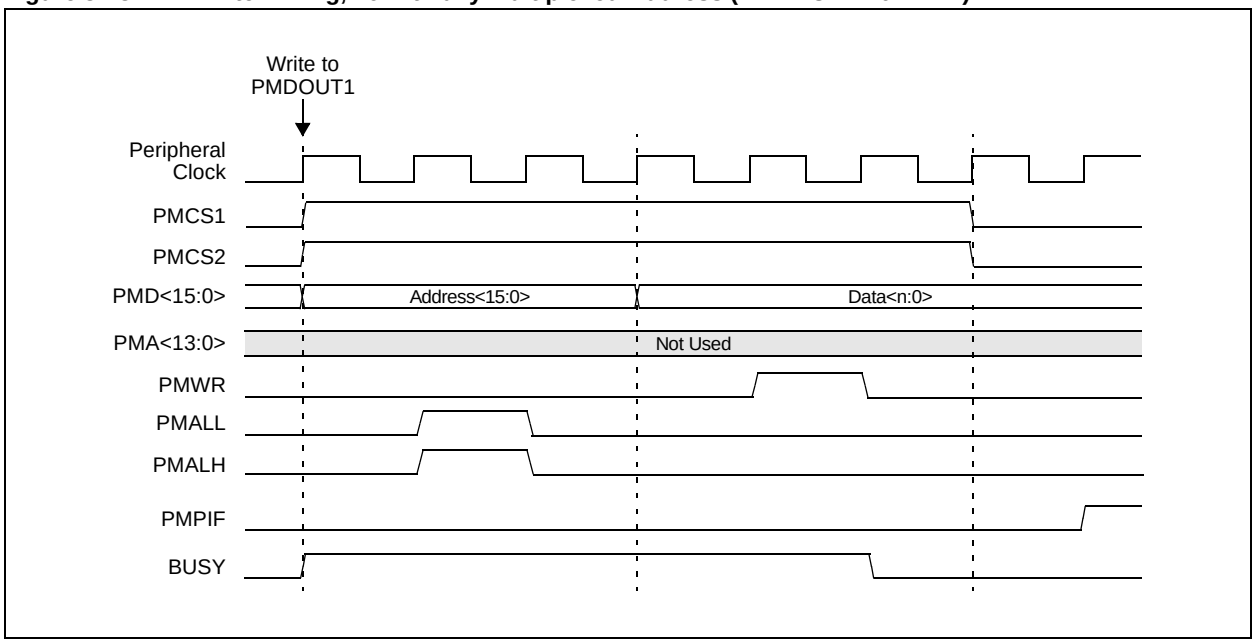


Figure 3-13: Write Timing, 16-Bit Fully Multiplexed Address (ADRMUX<1:0> = 11)



4.0 SLAVE PORT MODES

In Slave mode, the PMP module provides an 8-bit data bus and all the necessary control signals to operate as a slave parallel device. It is configurable for operation in Legacy, Buffered and Addressable modes, as shown in Table 4-1.

Table 4-1: Slave Port Modules

Slave Mode	MODE<1:0>	INCM<1:0>
Legacy	00	00
Buffered	00	11
Addressable	01	00

Slave mode provides several options for a flexible interface:

- 8-bit data bus
- Two address lines (Addressable mode only)
- Three control lines (read, write and Chip Select)
- Selectable polarity on all control lines

To use the PMP as a slave, the module must be enabled (ON = 1) and set to one of the two possible Slave modes (PMMODE<9:8> = 01 or 00).

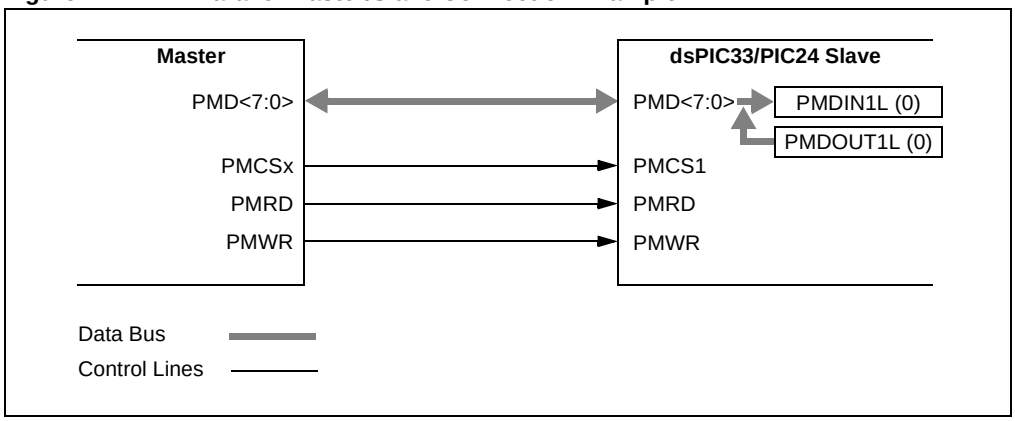
Note: For all control lines (and PMA<1:0> in Addressable PSP mode), the corresponding control bits in the PMCON and PMAEN registers must be configured for parallel port operation. See **Section 3.1.2 "Port Pin Control"** for more details.

4.1 Legacy Mode

In Legacy mode (MODE<1:0> (PMMODE<9:8>) = 00 and INCM<1:0> (PMMODE<12:11>) = 00), the module is configured as a Parallel Slave Port (PSP) with the associated enable module pins dedicated to the module. In this mode, an external device, such as another controller or microprocessor, can asynchronously read and write data using the 8-bit data bus (PMD<7:0>), the read (PMRD), write (PMWR) and Chip Select (PMCSx) inputs.

Note: PMCS1 is used as the Chip Select input in all Slave modes. PMCS2 is used only in Master mode.

Figure 4-1: Parallel Master/Slave Connection Example

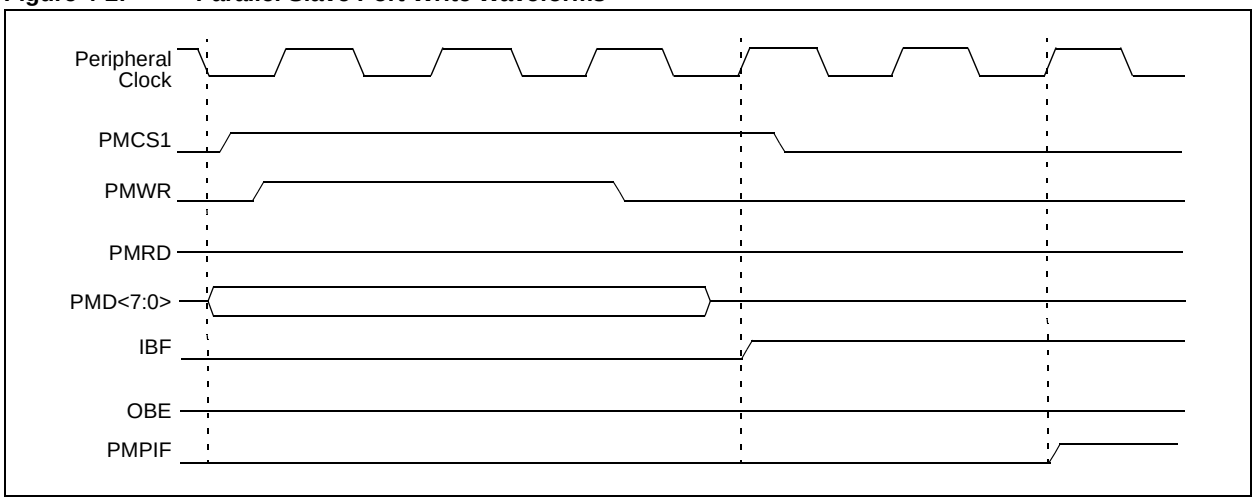


4.1.1 WRITE TO SLAVE PORT

When Chip Select is active and a write strobe occurs (PMCS1 = 1 and PMWR = 1), the data from PMD<7:0> is captured into the lower eight bits of the PMDIN1 register (PMDIN1<7:0>). The PMPIF and IBF flag bits are set when the write ends.

The timing for the control signals in Write mode is shown in Figure 4-2. The polarity of the control signals is configurable.

Figure 4-2: Parallel Slave Port Write Waveforms

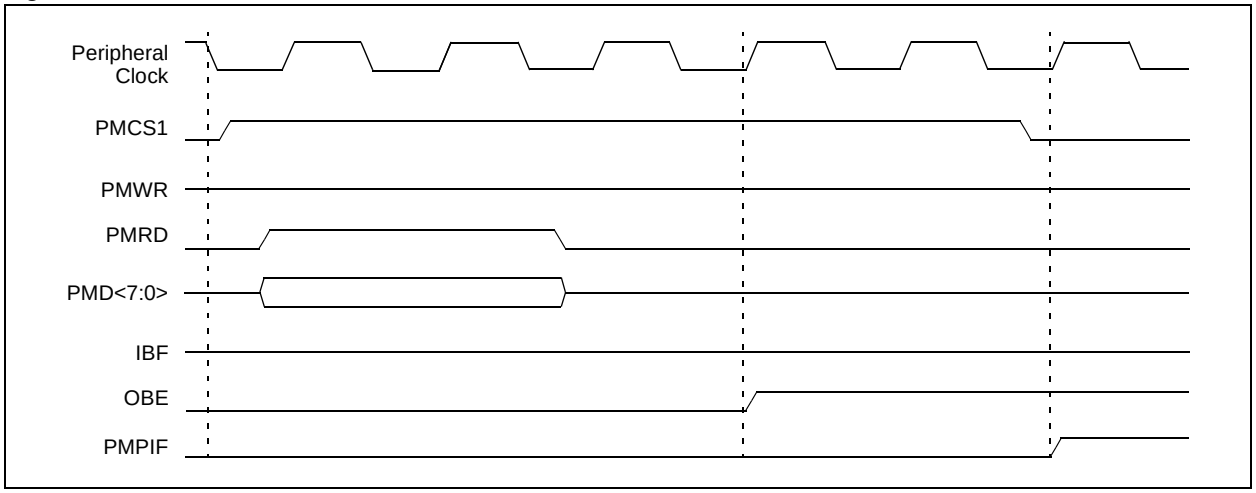


4.1.2 READ FROM SLAVE PORT

When Chip Select is active and a read strobe occurs (PMCS1 = 1 and PMRD = 1), the data from the lower eight bits of the PMDOUT1 register (PMDOUT1<7:0>) is presented onto PMD<7:0>. The data in PMDOUT1<7:0> is read out and the Output Buffer Empty Status flag, OBE, is set. If the user writes new data to PMDOUT1<7:0> to clear OBE, the data is immediately read out; however, OBE is not cleared.

The timing for the control signals in Read mode is shown in Figure 4-3.

Figure 4-3: Parallel Slave Port Read Waveforms



4.1.3 INTERRUPT OPERATION

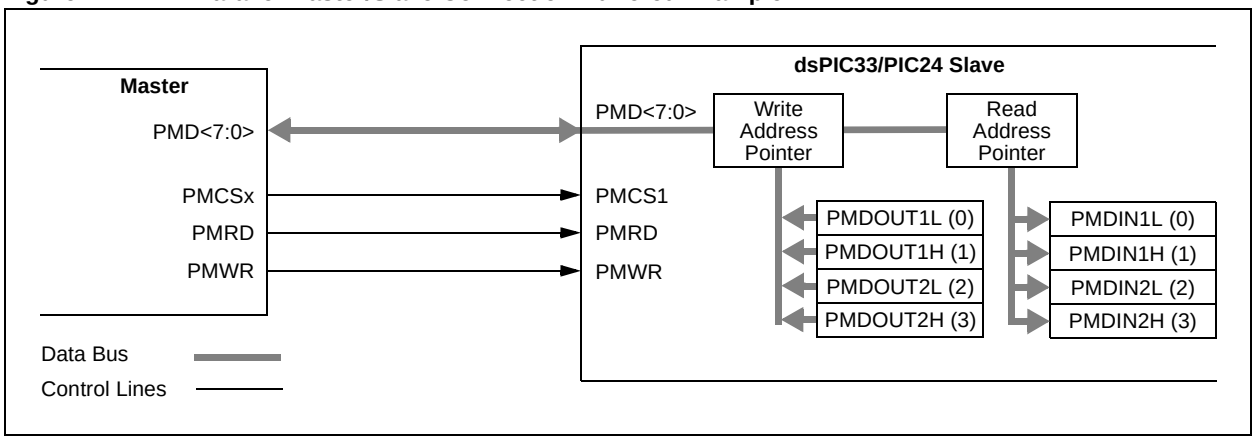
When either the PMCS1 or PMRD lines are detected high, the port pins return to the input state and the PMPIF bit in the interrupt control module is set. The user application should wait for PMPIF to be set before servicing the module. When PMPIF is set, the IBF and OBE bits can be polled and the appropriate action taken.

4.2 Buffered Parallel Slave Port Mode

Buffered Parallel Slave Port mode is functionally identical to the Legacy Parallel Slave Port mode with an exception of the implementation of 4-level read and write buffers. Buffered PSP mode is enabled by setting the INCM<1:0> bits (PMMODE<12:11>) to '11'.

When the Buffered mode is active, the module uses the PMDIN1 and PMDIN2 registers as write buffers, and the PMDOUT1 and PMDOUT2 registers as read buffers. Each register is split into two single-byte buffer registers, producing separate read and write buffers that are each four bytes deep. Buffers are numbered 0-3, starting with the lower byte of PMDIN1 or PMDOUT1 and progressing upward through the high byte of PMDIN2 or PMDOUT2.

Figure 4-4: Parallel Master/Slave Connection Buffered Example



4.2.1 READ FROM SLAVE PORT

For read operations, the bytes are sent out sequentially, starting with Buffer 0 (PMDOUT1<7:0>) and ending with Buffer 3 (PMDOUT2<15:8>) for every read strobe. The module maintains an internal pointer for tracking the buffer that is to be read.

Each buffer has a corresponding read status bit, OBxE, in the PMSTAT register. This bit is cleared when a buffer contains data that is not written to the bus and is set when data is written to the bus. If the current buffer location being read from is empty, a buffer underflow is generated and the Output Buffer Underflow Status bit, OBUF (PMSTAT<6>), is set. When all four OBxE status bits are set, the OBE bit is also set.

4.2.2 WRITE TO SLAVE PORT

For write operations, the data must be stored sequentially, starting with Buffer 0 (PMDIN1<7:0>) and ending with Buffer 3 (PMDIN2<15:8>). For read operations, the PMP module maintains an internal pointer to the buffer that is to be written next.

The input buffers have their own write status bits, IBxF. The bit is set when the buffer contains unread incoming data and cleared when the data has been read. The flag bit is set on the write strobe. If a write occurs on a buffer when its associated IBxF bit is set, the Input Buffer Overflow Status flag, IBOV, is set; any incoming data in the buffer is lost. If all 4 IBxF flags are set, the Input Buffer Full Status Flag (IBF) is set.

4.2.3 INTERRUPT OPERATION

In Buffered Slave mode, the module can be configured to generate an interrupt on every read/write strobe (IRQM<1:0> = 01). It can also be configured to generate an interrupt on a read from Read Buffer 3 or a write to Write Buffer 3 (IRQM<1:0> = 11), which is essentially an interrupt every fourth read/write strobe. When interrupting every fourth byte for input data, all Input Buffer registers should be read to clear the IBxF flags. If these flags are not cleared, an overflow condition can occur. The PMSTAT register provides status information on all buffers.

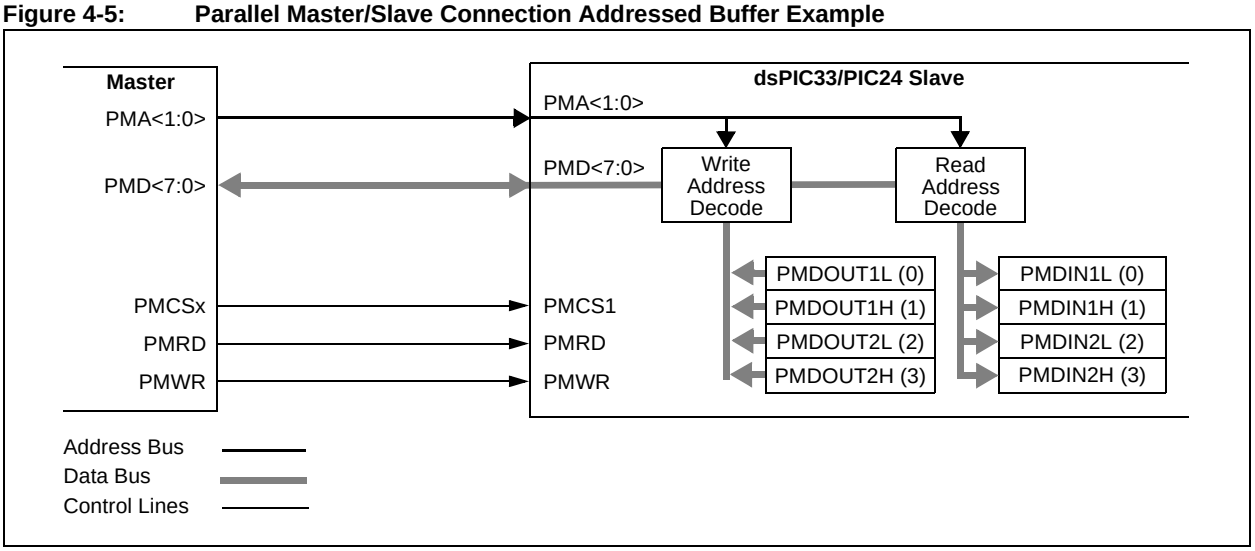
4.3 Addressable Parallel Slave Port Mode

In Addressable Parallel Slave Port mode, the module is configured with two extra inputs, PMA<1:0>. This makes the 4-byte buffer space directly addressable as fixed pairs of read and write buffers. The Addressable PSP mode is enabled by setting the MODE<1:0> (PMMODE<9:8>) bits to '01'. For Buffered Legacy mode, data is output from PMDOUT1 and PMDOUT2, and is read in PMDIN1 and PMDIN2. Table 4-2 shows the address resolution for the incoming address to the Input and Output Buffer registers.

Table 4-2: Slave Mode Address Resolution

PMA<1:0>	Output Register (Buffer)	Input Register (Buffer)
00	PMDOUT1<7:0> (0)	PMDIN1<7:0> (0)
01	PMDOUT1<15:8> (1)	PMDIN1<15:8> (1)
10	PMDOUT2<7:0> (2)	PMDIN2<7:0> (2)
11	PMDOUT2<15:8> (3)	PMDIN2<15:8> (3)

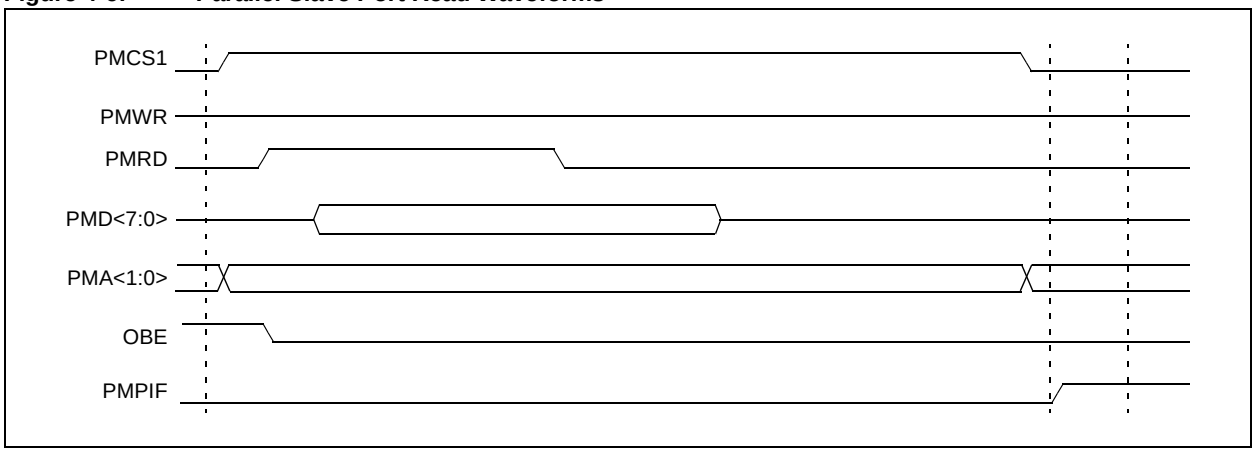
Figure 4-5: Parallel Master/Slave Connection Addressed Buffer Example



4.3.1 READ FROM SLAVE PORT

When Chip Select is active and a read strobe occurs (PMCS1 = 1 and PMRD = 1), the data from one of the four output bytes is presented onto PMD<7:0>. The byte to read depends on the 2-bit address placed on PMA<1:0>. Table 4-2 shows the corresponding output registers and their associated address. When an output buffer is read, the corresponding OBxE bit is set. The OBE flag bit is set when all the buffers are empty. For any buffer that is already empty, OBxE = 1, the next read to that buffer will set the OBUF (PMSTAT<6>) flag.

Figure 4-6: Parallel Slave Port Read Waveforms

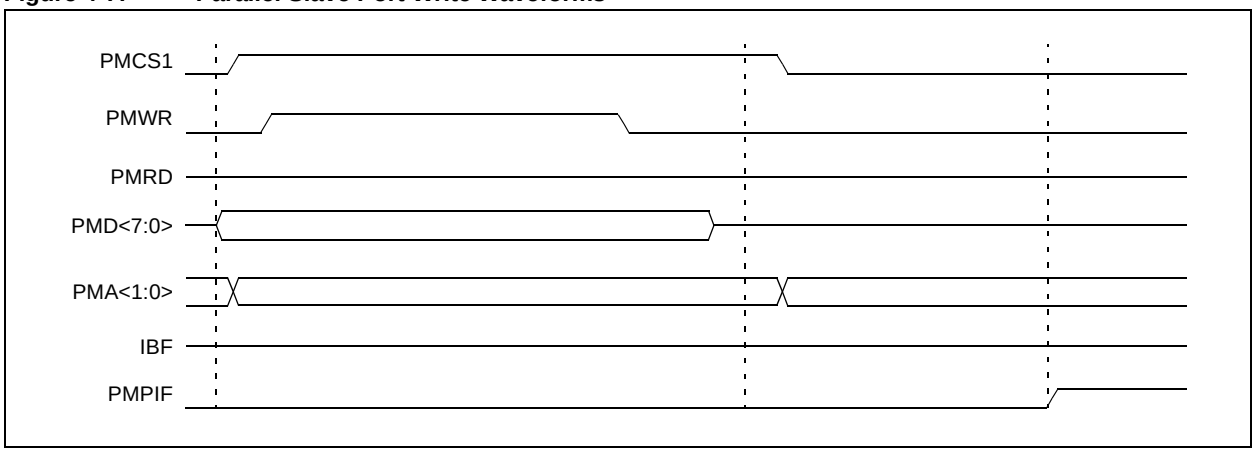


4.3.2 WRITE TO SLAVE PORT

When Chip Select is active and a write strobe occurs (PMCS1 = 1 and PMWR = 1), the data from PMD<7:0> is captured into one of the four input buffer bytes. Which byte is written depends on the 2-bit address placed on PMA<1:0>. Table 4-2 shows the corresponding input registers and their associated address.

When an input buffer is written, the corresponding IBxF bit is set. The IBF flag bit is set when all the buffers are written. If any buffer is already written, IBxF = 1, the next write strobe to that buffer will generate an IBOV event and the byte will be discarded.

Figure 4-7: Parallel Slave Port Write Waveforms



4.3.3 INTERRUPT OPERATION

In Addressable PSP mode, the module can be configured to generate an interrupt on every read/write strobe. It can also be configured to generate an interrupt on any read from Read Buffer 3 or write to Write Buffer 3 (an interrupt will occur whenever a read/write occurs when the PMA<1:0> pins are '11').

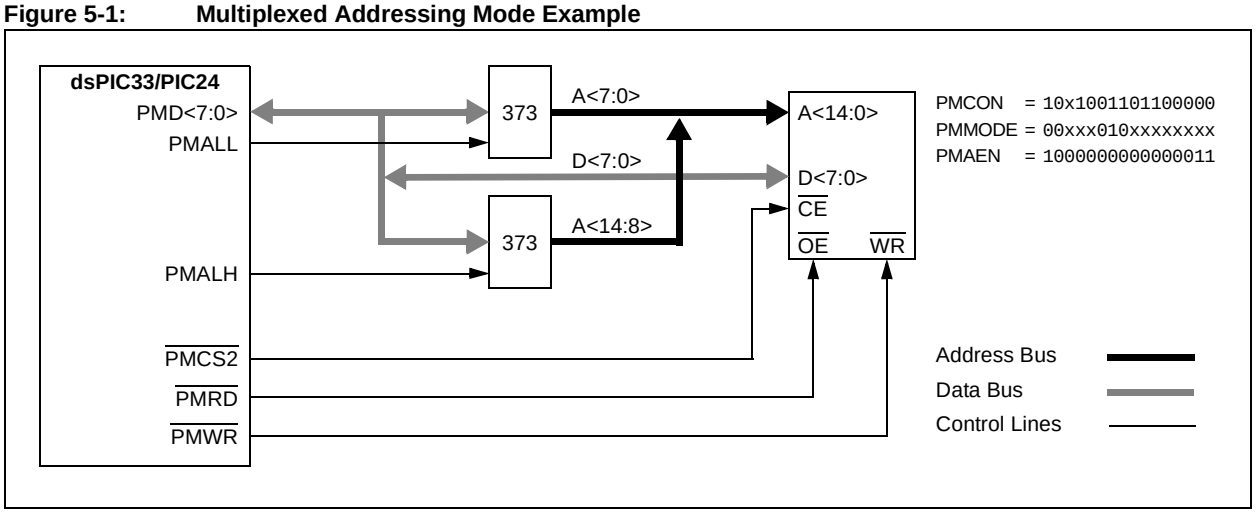
5.0 APPLICATION EXAMPLES

This section introduces some potential applications for the PMP module.

5.1 Multiplexed Memory or Peripheral

Figure 5-1 illustrates the connection of a memory or another addressable peripheral in Master Full Multiplex mode. Consequently, this mode achieves the best pin saving from the device perspective. However, for this configuration, some external latches are required to maintain the address.

Figure 5-1: Multiplexed Addressing Mode Example



5.2 Partially Multiplexed Memory or Peripheral

Partial multiplexing implies using more pins. However, for a few extra pins, extra performance can be achieved. Figure 5-2 shows an example of a memory or peripheral that is partially multiplexed with an external latch. If the peripheral has internal latches, no extra circuitry is required except for the peripheral itself (as shown in Figure 5-3).

Figure 5-2: Partially Multiplexed Addressing Mode Example

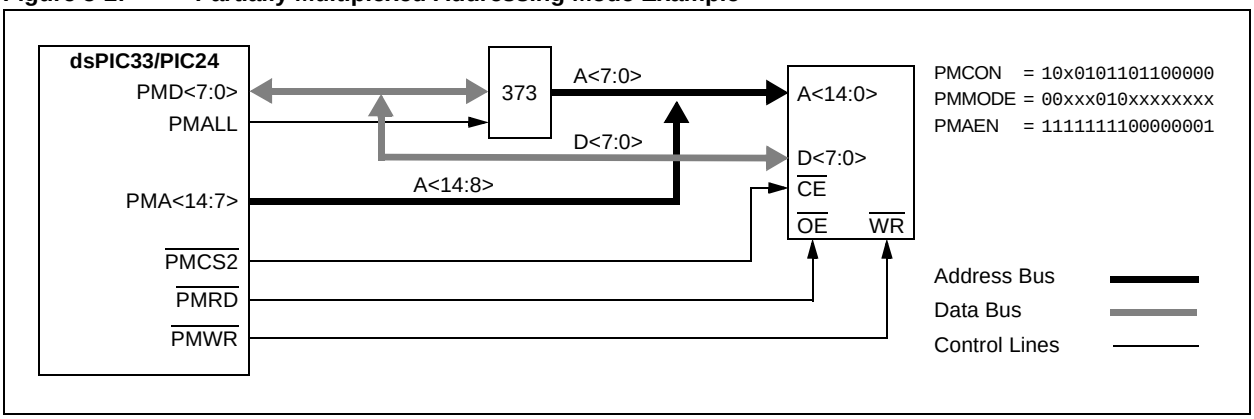
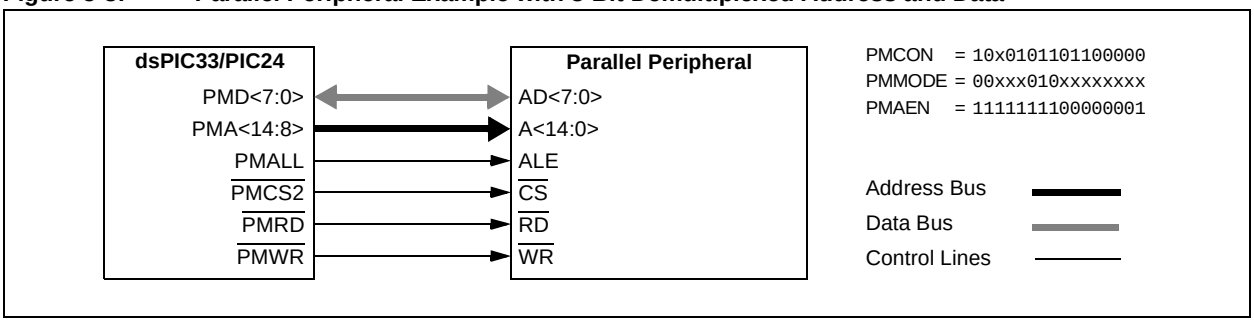


Figure 5-3: Parallel Peripheral Example with 8-Bit Demultiplexed Address and Data



5.3 Parallel Flash/EEPROM Examples

Figure 5-4 shows an example of connecting parallel Flash/EEPROM to the PMP. Figure 5-5 shows a slight variation of that, configuring the connection for 16-bit data from a single byte-addressable Flash/EEPROM. Figure 5-6 also demonstrates the interface with a 16-bit device without using byte select logic.

Figure 5-4: Parallel Flash/EEPROM Example (Up to 15-Bit Address), 8-Bit Data

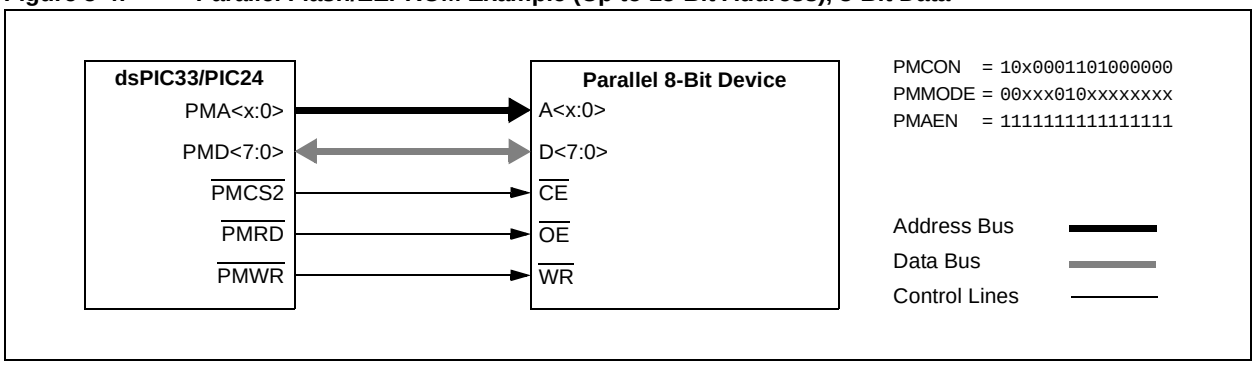


Figure 5-5: Parallel Flash/EEPROM Example (Up to 15-Bit Address), 16-Bit Data (Byte Select Mode)

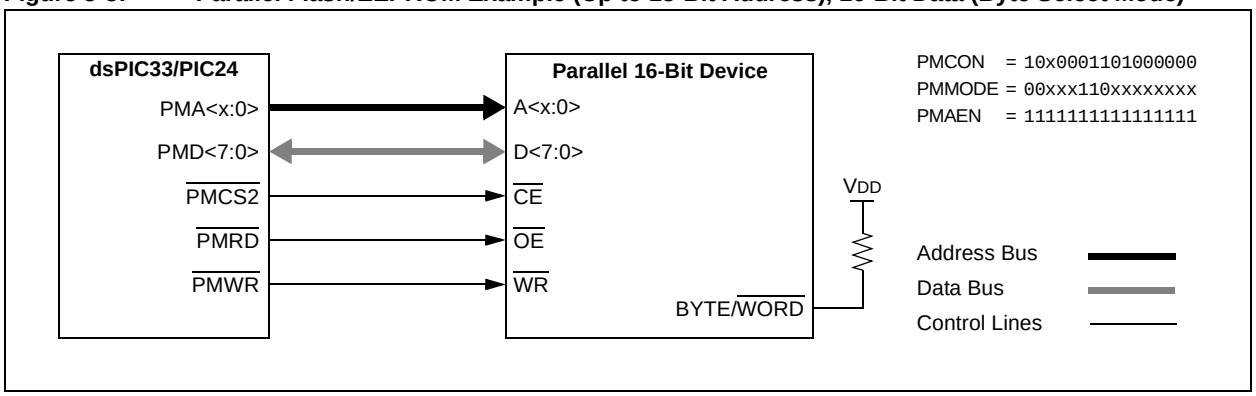
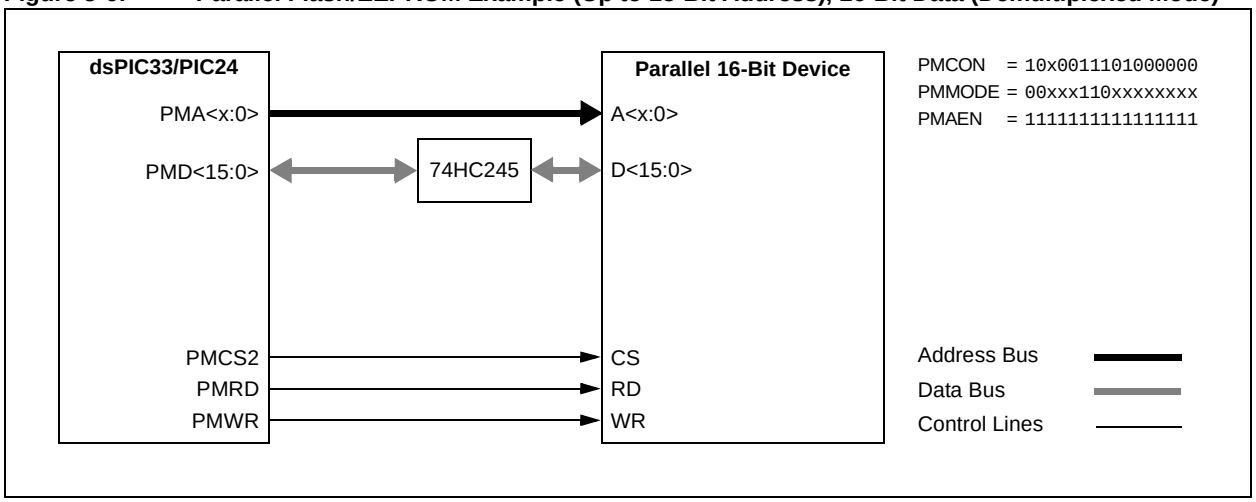


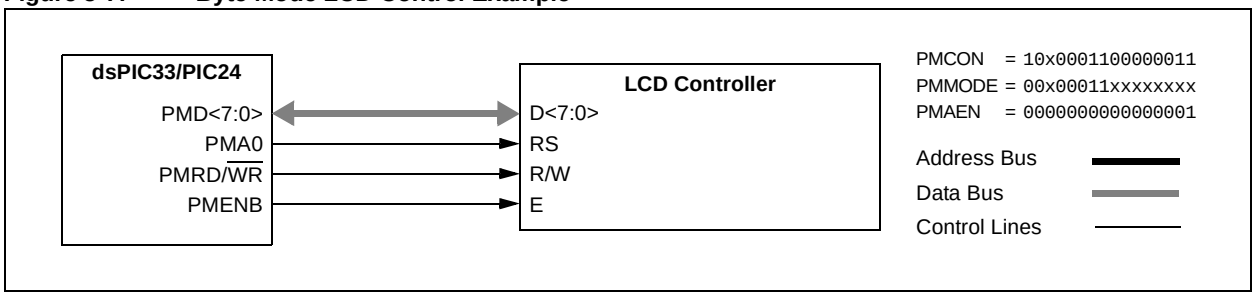
Figure 5-6: Parallel Flash/EEPROM Example (Up to 15-Bit Address), 16-Bit Data (Demultiplexed Mode)



5.4 LCD Controller Example

The PMP module can be configured to connect to a typical LCD controller interface, as shown in Figure 5-7. In this case, the PMP module is configured for active-high control signals because common LCD displays require active-high control.

Figure 5-7: Byte Mode LCD Control Example



6.0 OPERATION IN POWER-SAVING MODES

The dsPIC33/PIC24 family of devices has one power mode, the Normal Operational (Full-Power) mode, and two power-saving modes, Sleep and Idle, which are invoked by the PWRSAV instruction. Depending on the mode selected, entering a power-saving mode may also affect the operation of the module.

6.1 Sleep Mode

When the device enters Sleep mode, the peripheral clock is disabled. The consequences of Sleep mode depend on the mode in which the PMP module is configured when the Sleep mode is invoked.

6.1.1 MASTER MODE OPERATION

If the device enters Sleep mode while the module is operating in Master mode, PMP operation will be suspended in its current state until clock execution resumes. As this may cause unexpected control pin timings, users should avoid invoking Sleep mode when continuous use of the module is needed.

6.1.2 SLAVE MODE OPERATION

While the module is inactive, but enabled for any Slave mode operation, any read/write operations occurring at that time will be completed without the use of the device's clock. When the operation is complete, the module will issue an interrupt according to the setting of the IRQMx bits. This interrupt can wake the device from Sleep mode.

6.2 Idle Mode

When the device enters Idle mode, the peripheral clock sources remain functional. The SIDL bit (PMCON<13>) selects whether the module will stop or continue functioning in Idle mode. If SIDL = 1, the module will behave the same way as it does in Sleep mode (i.e., slave reception is still possible even though the module clocks are not available and Master mode is suspended).

If SIDL = 0 (the default), the module will continue operation in Idle mode. The current transaction in both Master and Slave modes will be completed and an interrupt is issued.

7.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 device families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Parallel Master Port (PMP) module are:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33/PIC24 device families.

8.0 REVISION HISTORY

Revision A (October 2017)

This is the initial version of this document.

Note the following details of the code protection feature on Microchip devices:

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