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## Section 32. Configuration

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### HIGHLIGHTS

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**Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices.

Please consult the note at the beginning of the “**Special Features**” chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: <http://www.microchip.com>

## 32.1 INTRODUCTION

A PIC32 family device includes several nonvolatile (programmable) Configuration Words that define device behavior.

The device configuration features may vary according to PIC32 family variants; however, the following features are common to all PIC32 devices:

- System Clock Oscillator mode and Phase-Locked Loop (PLL)
- Secondary Oscillator (SOSC) enable/disable
- Watchdog Timer (WDT) enable/disable and postscaler
- Boot Flash and Program Flash write-protect regions
- User ID
- Debug mode

The PIC32 Configuration Words are located in Boot Flash memory and are programmed when the PIC32 Boot Flash region is programmed.

System clock oscillator and PLL bits provide a large selection of flexible clock source options and PLL prescalers/postscalers.

The SOSC bit enables or disables a low-power SOSC that can serve as a clock source for several peripherals, such as RTCC, Timer1 and CPU.

The WDT and postscaler bits allow the user to permanently disable or enable the WDT. When enabled, a postscaler can be selected to provide a wide range of WDT periods. A Windowed mode Watchdog feature is also available.

The Boot Flash and Program Flash write-protected bits provide write protection to all of Boot Flash memory and selected regions of Program Flash memory.

User ID bits are available for programming application-specific or product-specific identification information, such as product ID or serial numbers. Debug mode bits provide a selection of debugging modes and channels.

**Note:** For more information on the available device Configuration Words, refer to the specific device data sheet.

## 32.2 MODES OF OPERATION

### 32.2.1 PIC32MX Configuration Words

In the PIC32MX family of devices, the Configuration Words select various device configurations, and are located in the last four Words (32-bit x 4 Words) of Boot Flash memory, DEVCFG0 to DEVCFG3.

During programming, a Configuration Word can be programmed a maximum of two times before a page erase must be performed. For example, during device programming, a user can program the Configuration Word, DEVCFG1, with desired data, and then perform a verification or other integrity check. DEVCFG1 can then be programmed again, this time setting any remaining unprogrammed bits to '0'.

**Note:** The Configuration Word, DEVCFG0, can only be programmed once before a page erase must be performed. Each time the Boot Flash memory region is erased, the DEVCFG0[31] bit is automatically set to '0', leaving only one additional programming operation available, DEVCFG0.

After programming the Configuration Words, the user should reset the device to ensure the Configuration data is reloaded with the new programmed values.

#### 32.2.1.1 CONFIGURATION REGISTER PROTECTION

To ensure the 128-bit data integrity of each Configuration Word, a comparison is continuously made between each Configuration bit and its stored complement. If a mismatch is detected, a Configuration Mismatch Reset is generated causing a device Reset.

### 32.2.2 PIC32MZ Configuration and Alternate Configuration Words

In the PIC32MZ family of devices, the Configuration Words select various device configurations, and are located at physical addresses 0x1FC0FFC0 (DEVCFG3) through 0x1FC0FFCC (DEVCFG0).

If an unrecoverable ECC error occurs when reading the Configuration Words, the Alternate Configuration Words are used to configure the device and Boot Flash memory. This configuration can be identical to the primary Configuration Words, or different to operate in another condition. The Alternate Configuration Words are located at physical addresses 0x1FC0FF40 (ADEVCFG3) through 0x1FC0FF4C (ADEVCFG0). To flag that an ECC error has occurred, the BCFGERR (RCON[27]) bit is set.

If uncorrectable ECC errors are found in both primary and alternate words, the BCFGFAIL (RCON[26]) bit is set and the default configuration is used.

During programming, all four Configuration Words should be programmed at the same time to ensure ECC operation. The Configuration Words can only be programmed once before a quad-word erase must be performed. All unprogrammed bits should be set to '0'.

After programming the Configuration Words, the user application should reset the device to ensure the configuration data is reloaded with the new programmed values.

#### 32.2.2.1 SEQUENCE NUMBER AND BOOT FLASH MEMORY

In the PIC32MZ family of devices, there are two regions of Boot Flash memory. Each can contain its own version of Configuration and Alternate Configuration Words, and its own bootloader. At boot the device reads two memory locations from each panel, which are called the sequence numbers. If the value programmed into the TSEQ[15:0] bits of the Boot Flash 1 Sequence Word 0 (BF1SEQ0) is equal to or greater than the value programmed into the TSEQ[15:0] bits of the Boot Flash 2 Sequence Word 0 (BF2SEQ0), Boot Flash 1 is aliased to the lower boot alias region. If the value of the TSEQ[15:0] bits of BF2SEQ0 is greater than the TSEQ[15:0] bits of BF1SEQ0, Boot Flash 2 is aliased to the lower boot alias region.

The CSEQ[15:0] bits must contain the complement value of the TSEQ[15:0] bits; otherwise, the value of the TSEQ[15:0] bits is considered invalid, and an alternate sequence is used.

Once Boot Flash memories are aliased, configuration space located in the lower boot alias region is used as the basis for the configuration words DEVSIGN0, DEVCP0 and DEVCFGx.

## 32.2.3 PIC32MZ W1 Configuration Words

In the PIC32MZ W1 family of devices, the Configuration Words select various device configurations, and are located at physical addresses 0x1F800000 (CFGCON0) through 0x1F800040 (CFGCON4) and 0x1F800100 (BCFG0).

During programming, a Configuration Word can be programmed only one time before a page erase must be performed.

The Configuration Words CFGCON0, CFGCON1, CFGCON2, CFGCON4 and BCFG0 are loadable into related registers. These Configuration Words values are loaded from boot Flash memory at system start-up. The user can update these Configuration Words for updating configuration values while the system is running. The user-updated values are not stored back in the boot Flash memory region. The Configuration Word CFGCON3 is not loadable. The user cannot update the configuration value while the system is running.

### 32.2.3.1 CONFIGURATION REGISTER PROTECTION

To ensure the 128-bit data integrity of each Configuration Word, a comparison is continuously made between each Configuration bit and its stored complement. If a mismatch is detected, a Configuration Mismatch Reset is generated, causing a device Reset.

## 32.3 EFFECTS OF VARIOUS RESETS

The Configuration data is reloaded from the corresponding Boot Flash memory Configuration Words on the following types of reset:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- External Reset ( $\overline{\text{MCLR}}$ )
- Configuration Mismatch Reset (CM)
- Watchdog Timer Reset (WDTR)
- Software Reset (SWR)
- NMI Time-out Reset (NMITR)

### 32.4 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Configuration are:

Title	Application Note #
No related application notes at this time.	N/A

**Note:** Please visit the Microchip web site ([www.microchip.com](http://www.microchip.com)) for additional application notes and code examples for the PIC32 device families.

## 32.5 REVISION HISTORY

### Revision A (August 2007)

This is the initial released version of this document.

### Revision B (October 2007)

Updated document to remove Confidential status.

### Revision C (April 2008)

Revised status to Preliminary; Revised U-0 to r-x; Revised Section 32.3.2; Revised Table 32-1; Revised Configuration Word DEVID Register; Revised Configuration Word DEVCFG2 Register.

### Revision D (June 2008)

Revised Register 31-1 (DEVCFG0); Change Reserved bits from “Maintain as” to “Write”.

### Revision E (July 2009)

This revision includes the following updates:

- Minor updates to the text and formatting have been incorporated throughout the document.
- Added a note regarding Configuration Word availability in PIC32MX devices to “**Section 32. Configuration Words**”.
- Added the following bits to **Table 32-1: Configuration Word Summary** and to the related registers:
  - SIGN (see Register 32-1)
  - WINDIS (Register 32-2)
  - FVBUSIO (Register 32-4)
  - FUSBIDIO (Register 32-4)
  - FSCM1IO (Register 32-4)
  - FCANIO (Register 32-4)
  - FETHIO (Register 32-4)
  - FMIIEN (Register 32-4)
  - FSRSEL (Register 32-4)

### Revision F (June 2011)

This revision includes the following updates:

- Added a note with information to customers for utilizing family reference manual sections and data sheets as a joint reference (see note above **32.1 “Introduction”**)
- Removed Register 32-1 through Register 32-5
- Removed **32.2 CONFIGURATION WORDS**
- Updated **32.2.1 “Configuration Words”**
- Removed **32.3.2 Device Code Protection**
- Removed **32.3.3 Program Write Protection (PWP)**
- Removed Table 32-1 through Table 32-3
- Updated all PIC32MX references to PIC32
- Updates to formatting and minor text changes were incorporated throughout the document

### Revision G (November 2013)

This revision includes the following updates:

- Added **32.2.2 “PIC32MZ Configuration and Alternate Configuration Words”**
- Minor updates to text and formatting were incorporated throughout the document

### Revision H (September 2020)

This revision includes the following update:

- Added **32.2.3 “PIC32MZ W1 Configuration Words”** and **32.2.3.1 “Configuration Register Protection”**.

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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