IGLOO2 HPMS

DDR Controller Configuration

Microsemi

Table of Contents

Introduction

The IGLOO2 HPMS has an embedded DDR controller (HPMS DDR). This DDR controller is intended to control an off-chip DDR memory. The HPMS DDR controller can be accessed from the HPMS (using HPDMA) as well as from the FPGA fabric.

When you use System Builder to build a system block which includes an HPMS DDR, System Builder configures the HPMS DDR controller for you based on your entries and selections.

No separate HPMS DDR configuration by the user is required. For details, please refer to the IGLOO2 System Builder User 's Guide.

System Builder

System Builder

Invoke System Builder to configure the HPMS DDR automatically.

1. In the Device Features tab of System Builder, check **HPMS External DDR Memory (HPMS DDR)**.
2. In the Memories tab, select the **DDR Memory Type**:
   - DDR2
   - DDR3
   - LPDDR
3. Select the **Width** of the DDR Memory: 8, 16 or 32
4. Check **ECC** if you want to have ECC for the DDR.
5. Enter the **DDR memory setting time**. This is the time the DDR memory requires to initialize.
6. Click **Import Register Configuration** to import the Register values for the FDDR from an existing text file containing the register values. See Table 1 for the register configuration file syntax.

Libero automatically stores this configuration data in the eNVM. Upon FPGA reset, this configuration data will automatically be copied into the HPMS DDR.

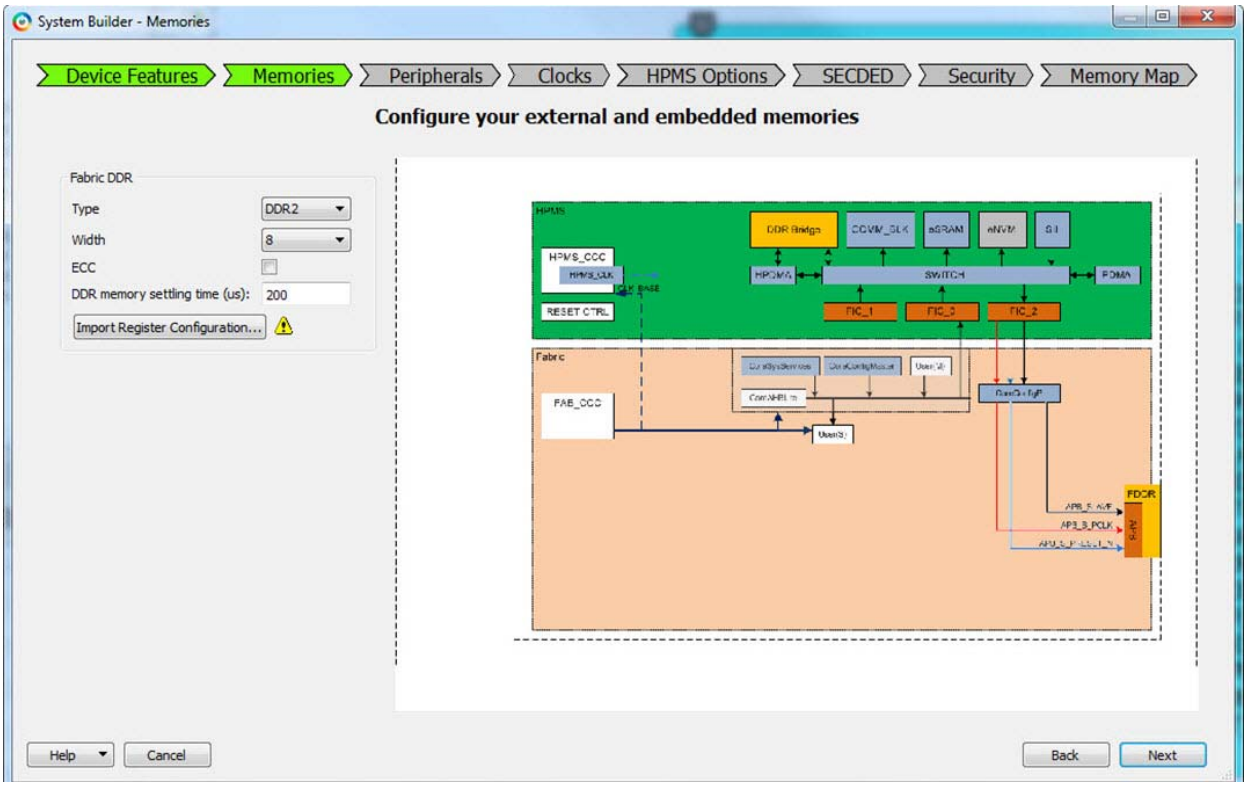

***Figure 1* • System Builder and HPMS DDR**

***Table 1* • Register Configuration File Syntax**

```
ddrc_dyn_soft_reset_CR 0x00 ;
ddrc_dyn_refresh_1_CR 0x27DE ;
ddrc_dyn_refresh_2_CR 0x30F ;
ddrc_dyn_powerdown_CR 0x02 ;
ddrc_dyn_debug_CR 0x00 ;
ddrc_ecc_data_mask_CR 0x0000 ;
ddrc_addr_map_col_1_CR 0x3333 ;
```

1 – HPMS DDR Controller Configuration

When you use the HPMS DDR Controller to access an external DDR Memory, the DDR Controller must be initialized at runtime. This is done by writing configuration data to dedicated DDR controller configuration registers. In IGLOO2, the eNVM stores the register configuration data and after FPGA reset, the configuration data is copied from the eNVM to the HPMS DDR's dedicated registers for initialization.

HPMS DDR Control Registers

The HPMS DDR Controller has a set of registers that need to be configured at runtime. The configuration values for these registers represent different parameters, such as DDR mode, PHY width, burst mode, and ECC. For complete details about the DDR controller configuration registers please refer to the Microsemi IGLOO2 User's Guide

HPMS MDDR Registers Configuration

). **To specify the DDR Register values:**

1. Use a text editor outside of Libero SoC, prepare a text file containing the Register names and values, as in Figure 1-1.
2. From System Builder's **Memory** tab, click **Import Register Configuration**.
3. Navigate to the location of the Registration Configuration text file you have prepared in Step 1 and select the file to import.

```
ddrc_dyn_soft_reset_CR          0x00 ;
ddrc_dyn_refresh_1_CR           0x27DE ;
ddrc_dyn_refresh_2_CR           0x030F ;
ddrc_dyn_powerdown_CR           0x02 ;
ddrc_dyn_debug_CR               0x00 ;
ddrc_ecc_data_mask_CR           0x0000 ;
ddrc_addr_map_col_1_CR          0x3333 ;
ddrc_addr_map_col_3_CR          0x3300 ;
```

Figure 1-1 **• Register Configuration Data - Text Format**

HPMS DDR Initialization

The Register Configuration data you import for the HPMS DDR are loaded into the eNVM and copied to the HPMS DDR configuration registers upon FPGA reset. No user action is required to initialize the HPMS DDR at runtime. This automated initialization is also modeled in simulation.

2 – Port Description

DDR PHY Interface

These ports are exposed at the top level of the System Builder generated block. For details, consult the IGLOO2 System Builder User Guide. Connect these ports to your DDR memory.

***Table 2-1* • DDR PHY Interface**

Port Name	Direction	Description
MDDR_CAS_N	OUT	DRAM CASN
MDDR_CKE	OUT	DRAM CKE
MDDR_CLK	OUT	Clock, P side
MDDR_CLK_N	OUT	Clock, N side
MDDR_CS_N	OUT	DRAM CSN
MDDR_ODT	OUT	DRAM ODT
MDDR_RAS_N	OUT	DRAM RASN
MDDR_RESET_N	OUT	DRAM Reset for DDR3
MDDR_WE_N	OUT	DRAM WEN
MDDR_ADDR[15:0]	OUT	Dram Address bits
MDDR_BA[2:0]	OUT	Dram Bank Address
MDDR_DM_RDQS ([3:0]/[1:0]/[0])	INOUT	Dram Data Mask
MDDR_DQS ([3:0]/[1:0]/[0])	INOUT	Dram Data Strobe Input/Output - P Side
MDDR_DQS_N ([3:0]/[1:0]/[0])	INOUT	Dram Data Strobe Input/Output - N Side
MDDR_DQ ([31:0]/[15:0]/[7:0])	INOUT	DRAM Data Input/Output
MDDR_DQS_TMATCH_0_IN	IN	FIFO in signal
MDDR_DQS_TMATCH_0_OUT	OUT	FIFO out signal
MDDR_DQS_TMATCH_1_IN	IN	FIFO in signal (32-bit only)
MDDR_DQS_TMATCH_1_OUT	OUT	FIFO out signal (32-bit only)
MDDR_DM_RDQS_ECC	INOUT	Dram ECC Data Mask
MDDR_DQS_ECC	INOUT	Dram ECC Data Strobe Input/Output - P Side
MDDR_DQS_ECC_N	INOUT	Dram ECC Data Strobe Input/Output - N Side
MDDR_DQ_ECC ([3:0]/[1:0]/[0])	INOUT	DRAM ECC Data Input/Output
MDDR_DQS_TMATCH_ECC_IN	IN	ECC FIFO in signal
MDDR_DQS_TMATCH_ECC_OUT	OUT	ECC FIFO out signal (32-bit only)

Port widths for some ports change depending on the selection of the PHY width. The notation "[a:0]/[b:0]/[c:0]" is used to denote such ports, where "[a:0]" refers to the port width when a 32-bit PHY width is selected, "[b:0]" corresponds to a 16-bit PHY width, and "[c:0]" corresponds to an 8-bit PHY width.

A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

5-02-00490-0/08.13