Atmel

APPLICATION NOTE

AT01030: Low-cost Ethernet to Wireless Gateway with ATmega256RFR2

Atmel AVR 8-bit Microcontroller

Features

- Ethernet gateway for IEEE® 802.15.4 wireless networks
- Production-ready turn-key solution
- Low BOM cost
- Low cost two-layer PCB construction
- Atmel® ATmega256RFR2 Wireless SoC with integrated IEEE 802.15.4 transceiver
- High-performance PCB dipole antenna
- WIZnet W5200 Ethernet MAC processor with hardwired TCP/IP stack
- TCP, UDP, IPv4 and other protocols
- 10BaseT/100BaseTX Ethernet MAC and PHY
- RJ45 Ethernet Jack w/ LED indicators
- Atmel AT24MAC402 2-Kbit EEPROM
- Atmel AT45DB642 4-Mbit DataFlash
- Micro-B USB power inlet
- 3.3V LDO regulator
- Power-good indicator
- TVS and ESD protection
- JTAGICE programming header
- One user UART header
- Two user GPIO pins
- One user defined LED
- One user defined push-button switch
- Manual CPU reset button

Description

The Low-Cost Gateway (LCGW) reference design is a turn-key production-ready solution that connects IEEE 802.15.4 wireless networks to wired Ethernet networks. This gateway allows IEEE 802.15.4 wireless devices to interface to smart phones and tablet computers running remote-control applications. The Atmel ATmega256RFR2 wireless system-on-a-chip (SoC) combines best-in-class radio performance with the efficient Atmel AVR® 8-bit CPU. The ATmega256RFR2 provides a responsive CPU and high-performance radio to address the demanding tasks of network coordinator and data concentrator. The WIZnet W5200 embedded Ethernet controller features a

10BaseT/100BaseTX MAC and PHY and supports many popular Ethernet protocols including TCP/IP, UDP and IPv4. The wired Ethernet interface is a low-cost, reliable and secure connection that works with the end user's existing routers, access-points, WLANs and ISPs. Wired Ethernet lowers cost and also avoids interference problems and regulatory issues inherent with co-located radio solutions. This reference design was developed with low BOM cost as a primary objective. The design is free of superfluous accessories and non-essential sub-systems. A standard JTAG interface is provided for programming and debug. The design includes optional EEPROM and Data-Flash memory sockets. DC power is derived from a USB Micro-B Dedicated Charge Port (DCP). This allows users to power the gateway with common phone chargers or from Wi-Fi Access Points with USB ports. Both USB and Ethernet connections have ESD/EMI suppression to improve reliability. The combination of Atmel ATmega256RFR2 and WIZnet W5200 provides a balanced solution with ample resources for gateway and data-concentration applications at an economical price.

Figure 1. Low-cost Gateway.

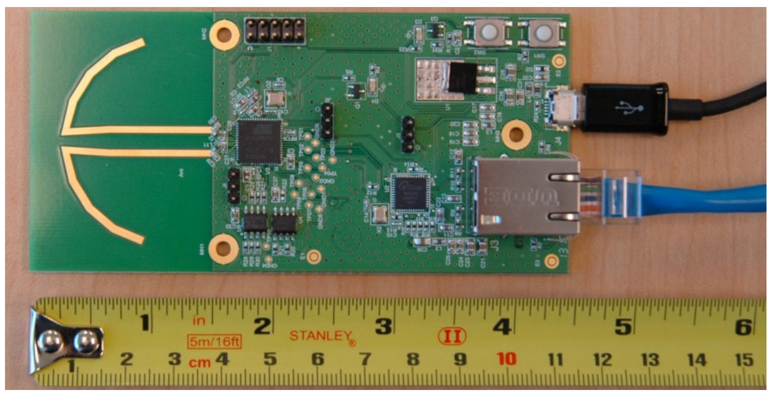
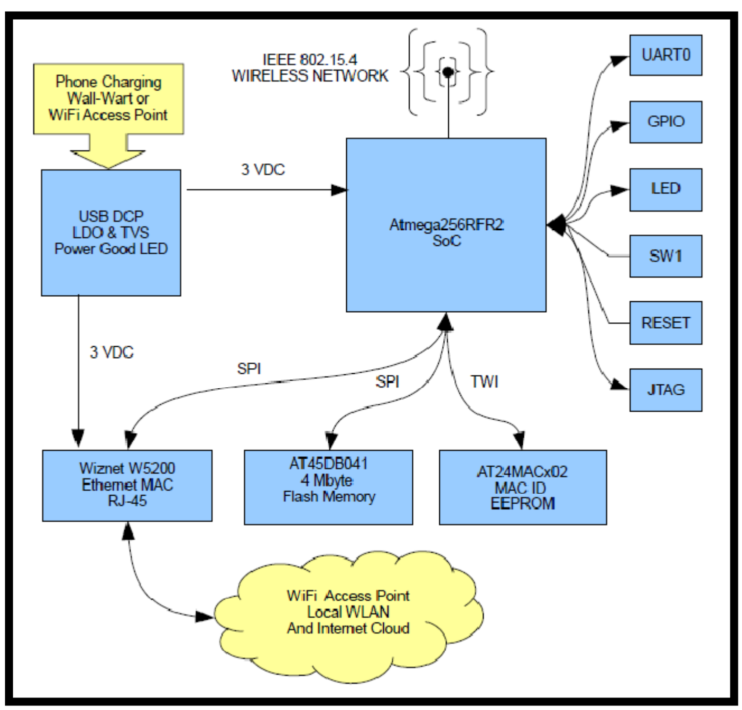


Figure 2. Low-cost Gateway Block Diagram.



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1. Operation

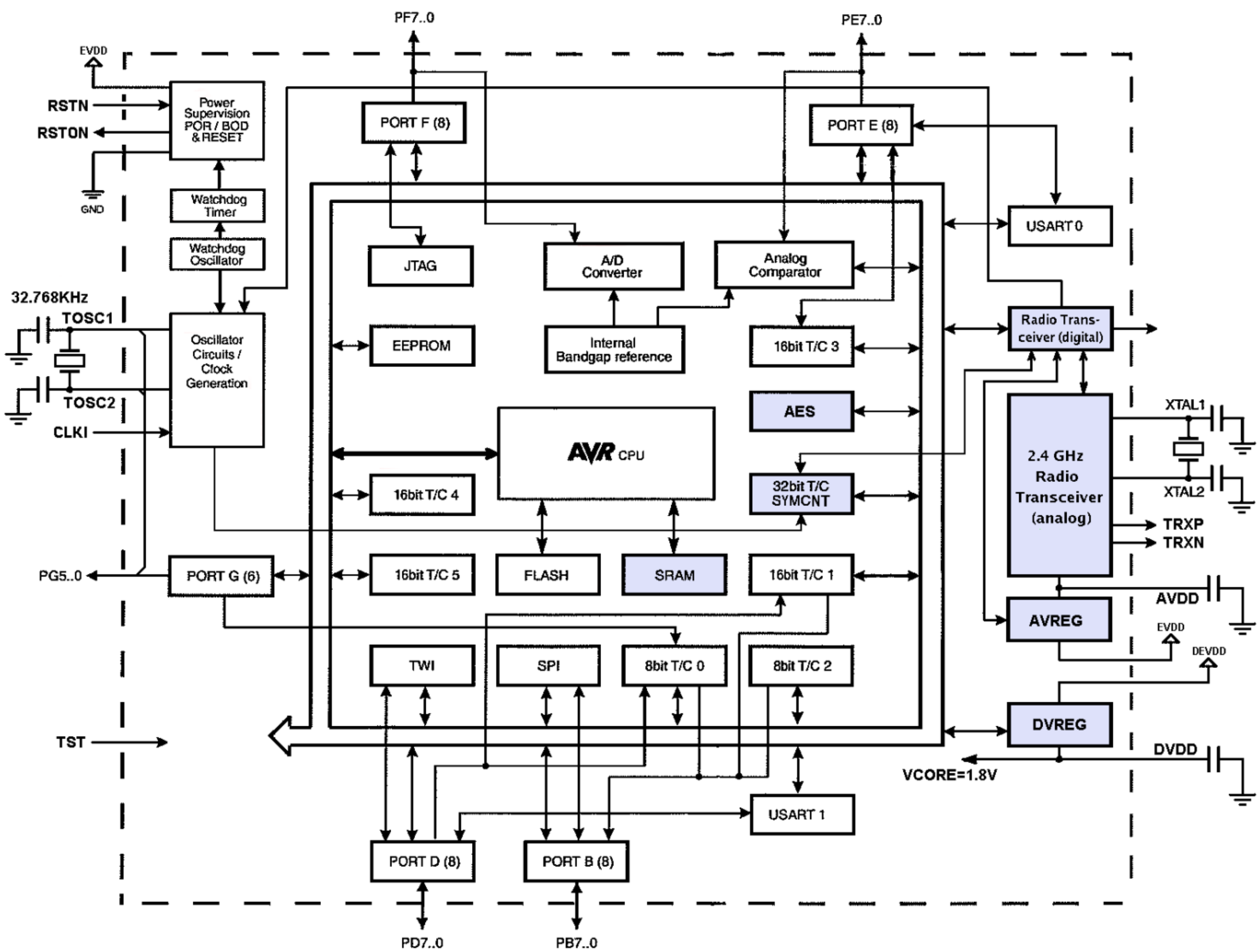
Connections to the LCGW are simple. Connect the DCP to a USB power source using the Micro-B connector. D3 will light indicating DC power is ready. Connect the RJ45 Ethernet port to a router with a CAT5 patch cable. The Atmel ATmega256RFR2 can be programmed and debugged using the 10-pin JTAG header and Atmel JTAGICE programmers. SW2 is a hardware RESET* for the CPU. Ethernet MAC Reset is driven by software. J5 exposes the power rails for testing. There are several user defined features; UART0, Port F GPIO, SW1 and D1 are uncommitted and available to the application developer.

2. Sub-systems

2.1 CPU

The Atmel ATmega2564/1284/644RFR2 is a low-power CMOS 8-bit microcontroller based on the Atmel AVR enhanced RISC architecture combined with a high data rate transceiver for the 2.4GHz ISM band. By executing powerful instructions in a single clock cycle, the device achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed. The radio transceiver provides high data rates from 250kb/s up to 2Mb/s, frame handling, outstanding receiver sensitivity and high transmit output power enabling a very robust wireless communication.

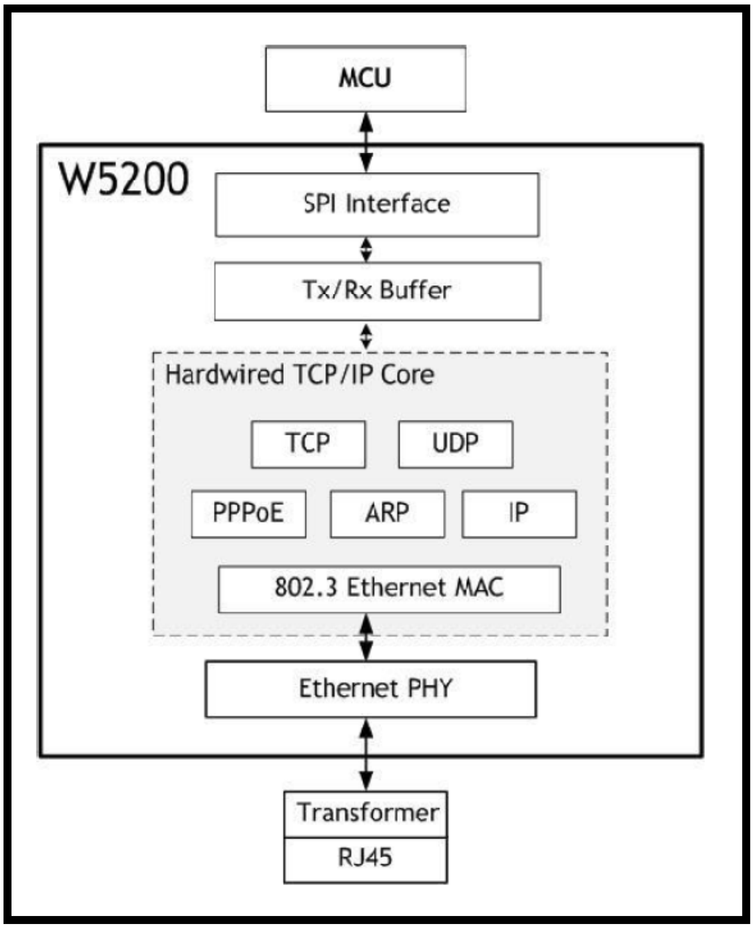
Figure 2-1. Atmel ATmega256RFR2 Block Diagram.



2.2 Ethernet MAC PHY

The W5200 chip is a hardwired TCP/IP embedded Ethernet controller that enables easier internet connection for embedded systems using Serial Peripheral Interface (SPI). W5200 suits best for users who need Internet connectivity for application that uses a single chip to implement TCP/IP stack, 10/100 Ethernet MAC and PHY. The W5200 is composed of a fully hardwired market-proven TCP/IP stack and an integrated Ethernet MAC and PHY. Hardwired TCP/IP stack supports TCP, UDP, IPv4, ICMP, ARP, IGMP and PPPoE, which has been proven in various applications for many years. W5200 uses a 32KB internal buffer as its data communication memory. By using W5200, users can implement the Ethernet application they need by using a simple socket program instead of handling a complex Ethernet Controller. Further information may be found at www.wiznettechnology.com.

Figure 2-2. W52 Block Diagram.



2.3 Memory

The LCGW is designed with two external memory devices onboard. The Atmel AT24MAC402 2-Kbit TWI EEPROM is intended for persistent storage of EUI-48 or EUI-64 addresses. This device can be used to store MAC addresses, credentials, calibration data, manifests and security keys. The Atmel AT24MAC EEPROM has a hardwired address of 0x0. Additionally the LCGW includes an Atmel AT45DB642 4-Mbit SPI flash memory for in-the-field upgrades, web-site storage, logs, electronic data sheets (TEDS) or general purpose scratch pad. Detailed datasheets for these devices can be found at www.atmel.com. These two memory devices are useful for gateway and data concentrator applications but they are optional and can be omitted to further reduce BOM cost.

2.4 Power System

DC power is derived from a USB Dedicated Charging Port (DCP) inlet. The LCGW can be powered from common mobile-device chargers or USB ports on Wi-Fi access points or PCs using a USB Micro-B cable. For safety, the power bus is protected by an SMT fuse and ESD/EMI suppression circuitry. USB supplies 5VDC. A linear buck-regulator supplies the 3.3VDC rail for the CMOS devices. Connector J5 exposes the 5VDC and 3.3VDC rails for testing. The Power-Good indicator, D1, will light if both 5VDC and 3.3VDC are present. Additional low-voltage rails are regulated and filtered by the Ethernet sub-system.

2.5 Antenna

The RF front end is designed for low-cost and high efficiency. A PCB dipole antenna was chosen because it does not require an external balun or specialized RF components which add cost. Additionally, the relatively large area of this dipole design significantly increases the effective area and antenna aperture. Larger antenna aperture dramatically improves receiver efficiency, sensitivity and range. This dipole antenna offers performance superior to chip antennas for receiving weak signals from remote nodes in marginal conditions. This antenna design is on par with high-performance external monopole antennas at a fraction of the cost. The antenna radiation pattern of the LCGW is moderately directional. This can be used to advantage by adjusting the orientation to bring in weak signals. Conversely, conductive objects and obstructions can be placed in the null zones to reduce adverse effects. The unpopulated PCB area around the antenna is essential to sustain a strong electric field. The electric field radiates from both sides of the PCB, top and bottom. Do not put conductors, labels or stickers in this area.

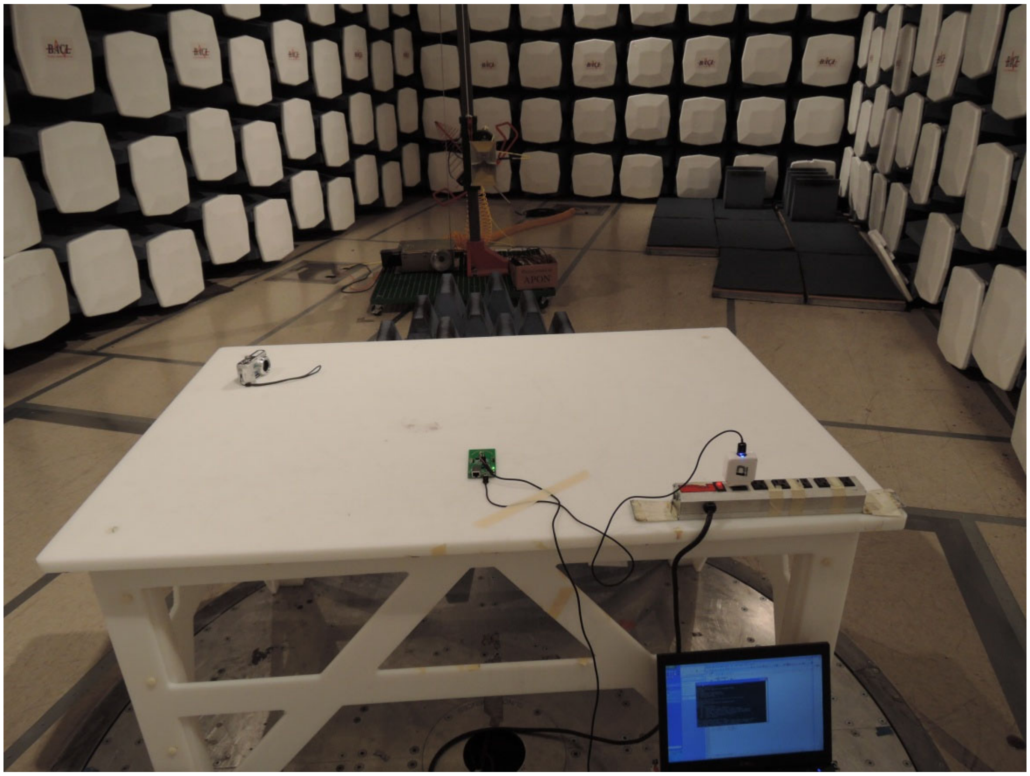
2.6 Enclosure

If LCGW is converted to a product for the general public will need to be mounted in an enclosure. Users can be very creative with enclosure design however there are a few guidelines for wireless devices. Any metal or conductive material, within 4 inches (10cm) of the antenna will have an effect on the far field radiation pattern. Metal enclosures should not be used. The suitability of plastic or other materials, for enclosures can be assessed with a household microwave oven. Place a sample of the material in the oven and cook it for a few seconds, if the material gets hot, or arcs, it should be avoided. Additionally, it is recommended to keep metal parts such as screws, nuts and washers, metallic labels away from the PCB antenna area. There are holes in the LCGW design that are the preferred location for fasteners. Using non-conductive fasteners is recommended.

2.7 Regulatory Compliance

The LCGW has been pre-tested for FCC Class B and CE compliance. Initial pre-scan data indicates this design is compliant with US and EU regulations. To obtain regulatory certification, developers will have to perform regulatory testing of their product in its final form including enclosure and all application specific features. Results may vary however; the positive pre-scan results are reassuring and indicate probability of successful certification is high.

Figure 2-3. Atmel LCGW in Test Chamber.



The Atmel ATmega256RFR2 SoC used in the LCGW has a special Band-edge filter feature. (See Section 9.12.8 of the ATmega256RFR2 datasheet.) This improves out-of-band rejection for channels 25 and 26 (2475 and 2480MHz.) The FCC defines a “Restricted Band” from 2483 to 2500MHz. Emissions in this Restricted Band are required to be below 54dBµV (500µV/m). Because of this requirement, many IEEE 802.15.4 devices are not able to use high power in channels 25 and 26. The Band-edge filter feature of Atmel RFR2 radios allows the use of higher power in these channels. The FCC pre-scan data cited in this document was taken using the full output power of the ATmega256RFR2 (+3.5dBm) and the Band-Edge feature enabled. The filer can be enabled by setting PLL_TX_FLT (bit 4) in the TRX_CTRL_1 (0x144) register. The pictures below show the effects of this filter and the regulatory limit-line.

Figure 2-4. No Band-edge Filter. FAIL.

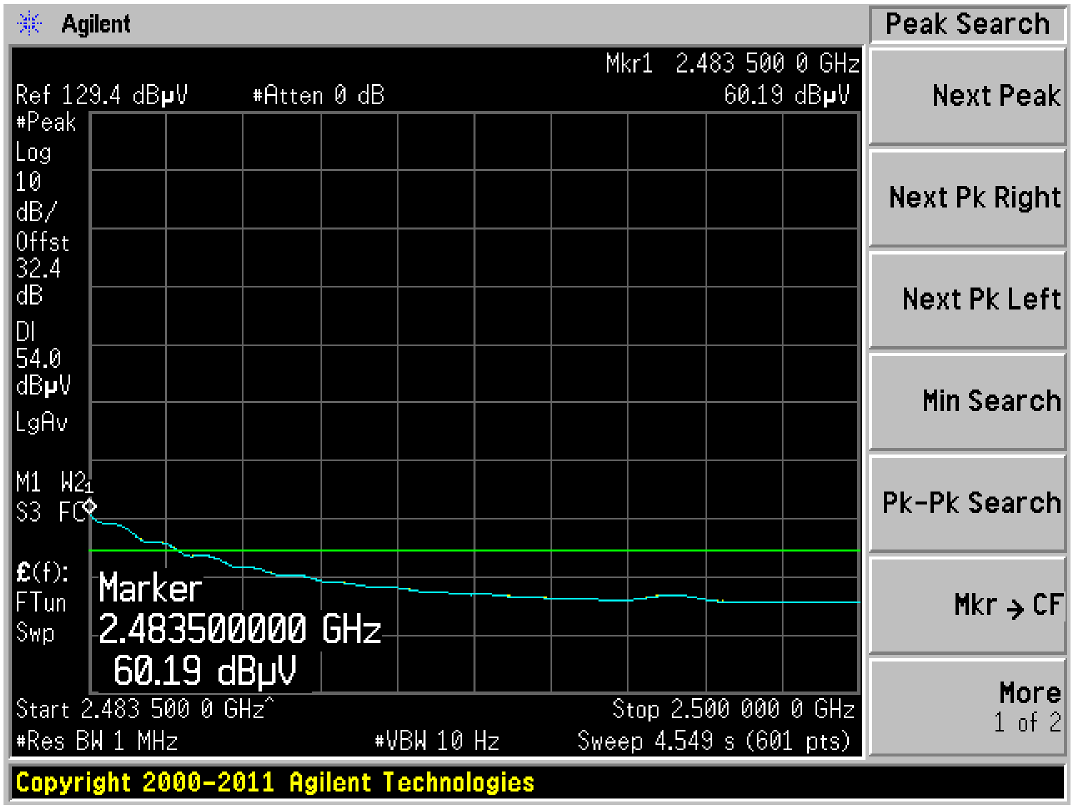
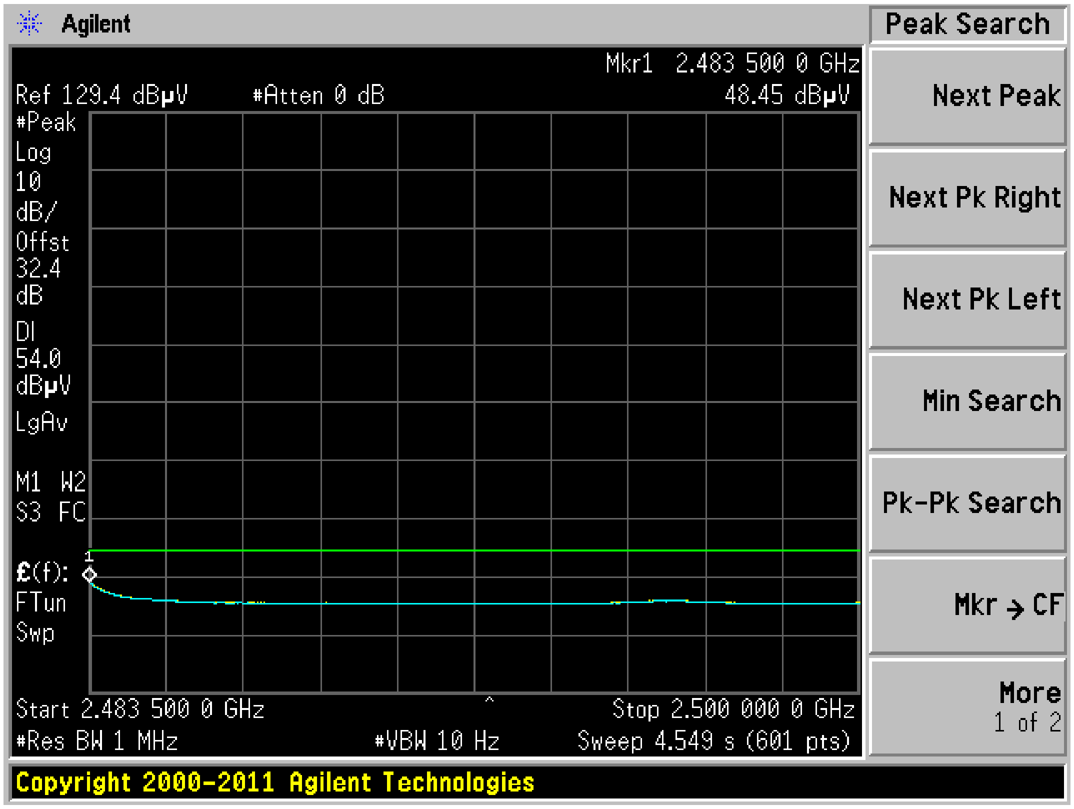


Figure 2-5. Band-edge Filter Enabled. PASS.



3. Pin Assignment

Table 3-1. LCGW Pin Assignment.

Pin	Signal	Group
J1.01	PF4-TCK	JTAG
J1.02	GND	JTAG
J1.03	PF6-TDO	JTAG
J1.04	3.3V	JTAG
J1.05	PF5-TMS	JTAG
J1.06	RESET*	JTAG
J1.07	N/C	JTAG
J1.08	N/C	JTAG
J1.09	PF7-TDI	JTAG
J1.10	GND	JTAG
J2.1	GND	USER UART
J2.2	PE1-TX0	USER UART
J2.3	PE0-RX0	USER UART
J5.1	GND	PWR TEST
J5.2	3.3V	PWR TEST
J5.3	USB_5V0	PWR TEST
J6.1	GND	USER GPIO
J6.2	PF2-ADC2	USER GPIO
J6.3	PF3-ADC3	USER GPIO

4. Debugging, Limitations and Advisory Caveats

For safety, the DCP power inlet is fused. If the Power-Good LED fails to light, check the fuse. If the fuse has blown and needs to be replaced, the root cause should be determined before putting the device back into service. For replacement parts a 1 Amp 0603 SMT fuse is recommended (Bourns SF-0603S100, or equivalent.)

Do not use flipped CAT5 cables.

Use caution connecting to Power Test Header J5. This header exposes 5VDC and may damage low voltage GPIO or UART cables.

Using the 3.3V supply for light external loads is permissible however be advised: The 3.3V LDO has limitations on available line current, load current and thermal dissipation. Exceeding theses limits may cause a malfunction.

At maximum transmitter power the Atmel ATmega256RFR2 may exceed emissions limits in the 2483 to 2500MHz restricted band. This can be corrected by enabling the PLL_TX_FLT bit in the TRX_CTRL_1 register. This special band-edge filtering feature of the Atmel RFR2 family allows use of high-power in channels 25 and 26. See Section 9.12.8 of the ATmega256RFR2 datasheet for complete details.

5. Software Resources

Atmel supplies many network stacks that run on the Atmel ATmgea256RFR2. These include the BitCloud® ZigBee® stacks, ZigBee Pro, ZigBee Light Link and ZigBee Home Automation, IEEE 802.15.4 MAC and the Atmel proprietary Light-Weight Mesh network stack. An example application using the LCGW, ATmega256RFR2 Xplained Pro remote nodes and an Android device is being released to accompany this reference design. This will include drivers for the WIZ5200 and example code. Developers may also use the MACRAW mode of the WIZ5200 and a third-party upper layer protocol. This reference design is released with an RF diagnostic application from the Atmel IEEE 802.15.4 MAC software package.

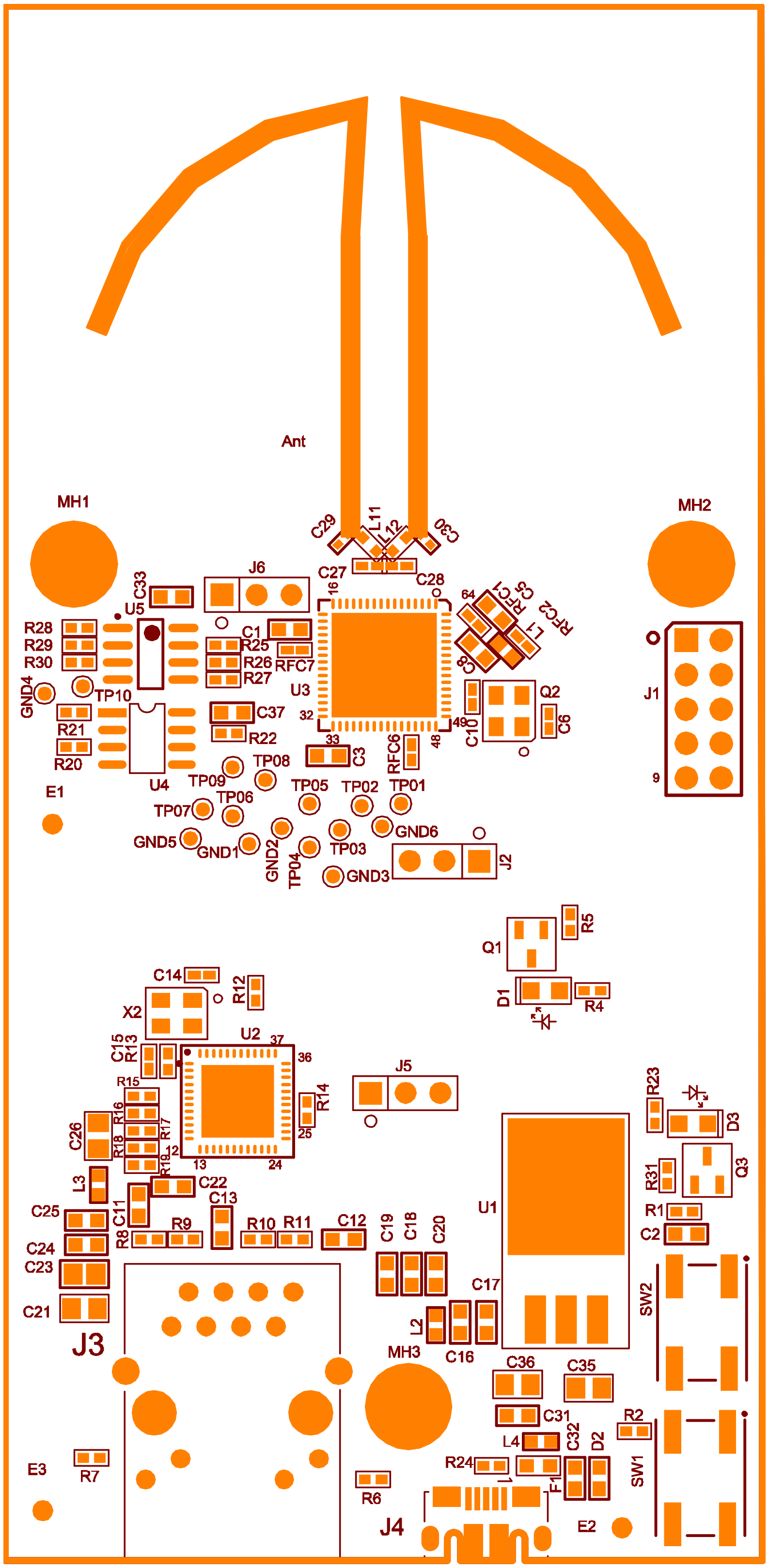
6. General Specifications

Table 6-1. LCGW General Specifications.

Parameter	Value	Unit
Size	4.5 x 2.2 x 0.7	Inch
Size	11.4 x 5.5 x 1.7	Cm
Weight	<1.0	Oz
Weight	<28	Gram
Voltage	5	VDC
Current	175	mA
Power connector	USB Micro-B	
RF TX power	+3.5	dBm
Frequency	2405 – 2480	MHz
Ethernet	10/100 BASE-T	Mb/S
Ethernet connector	RJ45	
Color	Green	
ROHS	Yes	
OP temp	-40 to +85	°C

7. Build Package

Figure 7-1. LCGW Assembly Drawing.



The ultimate goal of this reference design is to give Atmel customers a head-start on their own gateway products. This appnote includes manufacturing documents ready for release to manufacturing teams. The documents provided were used as-is to build the devices characterized in this app-note. As a pedagogical example, this design was implemented using common manufacturing practices and easily obtainable components. These documents are believed to be accurate however, omissions and errors may exist. Furthermore manufacturing guidelines, rules and abilities vary within different organizations. The customer is ultimately responsible for reviewing these materials and determining the suitability for production.

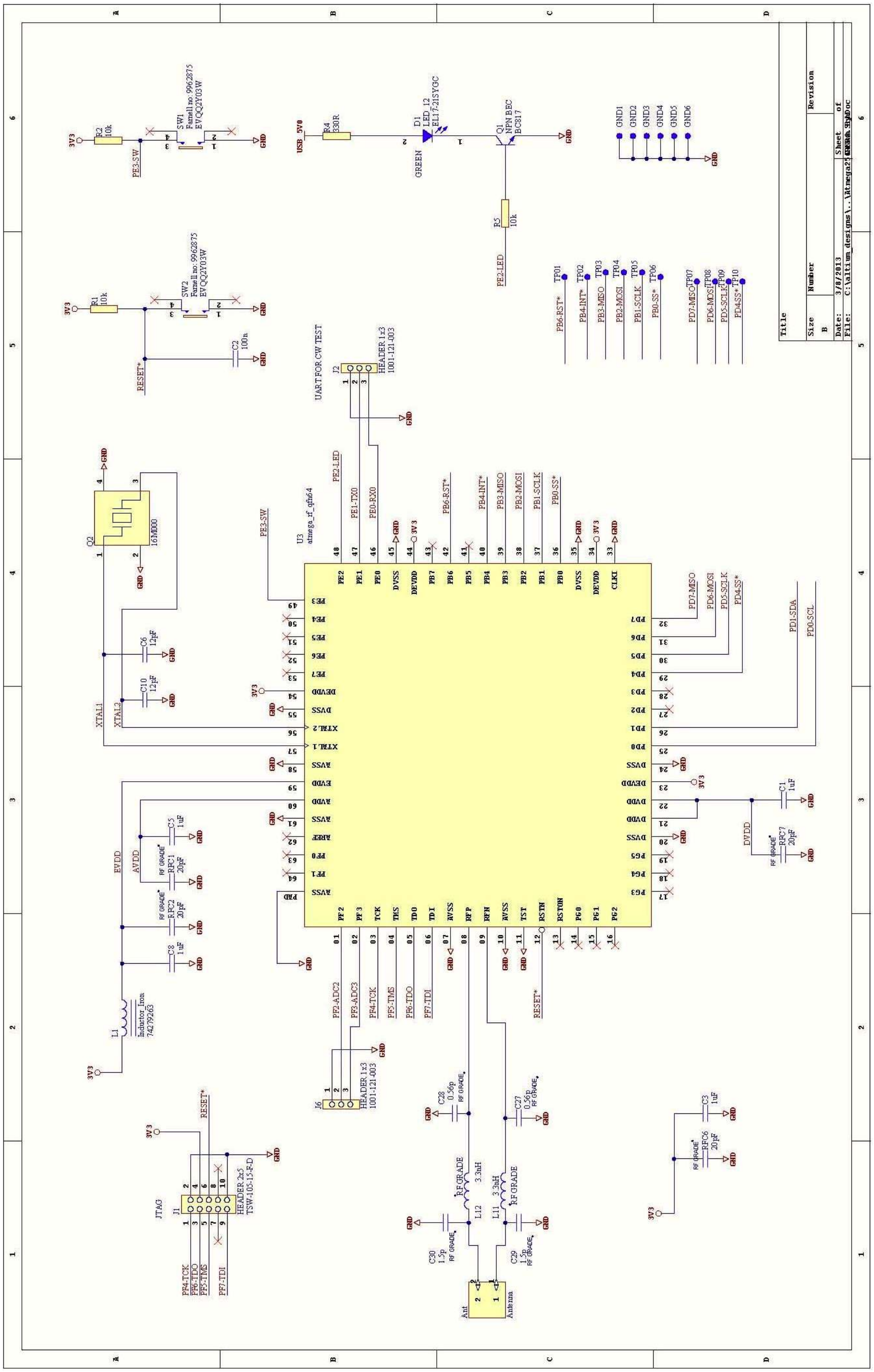
One of the goals of this design was low BOM cost. A ‘costed’ BOM is included for reference. The budgetary prices shown are for small quantities from popular retail distributors. Pricing is expected to fall off considerably as volume increases. Developers are encouraged to get market-price quotations from Atmel and other manufacturers based on accurate volumes and forecasting.

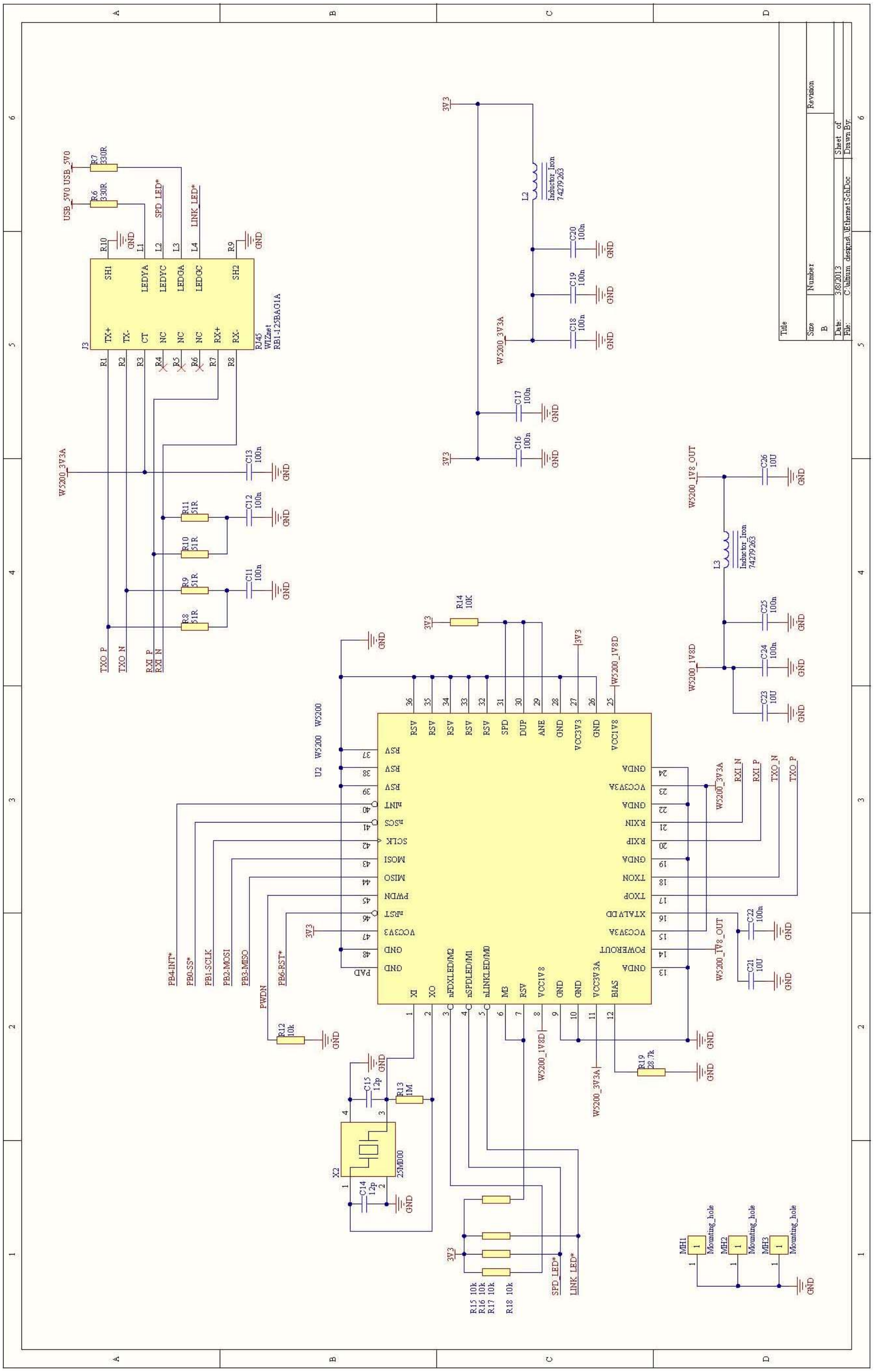
8. Components and Alternate Sources

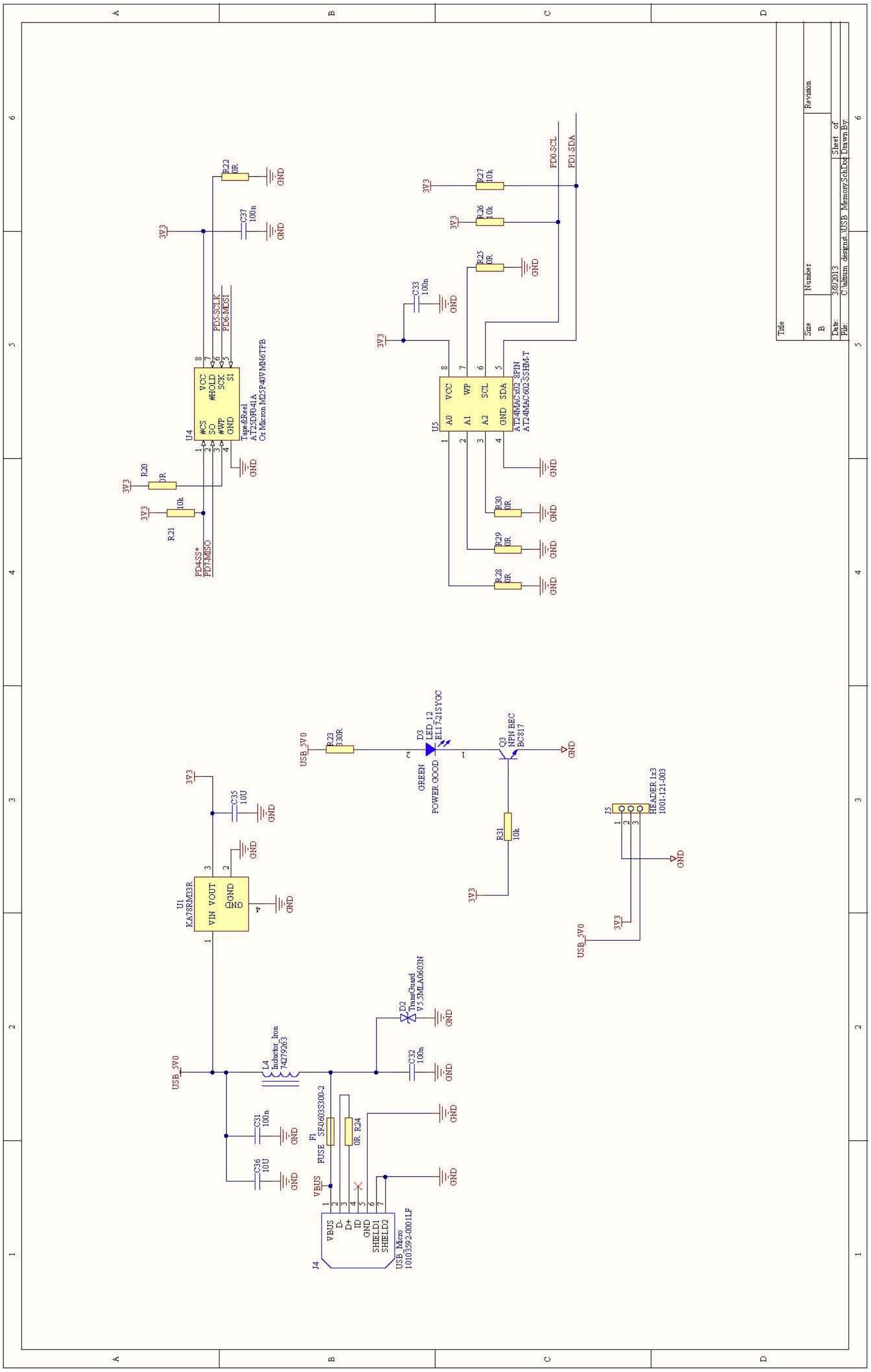
Contract Manufacturers and Materials Managers will want to substitute components. Substitution of passives in the RF signal-chain is risky. This design was tested using Murata brand GJM capacitors and LQG inductors. These devices are recommended. If substitution is necessary in the RF signal-chain top quality high-frequency components from reliable vendors should be used. Also the tolerance, drift and phase-noise of 16MHz crystal will affect the RF Carrier and may adversely impact regulatory compliance. Substitutions in these sub-systems will require evaluation by a qualified Engineer.

Appendix A.

A.1 Schematics




U2 W5200
J3
RJ45
WIZnet
RB1-125BAG1A
X2
25M000
Inductor_Iron
74279263
Mounting_hole
W5200_3V3A
W5200_1V8D
W5200_1V8_OUT
USB_5V0
SPD_LED*
LINK_LED*
TXO_P
TXO_N
RXI_P
RXI_N
PB4-INT*
PB0-SS*
PB1-SCLK
PB2-MOSI
PB3-MISO
PWDN
PB6-RST*
GND
3V3


U4
AT25DF041A
Or Micron M25P40VMN6TPB
Tape&Reel
U5
AT24MAC602_8PIN
AT24MAC602-SSHM-T
PD0-SCL
PD1-SDA
PD5-SCLK
PD6-MOSI
PD4-SS*
PD7-MISO
U1
KA78RM33R
D3
LED_12
EL17-21SYGC
GREEN
POWER GOOD
Q3
NPN BEC
BC817
J5
HEADER 1x3
1001-121-003
J4
USB_Micro
10103592-0001LF
L4
Inductor_Iron
74279263
F1
FUSE
SF-0603S300-2
D2
TransGuard
V5.5MLA0603N
USB_5V0
3V3
GND
Title
Size
Number
Revision
Date:
File:
Sheet of
Drawn By:

A.2 Costed BOM

LOW-COST GATEWAY BILL OF MATERIALS

CUSTOMER: ATMEL
PROJECT : lc_gateway
REVISION: 2
DATE : 3/4/2013

Item	QT	Designator	VAL	MPN	Manufacturer	COST_EA_1K	COST	Description
1	2	L11, L12	3.3 nH	LQG18HN3N3S00D	Murata	0.097	0.194	SMD RF inductor 0603.
2	1	Ant					0.000	
3	1	U3		ATMEGA256RFR2-ZU	Atmel	6.300	6.300	Atmega RF Soc QFN 64
4	1	J3		RB1-125BAG1A	WIZnet	1.760	1.760	CONN MAGJACK 1PORT 100 BASE-T
5	7	R20, R22, R24, R25, R28, R29, R30	0R			0.003	0.021	Thick film resistor, SMD 0402, 1/16W, 1%
6	2	C27, C28	0.56p	GJM1555C1HR50WB01D	Murata	0.038	0.076	Ceramic capacitor, SMD 0402, NP0, 50V, +/-0.05pF
7	1	R13	1M			0.003	0.003	Thick film resistor, SMD 0402, 1/16W, 1%
8	4	C1, C3, C5, C8	1uF	0603YC104KAT2A	AVX	0.012	0.048	Ceramic capacitor, SMD 0603, X7R, 16V, □10 %
9	2	C29, C30	1.5p	GJM1555C1H1R5WB01D	Murata	0.038	0.076	Ceramic capacitor, SMD 0402, NP0, 50V, +/-0.25pF
10	1	U1	3V30	KA78RM33RTF	Fairchild	0.237	0.237	KA78RM33R LDO 3.3V D-PAK
11	13	R1, R2, R5, R12, R14, R15, R16, R17, R18, R21, R26, R27, R31	10k			0.003	0.039	Thick film resistor, SMD 0402, 1/16W, 1%
12	5	C21, C23, C26, C35, C36	10U	C2012X5R1E106K	tdk	0.046	0.230	Ceramic capacitor, SMD 0805, X5R, 25V, □10%
13	4	C14, C15, C6, C10	12p	GJM1555C1H150JB01D	Murata	0.038	0.152	Ceramic capacitor, SMD 0402, NP0, 50V, +/-5%
							0.000	
15	1	X1	16M000	ABM8-16.000MHZ-10-1-U-T	ABRACON	1.008	1.008	CRYSTAL 16.000 MHZ 10PF SMD
16	4	RFC1, RFC2, RFC6, RFC7	20pF	GJM1555C1H200GB01D	Murata	0.038	0.152	Ceramic capacitor, SMD 0402, C0G, 50V, +/-5%
17	1	X2	25M000	ABM8-25.000MHZ-B2-T	ABRACON	0.756	0.756	CRYSTAL 16.000 MHZ 10PF SMD
18	1	R19	28.7k			0.003	0.003	Thick film resistor, SMD 0402, 1/16W, 1%
19	4	R8, R9, R10, R11	51R			0.003	0.012	Thick film resistor, SMD 0402, 1/16W, 1%
20	16	C2, C11, C12, C13, C16, C17, C18, C19, C20, C22, C24, C25, C31, C32, C33, C37	100n	0603YC104KAT2A	AVX	0.012	0.192	Ceramic capacitor, SMD 0603, X7R, 16V, □10 %
21	4	R4, R6, R7, R23	330R			0.003	0.012	Thick film resistor, SMD 0402, 1/16W, 1%
22	3	J2, J5, J6	1001-121-003	TSW-103-05-T-S	SAMTEC	0.140	0.420	Pin Header 1x3, 2,54mm THM (de3572)
23	1	J4	10103592-0001LF	10103592-0001LF	FCI	0.345	0.345	Micro USB B Connector
24	4	L1, L2, L3, L4	74279263	74279263	Wurth Elektronik	0.074	0.296	FERRITE BEAD 220 OHM .5A 0603
25	1	U5	AT24MAC602-SSHM-T	AT24MAC602-SSHM-T	ATMEL	0.288	0.288	I2C EEPROM w/ EUI-64 MAC ID SOIC8
26	1	U4	AT25DF041A	AT25DF041A-SSHF-B	ATMEL	0.740	0.740	4Mbit SPI serial flash memory (de32610)
27	2	Q1, Q3	BC817	BC817-40-7-F	Diodes Incorporated	0.035	0.069	General purpose SMD small signal BJT transistor. Polarity:NPN, Body:SOT23,
28	2	D1, D3	EL17-21SYGC	APT2012CGCK	Kingbright	0.066	0.132	LED, Green, Wave length=575nm, SMD 0805, □70□
29	2	SW1, SW2	EVQQ2Y03W	EVQQ2Y03W	Panasonic	0.161	0.322	6.5x6.0 mm SMD pushbutton, 10ms bounce, 3.5N force
30	3	E1, E2, E3	FIDUCIAL 1.5mm				0.000	Fiducial point for PCB coordinates 1.5mm pad and 3mm hole in mask
31	1	F1	SF-0603S300-2	SF-0603S300-2	Bourns	0.216	0.216	Slow Blow Surface Mount Fuse, 32V, 3A, 0603
32	16	GND1, GND2, GND3, GND4, GND5, GND6, TP01, TP02, TP03, TP04, TP05, TP06, TP07, TP08, TP09, TP10	Surface mount pads				0.000	Single thru-hole testpin
33	1	J1	TSW-105-15-F-D	TSW-105-08-G-D	SAMTEC	0.865	0.865	(Can be replaced by A08-1209 to avoid bend) 2x5 pin header, 2.54 mm pitch, P=13.2mm, THM, Flash selective gold,
34	1	D2	V5.5MLA0603N	V5.5MLA0603N	Littelfuse	0.217	0.217	Transient Voltage Surge Suppression (de35029)
35	1	U2	W5200	W5200	WIZnet	4.331	4.331	Ethernet Controller
36	3	MH1, MH2, MH3	Mounting_Hole				0.000	
37	1	lc_gateway Board PCB	305-PD-13-xxxx			0.500	0.500	

20.012 Total PCBA cost

A.3 Antenna Patterns

Figure A-1. LCGW Antenna Pattern XY Horizontal Polarity.

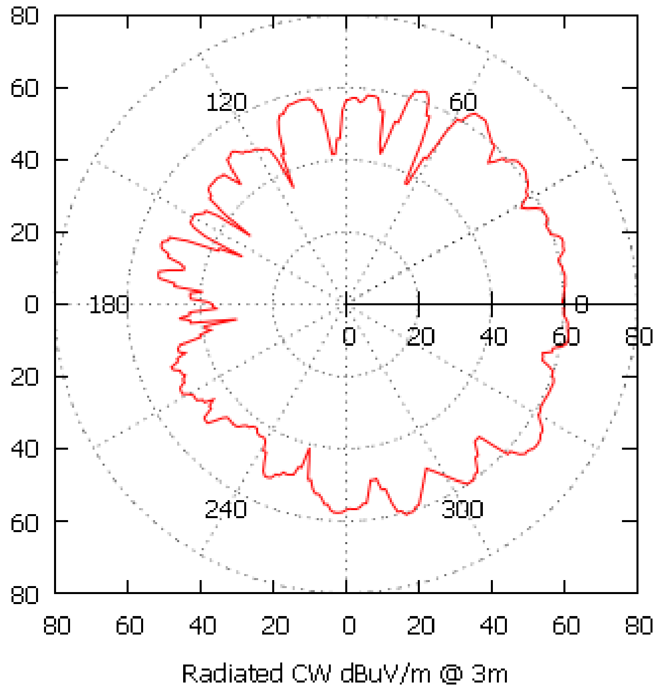


Figure A-2. LCGW Antenna Pattern XY Vertical Polarity.

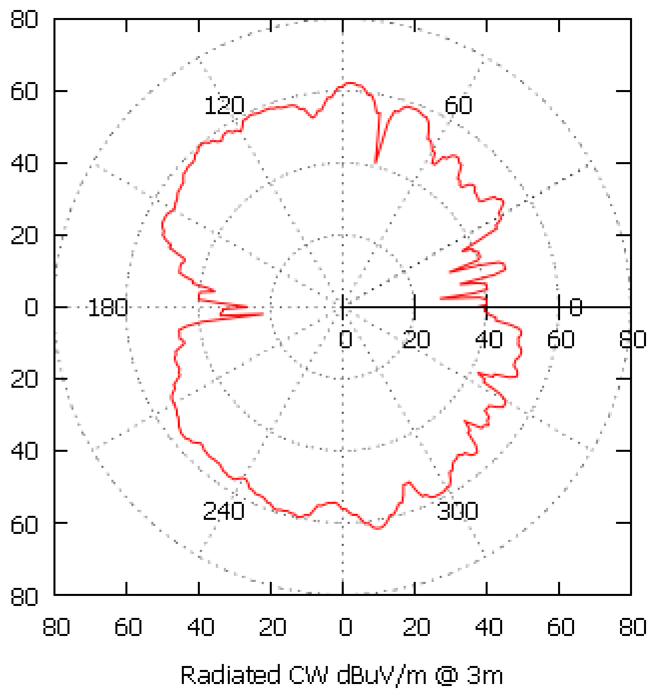


Figure A-3. LCGW Antenna Pattern YZ Horizontal Polarity.

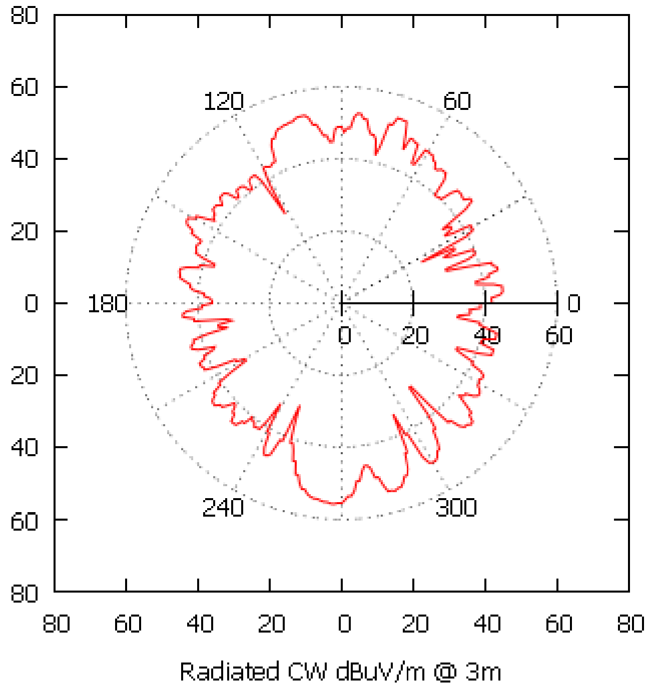
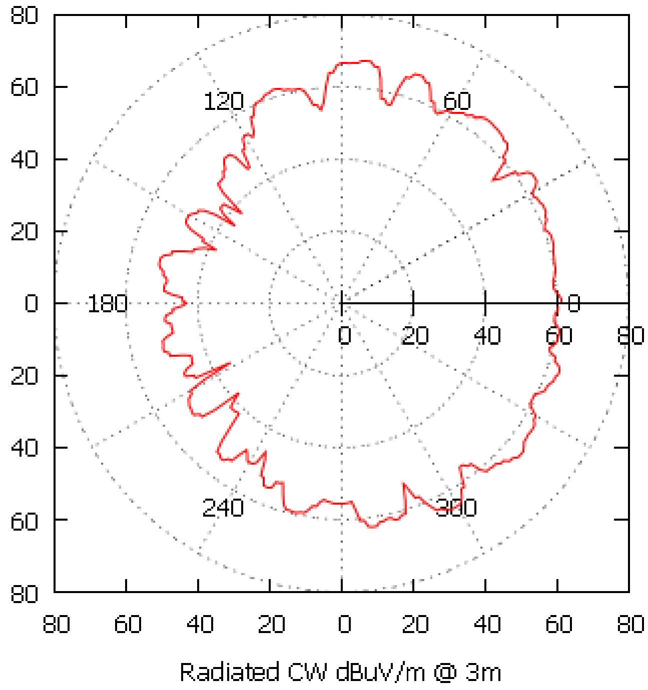


Figure A-4. LCGW Antenna Pattern YZ Vertical Polarity.



Appendix B. Revision History

Doc. Rev.	Date	Comments
42150A	07/2013	Initial document release

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