APPLICATION NOTE

Discrete Power Supply Solution for Atmel SAMA5D4

Atmel | SMART SAMA5D4 Series

Scope

A wide variety of applications based on Atmel® | SMART SAMA5D4x embedded MPUs (eMPUs) can be powered from a low-cost power supply solution based on discrete components.

This application note provides developers with a recommended application schematic and associated functional descriptions.

Reference Documents

Type	Title	Atmel Lit. No.
Datasheet	SAMA5D4 Datasheet	11238

Table of Contents

1. Power Supply Overview of Atmel eMPU Systems

1.1 Atmel SAMA5D4x Power Rails

Atmel SAMA5D4x eMPUs power rails and their respective operating ranges are listed in Table 1-1. An approximate current consumption is provided for each rail in order to size the corresponding regulator. Accurate numbers and descriptions are provided in the SAMA5D4 datasheet.

Depending on the application complexity, SAMA5D4x power input pins may be grouped into two (e.g., 3.3V + 1.8V), three (e.g., 3.3V + 1.8V + 1.2V) or more power planes. In secure applications, or any application that requires writing into the internal fuse box, an additional 2.5V power rail is needed to supply the VDDFUSE input pin.

The SAMA5D4x series also features a backup power domain to retain information during power-down periods by means of a storage element (e.g., a battery or a super-capacitor). It is supplied by the VDDBU pin and must be fed through a 2V regulator.

Table 1-1. SAMA5D4x Series Power Supply Inputs

Power Rail	Circuit Supplied by the Power Rail	Range	Consumption
VDDCORE	Core Voltage Regulator	1.62–1.98V, 1.80V	0.35A
VDDIODDR	External Memory Interface I/O lines	1.70–1.90V, 1.80V 1.14–1.32V, 1.20V	0.05A 0.03A
VDDIOM	NAND and HSMC Interface I/O lines	1.65–1.95V, 1.80V 3.00–3.60V, 3.30V	0.03A
VDDIOP	Peripheral I/O lines	1.65–3.60V	0.03A
VDDUTMIC	USB Device and host UTMI+ core logic and UTMI PLL	1.10–1.32V, 1.20V	0.02A
VDDUTMII	USB Device and host UTMI+ interface	3.00–3.60V, 3.30V	0.02A
VDDPLLA	PLLA	1.10–1.32V, 1.20V	0.02A
VDDOSC	Main oscillator	1.65–3.60V, 3.30V	0.001A
VDDANA	Analog-to-Digital Converter, and other analog circuits	3.00–3.60V, 3.30V	–
VDDFUSE	Programmable Fuse Box	2.25–2.75V, 2.50V	0.05A
VDDBU	Backup domain	1.88–2.12V, 2.00V	0.0001A

In all modes other than Backup mode, each power supply input must be powered to operate the device. The only exception is the VDDFUSE input which can be left unpowered if the fuse box is not used in Write mode.

1.2 Atmel SAMA5D4x VCCCORE Generation

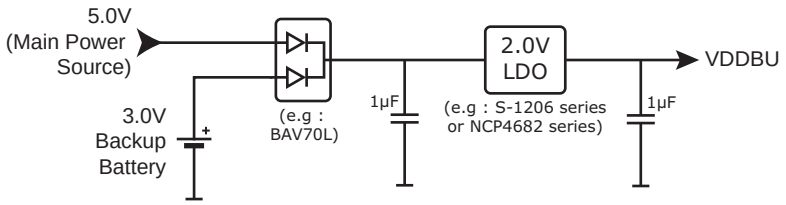
Atmel SAMA5D4x devices embed a linear low dropout (LDO) voltage regulator to generate their core logic power supply (VCCCORE). The input of this regulator is VDDCORE and its output is internally connected to some of the VCCCORE pins. The remaining VCCCORE pins are fed from the VCCCORE plane of the printed circuit board (PCB). This plane must contain at least one 10µF capacitor (max 20µF) to ensure the regulator stability. Additional 10nF to 100nF capacitors of X5R or X7R type must be connected to each VCCCORE pin for proper decoupling.

This LDO voltage regulator cannot be shut down. Therefore the VCCCORE pins cannot be fed by an external voltage regulator at the risk of creating a short circuit between the internal regulator and the external one.

1.3 Atmel SAMA5D4x VDDBU Generation

The SAMA5D4x series embeds a backup power domain which supplies a Real-Time Clock circuit, a backup memory and others. This power domain is designed for ultra-low-power consumption (8µA typ.) and is therefore suited to be supplied by a storage element such as a super-capacitor or a battery. The operating range of VDDBU (2V±120mV) calls for the use of an external voltage regulator. Low-power LDO regulators in the S-1206 series from Seiko Instruments and NCP4682 series from ON Semiconductor with a typical 1µA operating current meet the criteria.

Figure 1-1. VDDBU Generation



As described in the SAMA5D4x series datasheet, the VDDBU power supply must always be the first power source applied to the system and the last one disconnected from the system. It is therefore good practice to monitor the storage element discharge in order to shutdown the system before the VDDBU voltage goes out of its operating range,

If the backup functionality of the SAMA5D4x device is not used in the application, VDDBU can be fed directly from the main power source through a 2.0V regulator. In this case, a low-power regulator is not necessary. A generic low-cost device (e.g. TLV431A or equivalent) can be chosen. In case of input power loss, small storage capacitors (e.g., 1µF) help to extend the presence of the VDDBU voltage after a system shutdown as specified in the device datasheet.

1.4 Power Supply Topologies and Power Distribution

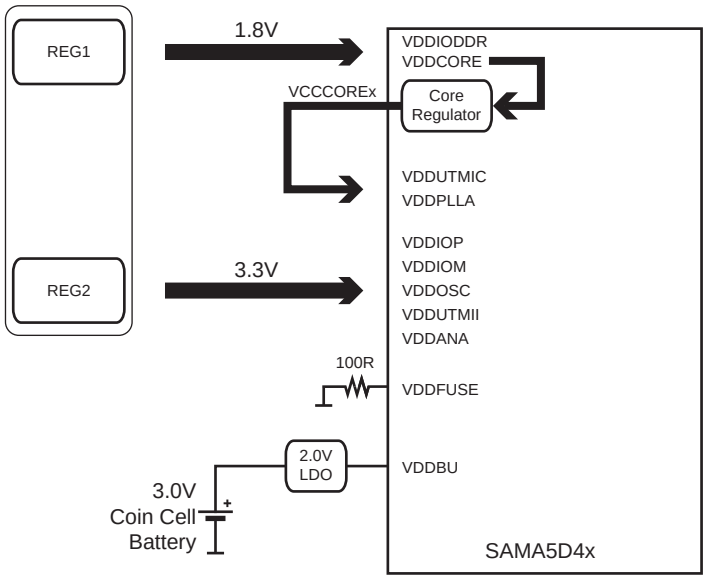
1.4.1 2-channel Topology with 1.8V (DDR2 or LPDDR) Memories

When SAMA5D4x devices are equipped with 1.8V external memories (LPDDR or DDR2 type), the lowest cost power supply is achieved by implementing a 2-rail topology (3.3V / 1.8V) as shown in Figure 1-2. While optimized from a system cost perspective, this topology has the following limitations:

- The fuse box cannot be accessed in Write mode because VDDFUSE = 0V.
- The analog section of the device (VDDANA) is powered from the (noisy) digital 3.3V rail.

These limitations can be overcome by adding two regulators for VDDANA and VDDFUSE. In such case, these regulators should be enabled and disabled along with the main 3.3V regulator.

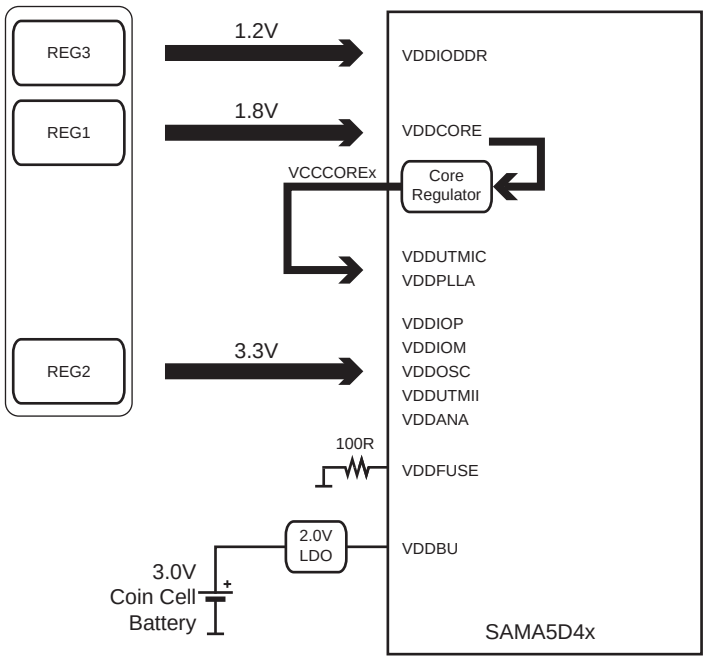
Figure 1-2. 2-channel Power Supply Example on SAMA5D4x Series Equipped with a 1.8V External Memory



1.4.2 3-channel Topology with (1.2V / 1.8V) LPDDR2 memories

The 2-channel topology can be extended to support LPDDR2-type external memories. An additional 1.2V voltage regulator is added to supply the LPDDR2 interface. See Figure 1-3.

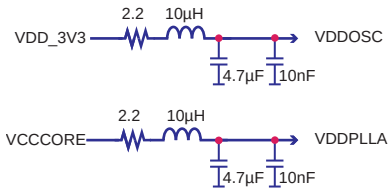
Figure 1-3. 3-channel Power Supply Example on SAMA5D4x Series (LPDDR2 support)



1.5 Clock Circuits Power Supply

Atmel eMPUs have separate power supply inputs for their oscillators and PLL circuits. These analog circuits can be decoupled from the digital (core and I/Os) activity of the device and thus generate less jittered clocks. Atmel highly recommends feeding these power supply inputs with low-noise sources for applications where clock jitter is important (e.g., high-speed USB). The simplest way to do this is to filter the digital rails with an LC network as shown in Figure 1-4. Choosing a 20 kHz corner frequency is a good trade-off between component size/cost and the necessary high-frequency attenuation for clock circuits. The inductors must be sized for low DC resistance and good DC superimposition characteristics (TDK MLZ series and Taiyo Yuden CBM series are possible choices). The serial resistor in the filter schematic must be adjusted to take the inductor DCR into account. Example of inductors: Taiyo Yuden CBMF1608T100K (10 µH, 0.36 Ω, 115 mA, 0603) and TDK MLZ1608N100L (10 µH, 0.6 Ω, 60 mA, 0603).

Figure 1-4. Recommended Filter on Clock Circuits Power Supply



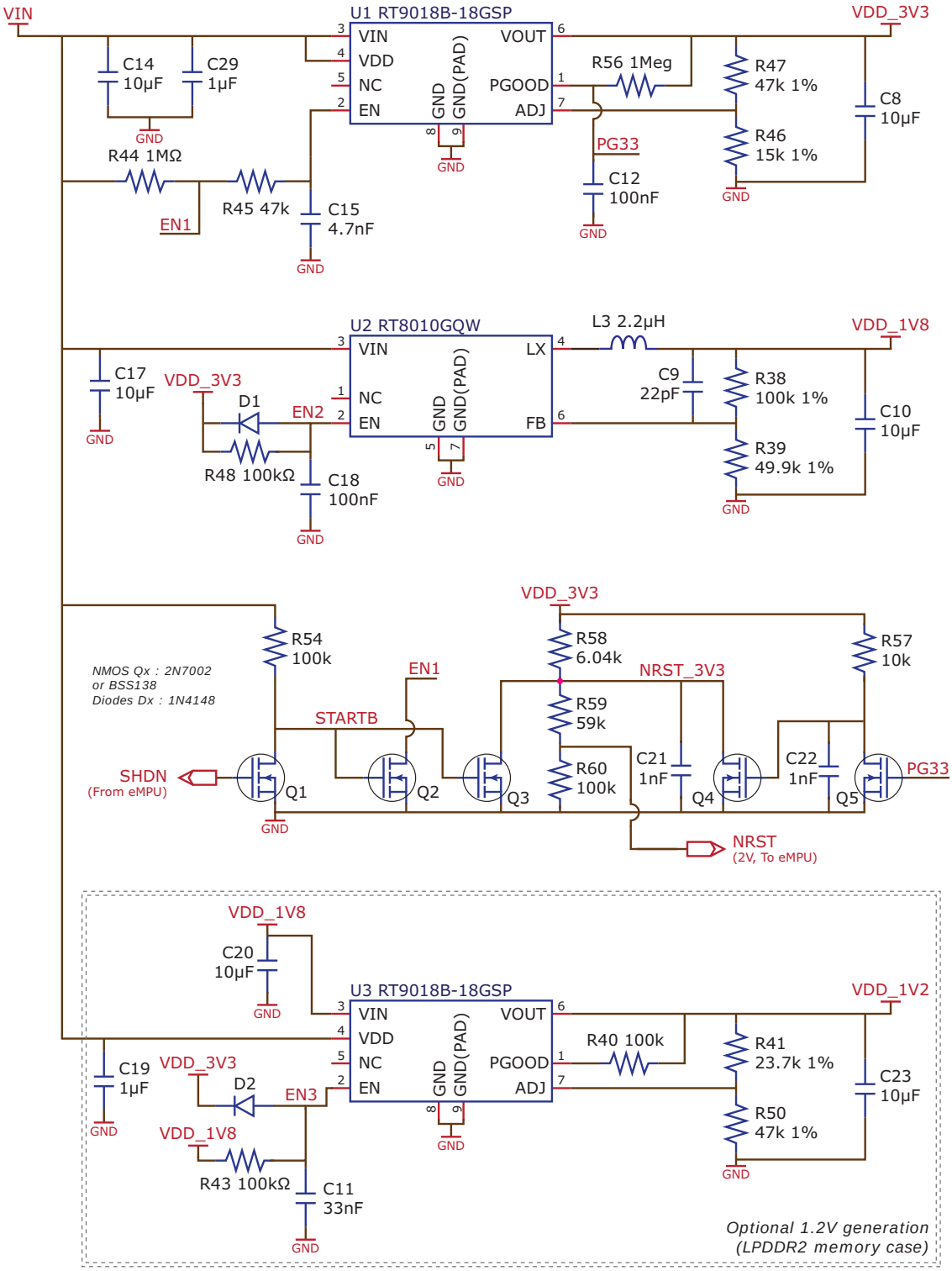
1.6 Power Supplies Monitoring

Atmel MPU power rails are not internally monitored. In low-cost systems, when the input power can be removed without advising the application, it is recommended to monitor the input voltage to detect the input power loss. In this power-fail case, the application should start a power-off sequence. This is particularly relevant in SAMA5D4 systems equipped with LPDDR2 memories for which uncontrolled power-off conditions may lead to damage to the memory IC.

2. Reference Schematic and Description

2.1 Basic Reference Schematic

Figure 2-1. Basic Reference Schematic



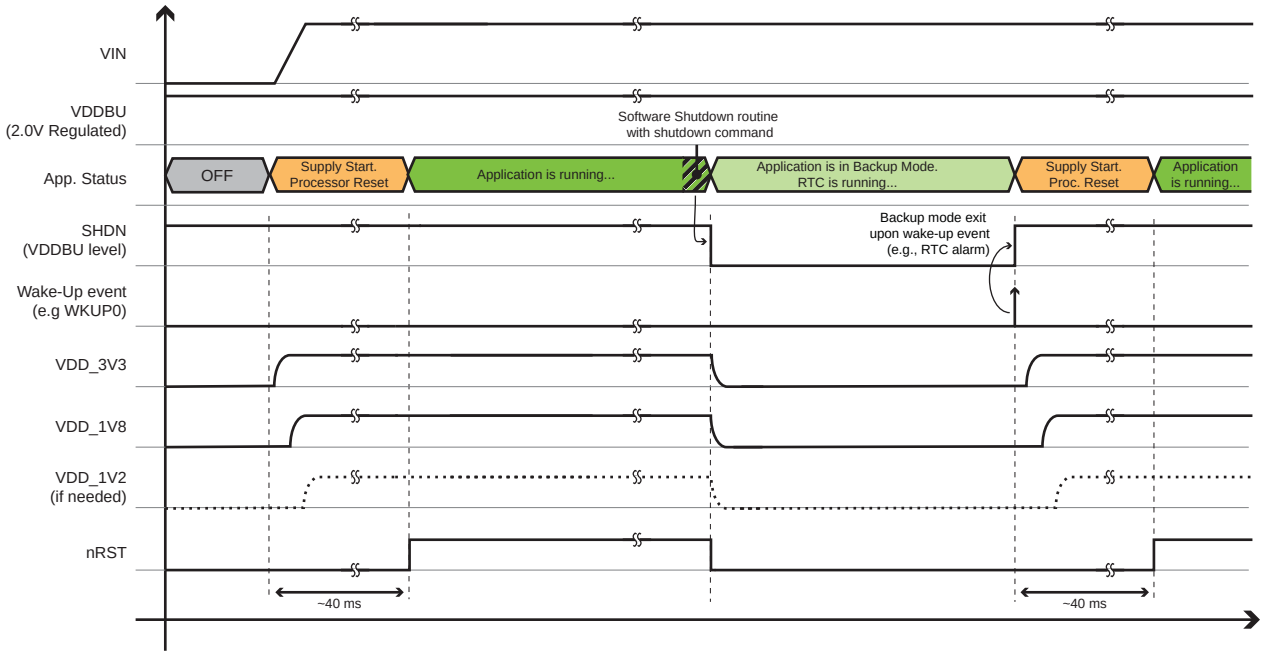
In this schematic, the power input VIN ranges from 3.5V to 5.5V. The lower limit (3.5V) is set by the need to generate a 3.3V voltage (VDD_3V3) to feed some of the eMPU rails.

VIN supplies a linear low dropout regulator (U1) to make the VDD_3V3 voltage and a DCDC buck regulator (U2) to make the VDD_1V8 voltage. In designs embedding an LPDDR2 memory, an optional VDD_1V2 supply channel can be built from the VDD_1V8 rail with a low input voltage low dropout regulator (U3).

Low-cost discretes are used to control the regulators' enable pins (EN) and the NRST signal of the SAMA5D4 device. As demonstrated in the following, this schematic ensures proper supply sequencing and reset assertion during power-up and power-down phases.

This power supply is designed to be controlled by the eMPU Shutdown Controller (SHDWC) and its SHDN pin. Refer to the section "Shutdown Controller (SHDWC)" in the SAMA5D4 datasheet for a complete description. In summary, SHDN is high when the eMPU is running, and SHDN is low when the eMPU goes to Backup mode or to OFF mode. The SHDN pin defaults to '1' (VDDBU level) when VDDBU is first applied. Figure 2-2 shows a typical application timing diagram and in particular the use of the Shutdown Controller.

Figure 2-2. Typical Application Timing Diagram



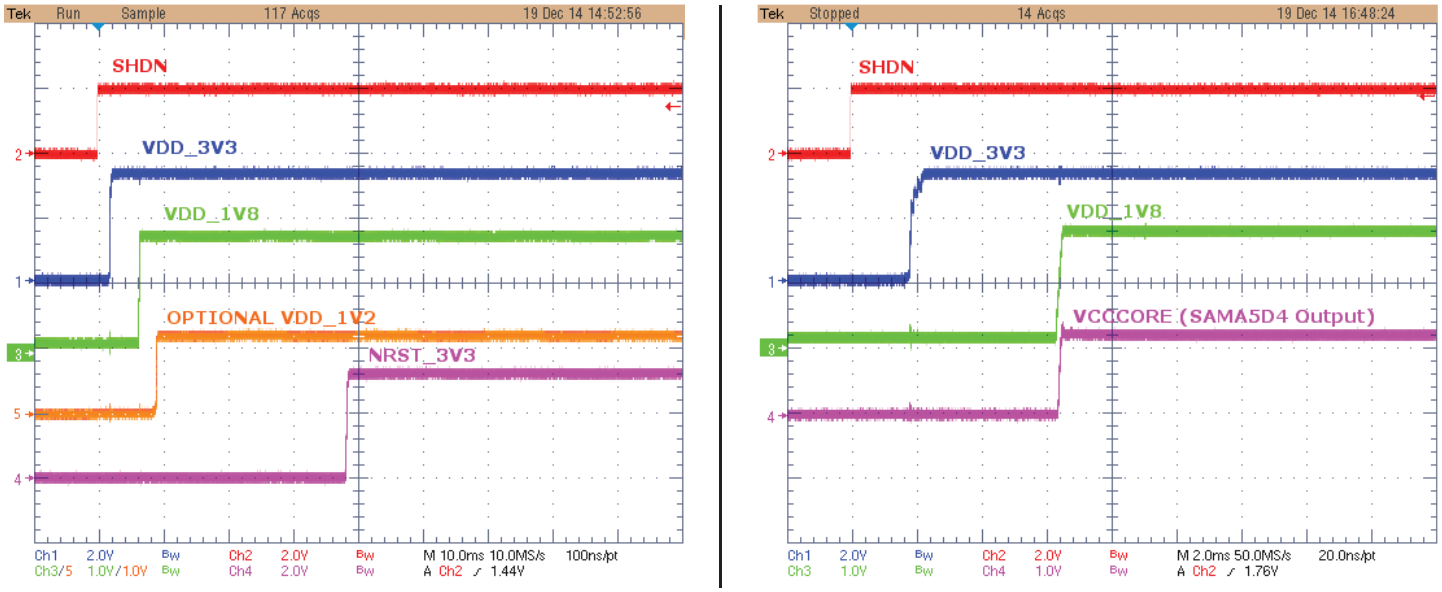
2.2 Wake-Up and Shutdown Description

2.2.1 Wake-Up Description

Figure 2-3 shows the typical wake-up waveforms of the basic reference schematic power supply. In the left-hand image, upon a wake-up event (not shown here), the processor pulls the SHDN pin high (VDDBU level 2.0V) and exits Backup mode. SHDN is applied through Q1 and Q2 to the enable pin of U1. The delay between SHDN and the start of regulator U1 is tuned with the (R44 + R45) / C15 network (here about 2ms, shown in the right-hand image). U1 starts regulating the VDD_3V3 output to 3.3V which enables the U2 regulator through the R48 / C18 delay network (here about 5ms). When applicable, regulator U3 is started by VDD_1V8 presence through the R43 / C11 delay network (here about 3ms). When VDD_1V8 rises, SAMA5D4's internal VCCCORE LDO regulator starts to regulate VCCCORE to 1.2V (See right-hand figure).

During this startup phase, the processor is held in reset (NRST low) with a delayed version of the PGOOD (power-good) output of U1. The delay network is made by (R56 / C12), here about 35ms. Q4 / Q5 / R56 / C13 shape the slowly rising PG33 signal. The resistor ladder R58 / R59 / R60 makes a 2V level reset signal (NRST) for the SAMA5D4 device and a generic 3.3V reset signal (NRST_3V3) for other components on the board.

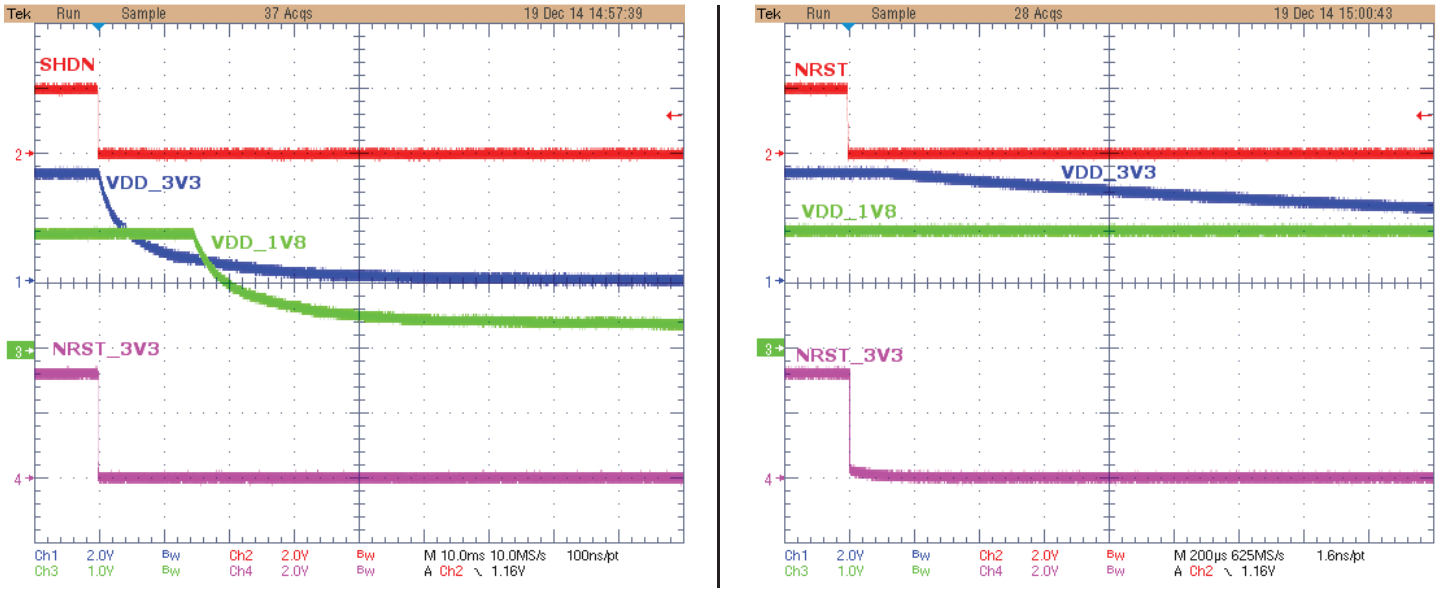
Figure 2-3. Wake-up Waveforms



2.2.2 Shutdown Description

Figure 2-4 shows the typical shutdown waveforms of the reference schematic power supply. In the left-hand image, upon a shutdown request in the Shutdown Control register (SHDW_CR), the processor pulls the SHDN pin low and enters Backup mode. NRST is almost immediately pulled low through Q1, Q2 and Q3. The delay between the SHDN falling edge and the NRST signal assertion is less than 10µs and depends on the R54-C_{STARTB} delay. C_{STARTB} is a sum of parasitic capacitances at node STARTB (Q1's drain capacitance, Q2 and Q3's gates capacitances). After the R45 / C15 delay (about 100µs as depicted in the right-hand image), the enable pin of U1 falls. U1 stops and discharges its output capacitor through its internal discharge resistor. When VDD_3V3 falls, it discharges C18 through D1 and C11 and D2. The enable pins of U2 and U3 are pulled low, thus stopping these regulators.

Figure 2-4. Shutdown Waveforms

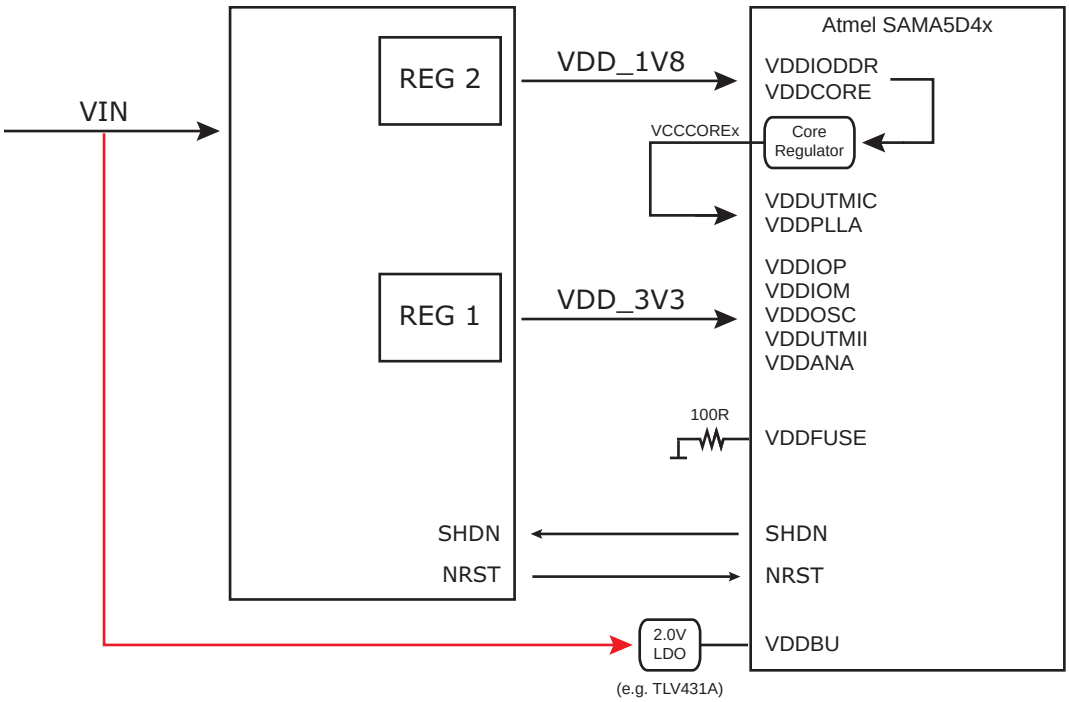


3. Variations from the Reference Schematic

3.1 Applications Without Backup Battery

To start the power supply described in Figure 2-1, the SHDN output of the SAMA5D4 must be set to a high level. The SHDN pin, which is part of the VDDBU power domain of the Atmel device, defaults to a high level when VDDBU is applied for the first time, thus ensuring a safe first start-up of the application. If VDDBU is not built from an always-on source (like a battery), it is convenient to regulate VDDBU voltage from the input power source (VIN) rather than from one output of the power supply. This way, the SHDN pin and, more generally, the Shutdown Controller are properly supplied before the power supply starts and after the shutdown command.

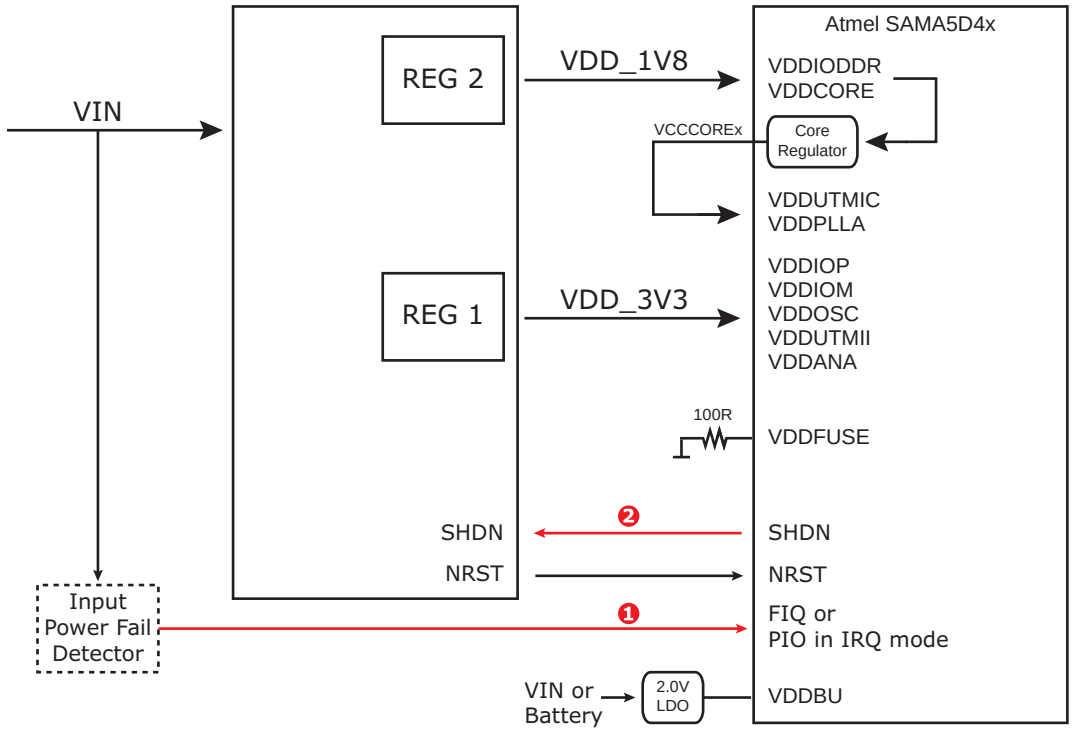
Figure 3-1. Applications Without Backup Battery



3.2 Input Power-Fail Detection

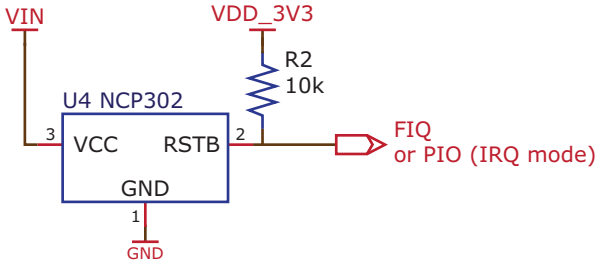
It is possible to add an input power-fail detection circuit to the basic reference schematic depicted in Figure 2-1. The principle, described in Figure 3-2, is to monitor the input voltage VIN and to warn the processor with an interrupt in case of power loss. The Fast Interrupt (FIQ) input or any I/O configured as an interrupt input may be used. Upon this interrupt request, a software power- off sequence is started during which some data storage and/or service shutdown may be performed depending on the remaining ”ON” time. This power-off sequence then ends by setting the bit SHDW in SHDW_CR. The SHDN pin falls down to 0 which turns off the power supply, as described in Section 2.2.2 “Shutdown Description” on page 10.

Figure 3-2. Power Loss Management Principle



To monitor the input voltage VIN, several solutions are possible depending on available resources at system level. (e.g., a system with a voltage reference on-board only requires an additional voltage comparator). Figure 3-3 shows one possible implementation using an integrated voltage monitor circuit.

Figure 3-3. Input Power-Fail Detection Examples



3.3 Discrete Components Selection

The discrete components listed in this application note are given as implementation examples. They are not strong recommendations. The reader may adapt the presented schematics to his specific needs and still keep the basic principles described in the previous sections. As the focus of this application note is the solution cost, only low-cost components are selected. This may lead to “over-sized” components compared to the real application need because they give the best price in this particular case. While cost and ease of procurement are the primary criteria for component selection, other criteria have to be considered to select other types of components:

- Regulators: Devices should feature an enable input and a power-good output as they ease the design of the power sequencing and reset generation circuits.
- NMOS transistors: Low threshold voltage (< 2V) devices are best to ensure safe commutation in all cases (VDDBU is regulated to 2V).
- Diodes: Any general-purpose, small signal device with a low reverse current specification (<20nA at 20V and 25°C) is suitable.

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