ENT-AN1035

Application Notes

One-Step and Two-Step Systems Using Microsemi 1588v2 PHYs

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

In revision 2.0 of this document, formatting was updated.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 One-Step and Two-Step Systems Using Microsemi 1588v2 PHYs

This document illustrates one-step and two-step applications using Microsemi 1588v2 PHYs, highlighting major differences between these methods for ordinary clock and boundary clock systems.

The documents for the following products are available for reference: VSC8492 Dual Channel Universal 10G PHY or 10 GbE PHY with OTN/FEC and IEEE 1588; VSC8494 Quad Channel Universal 10G PHY or 10 GbE PHY with OTN/FEC and IEEE 1588; VSC8488-15 Dual Channel WAN/LAN/Backplane XAUI to SFP+/KR Transceiver; and VSC8487-15 WAN/LAN/Backplane XAUI to SFP+/KR Transceiver.

The primary difference between one-step and two-step 1588 systems using Microsemi PHYs is that the one-step method provides the transmit timestamp in the PTP message on the fly, whereas the two-step method requires an additional follow-up message containing transmit time of the preceding message. Types of 1588 one-step and two-step systems include:

- End-to-end transparent clocks (E2E TC)
- Peer-to-peer transparent clocks (P2P TC)
- Boundary clocks (BC)
- Ordinary clocks (OC)

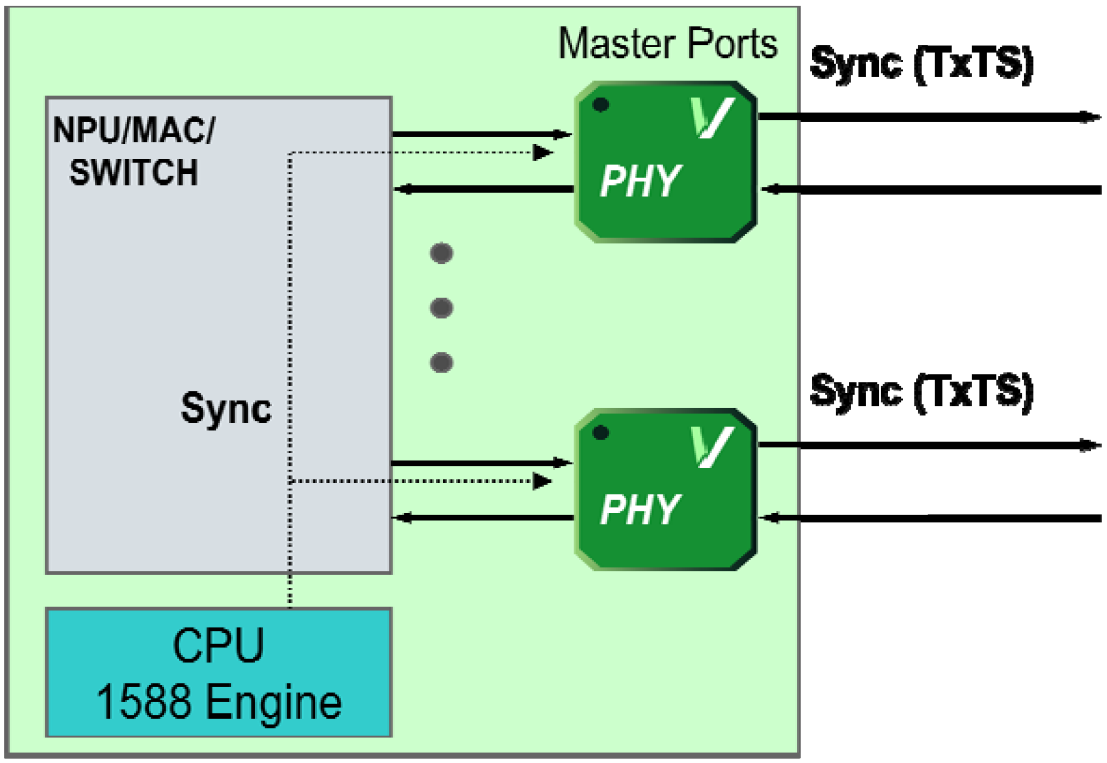
All two-step systems require a 1588 engine to generate follow-up messages.

The one-step solution reduces system cost by not requiring a 1588 engine to generate follow-up messages. However, Microsemi PHYs have the flexibility to provide accurate time stamp correction for both one-step and two-step 1588 solutions.

2.1 One-Step vs. Two-Step OC/BC

The following illustration shows a one-step OC/BC example.

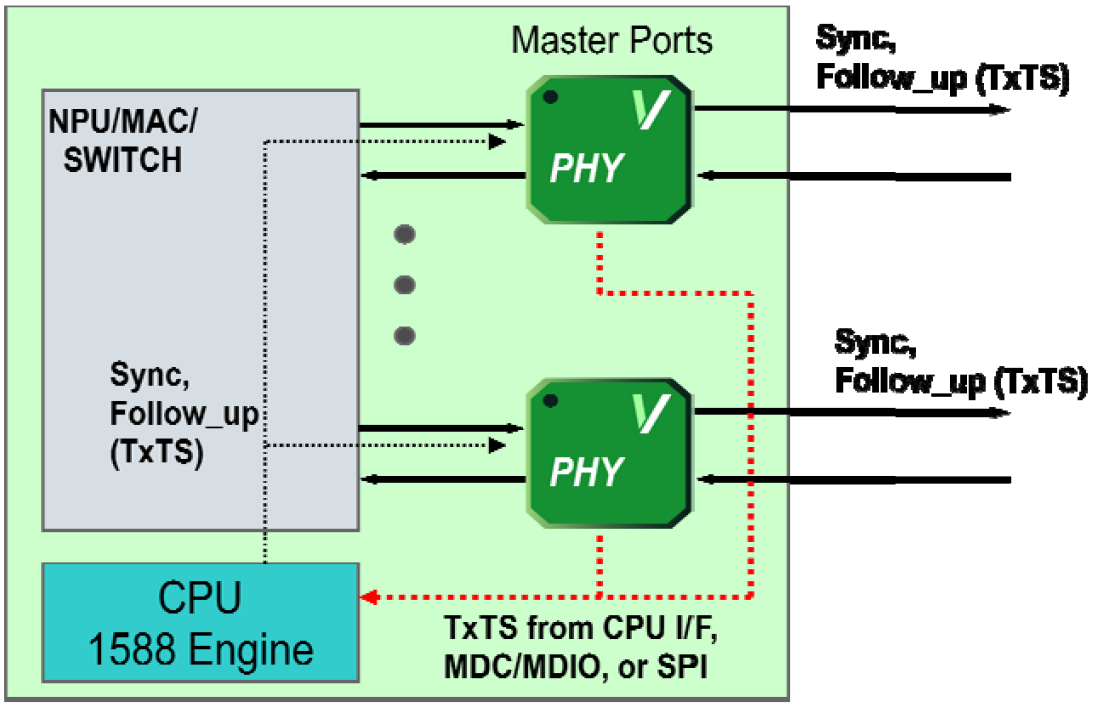
Figure 1 • One-Step OC/BC



The 1588 engine forwards a sync message to all master ports and each PHY overwrites the OriginTime with a transmit time stamp (TxTS).

The following illustrations shows a two-step OC/BC example.

Figure 2 • Two-Step OC/BC



The 1588 engine forwards a sync message to all master ports and each PHY saves the transmit time stamp (TxTS) in a FIFO. The 1588 engine then reads the TxTS and sends a Follow_up message with the TxTS. The transmit time stamps can be read from the FIFO using the SPI, MDIO, or parallel CPU interface. The parallel CPU interface is only available on the VSC8492/VSC8494 (instead of the MDIO).

This illustrates the primary difference between one-step and two-step OC/BC: one-step only forwards the sync message containing the TxTS, whereas two-step systems forward the sync message plus a Follow-up message containing the TxTS.

The SPI, MDIO, or CPU interface can be used to access the time stamp for FIFO for two-step mode.

The time stamp FIFO serial interface block writes (“pushes”) time stamp/fram signature pairs to the external chip interface consisting of three output pins: SI_DO, SI_CLK, and SI_EN_N. The SPI provides higher speed access to time stamps than the MDC/MDIO, and higher bandwidth ultimately allows more slaves in the network.

The following lists MDIO, SPI bandwidth, and max slave estimates:

- SPI (40 MHz) approximately 730K time stamps per second (11.4K max slaves).
- SPI (20 MHz) approximately 365K time stamps per second (5.7K max slaves).
- MDIO (2.5 MHz) approximately 6.2K time stamps per second (96 max slaves).
- MDIO (12.5 MHz) approximately 31K time stamps per second (480 max slaves).
- Assumptions: 32-bit time stamp (ns) and 16-bit frame identifier, MDIO access 64-bit (including 32-bit preamble).
- Sync rate is 64 frames per second.
- 80% utilization is assumed for estimates. Designs need to take into account other devices or slaves loading on the bus bandwidth.

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