AN1975

SCH3227/SCH3226/SCH3224/SCH3222 System BIOS Porting Guide

Author: *Vicky Chen*
Microchip Technology Inc.

INTRODUCTION

This document provides BIOS engineers a quick reference to port System BIOS in support of these SCH322x I/O devices: PARALLEL PORT, SERIAL PORT1, SERIAL PORT2, KEYBOARD, RUNTIME REGISTERS, SERIAL PORT3, SERIAL PORT4, SERIAL PORT5, SERIAL PORT6, Watchdog Timer and the Hardware Monitor Block Initialization. The SCH322x consists of SCH3227, SCH3226, SCH3224 and SCH3222.

References

The following documents should be referenced when using this application note. Please contact your Microchip representative for availability.

- SCH322x Product Brief
- ACPI Specification, Rev. 5.0 (12-06-11)

1.0 Contents

This guide consists of the following chapters:

2.0 DEVICE ID

This chapter describes the Device ID definitions to support for SCH3227/SCH3226/SC3224/SCH3222.

SCH3224 and SCH3222

The Device ID register at Plug & Play Index 0x20 holds 0x7F.

SCH3227 and SCH3226

The Device ID register at Plug&Play Index 0x20 is affected by the STRAP OPTION (STRAPOPT, see Section 2.1) pin.

The STRAPOPT provides bit[1] of this 0x20 register:

- If STRAPOPT=1 then Device ID = 0x7F.
- If STRAPOPT=0 then Device ID = 0x7D.

2.1 STRAPOPT PIN FUNCTIONS

The STRAPOPT connection defines pin functions to support for both SCH3226 and SCH3227 only, and also the contents of the Device ID register at Plug&Play Index 0X20.

- When connected to VTR, the table column STRAPOPT=1 applies.(Note 2-1).

  If the board design sets STRAPOPT=1, then this pinout contains UARTs 5 and 6.
- When connected to VSS, the table column STRAPOPT=0 applies.(Note 2-1).

  If the board design sets STRAPOPT=0, then this pinout does not contain UARTs 5 and 6.

Note 2-1 Please see the Table 3-1, “SCH3227 SUMMARIES BY STRAP OPTION” and the Table 3-2,”SCH3226 SUMMARIES BY STRAP OPTION” in the SCH322x Product Brief for the details.

3.0 OBTAINING THE SCH322X CONFIGURATION BASE ADDRESS

The BIOS uses these configuration ports to initialize the logical devices at Power On Self-Test. The INDEX and DATA ports are only valid when the SCH322x is in Configuration Mode.

The Base Address of the Configuration Access Ports is determined by the Strap Options. See Table 3-1.

Strap options must be added to allow four Configuration Register Base Address options: 0x002E, 0x004E, 0x162E, or 0x164E. At the deasertting edge of PCIRST# or VCC POR the nRTS1/SYSOPT0 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[7:0]= 0x2E
- 1 = Index Base I/O Address bits A[7:0]= 0x4E

At the deasertting edge of PCIRST# or VCC POR the nDTR1/SYSOPT1 pin is latched to determine the configuration base address:

- 0 = Index Base I/O Address bits A[15:8]= 0x16
- 1 = Index Base I/O Address bits A[15:8]= 0x00

The above strap options will allow the Configuration Access Ports (CONFIG PORT, the INDEX PORT, and DATA PORT) to be controlled by the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins and by the Configuration Port Base Address registers at offset 0x26 and 0x27. The configuration base address at power-up is determined by the SYSOPT strap option. The SYSOPT strap option is the latched state of the nRTS1/SYSOPT0 and nDTR1/SYSOPT1 pins at the deasserting edge of PCIRST#. The nRTS1/SYSOPT0 pin determines the lower byte of the Base Address and the nDTR1/SYSOPT1 pin determines the upper byte of the Base Address. The following table summarizes the Base Configuration address selected by the SYSOPT strap option.

TABLE 3-1: SYSOPT Strap Option Configuration Address Select

SYSOPT1	SYSOPT0	Default CONFIG PORT/ INDEX PORT Address	Data Port
1	0	0x002E	INDEX PORT + 1
1	1	0x004E	
0	0	0x162E	
0	1	0x164E	

APPLICATION NOTE: The nRTS1/SYSOPT0 and the nDTR1/SYSOPT1 pins requires external pull-up/pull-down resistors to set the default base I/O address for configuration to 0x002E, 0x004E, 0x162E, or 0x164E.

Note 3-1 An external pull-down resistor is required for the base I/O address to be 0x02E for configuration. An external pull-up resistor is required to move the base I/O address for configuration to 0x04E.

Note 3-2 The configuration port base address can be relocated through CR26 and CR27.

TABLE 3-2: CHIP-LEVEL (GLOBAL) CONFIGURATION REGISTERS

Register	Address	Description
CHIP (GLOBAL) CONTROL REGISTERS		
Configuration Address Byte 0 Default =0x002E (Sysopt0 = 0) =0x004E (Sysopt0 = 1) on VCC POR and PCI RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0 (Note 3-3)
Configuration Address Byte 1 Default =0x16 (Sysopt1 = 0) =0x00 (Sysopt1 = 1) on VCC POR and PCI RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] (Note 3-3)

Note 3-3 To allow the selection of the configuration address to a user-defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (**Note:** Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a PCI Reset or Vcc POR.

Note:	The default configuration address is either 02Eh or 04Eh, as specified by the SYSOPT pin.

4.0 CONFIGURATION REGISTER PROGRAMMING

The SCH322x contains the configuration registers CR02-CR2F and the Logical Devices #3: PARALLEL PORT, #4:SERIAL PORT1, #5:SERIAL PORT2, #7:KEYBOARD, #A:RUNTIME REGISTERS, #B:SERIAL PORT3, #C:SERIAL PORT4, #D:SERIAL PORT5, #E:SERIAL PORT6.

After the SCH322x enters the configuration state, the configuration registers can be programmed by first writing the register index number (0x02 - 0x2F) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or reading the configuration register contents through the DATA PORT Configuration register access remains enabled until the configuration state is explicitly exited.

CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Section 4.1, "Entering the Configuration State".
2. Section 4.2, "Configure the Configuration Registers".
3. Section 4.3, "Exiting the Configuration State".

4.1 Entering the Configuration State

To enter the Configuration State, the system writes the configuration key consists of 0x55 to CONFIG PORT. Once the configuration key is received correctly, the chip enters into the Configuration State.

4.2 Configure the Configuration Registers

The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports. In Configuration mode, the INDEX PORT is located at CONFIG PORT address and the DATA PORT is at IDEX PORT address + 1.

The desired Configuration Registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.
2. Write the address of the desired Configuration Register within the logical device to the INDEX PORT and then write or read the Configuration Register through the DATA PORT.

Note:	If accessing the Global Configuration Registers, step (1) is not required.

4.3 Exiting the Configuration State

To exit the Configuration State, the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

4.4 Example: Configure the Configurations

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;----------------------------.
; ENTER CONFIGURATION STATE  |
;----------------------------'
MOV DX,02Eh         ;SYSOPT = 0
MOV AX,055h
OUT DX,AL
;----------------------------.
; CONFIGURE REGISTER CR26 and|
; LOGICAL DEVICE 3 and CR22 |
;----------------------------'
MOV DX,02Eh
MOV AL,26h
OUT DX,AL           ;Point to CR26
MOV DX,02Fh
IN  AL,DX           ;READ CR26
;
MOV DX,02Eh
MOV AL,07h
OUT DX,AL           ;Point to LD# Config Reg
MOV DX,02Fh
MOV AL,4h
OUT DX,AL           ;Point to Logical Device 4
;
MOV DX,02Eh
MOV AL,22h
OUT DX,AL           ;Point to CR22
MOV DX,02Fh
MOV AL,010h         ;Bit[4] Serial Port 1 Power On
OUT AL,DX           ;Update CR22
;----------------------------.
; EXIT CONFIGURATION STATE    |
;----------------------------'
MOV DX,02EH
MOV AX,AAH
OUT DX,AL
```

4.5 Configuration Registers Summary

The following table summarizes the logical device allocation for the different varieties of SCH322x devices.

TABLE 4-1: SCH322X LOGICAL DEVICE SUMMARY

Logical Device	SCH3222	SCH3224	SCH3226	SCH3227
0	RESERVED	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED	RESERVED
2	RESERVED	RESERVED	RESERVED	RESERVED
3	RESERVED	PARALLEL PORT	RESERVED	PARALLEL PORT
4	SERIAL PORT 1	SERIAL PORT 1	SERIAL PORT 1	SERIAL PORT 1
5	SERIAL PORT 2	SERIAL PORT 2	SERIAL PORT 2	SERIAL PORT 2
6	RESERVED	RESERVED	RESERVED	RESERVED
7	KEYBOARD	KEYBOARD	KEYBOARD	KEYBOARD
8	RESERVED	RESERVED	RESERVED	RESERVED
9	RESERVED	RESERVED	RESERVED	RESERVED
Ah	RUNTIME REGIS-TERS	RUNTIME REGIS-TERS	RUNTIME REGIS-TERS	RUNTIME REGISTERS
Bh	SERIAL PORT 3	RESERVED	SERIAL PORT 3	SERIAL PORT 3
Ch	SERIAL PORT 4	RESERVED	SERIAL PORT 4	SERIAL PORT 4

TABLE 4-1: SCH322X LOGICAL DEVICE SUMMARY (CONTINUED)

Logical Device	SCH3222	SCH3224	SCH3226	SCH3227
Dh	SERIAL PORT 5	SERIAL PORT 5	If STRAPOPT=1 SERIAL PORT [5/6] ELSE reserved	If STRAPOPT=1 SERIAL PORT [5/6] ELSE reserved
Eh	SERIAL PORT 6	SERIAL PORT 6		
Fh	RESERVED	RESERVED	RESERVED	RESERVED

TABLE 4-2: CONFIGURATION REGISTER SUMMARY

Index	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Configuration Register
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x7D-0x7F	0x7D-0x7F	0x7D-0x7F	0x7D-0x7F	Device ID - See Section 2.0, "DEVICE ID"
0x19	R/W	-	0x00	0x00	-	TEST8
0x21	R	Current Revision				Device Rev - hard wired
0x22	R/W	0x00	0x00	0x00	0x00	Power Control
0x23	R/W (PME_STS1)	0x00	0x00	0x00	-	Reserved
0x24	R/W	0x44	0x44	0x44	-	OSC
0x25	R/W	-	0x00	0x00	-	TEST9
0x26	R/W	See Table 3-2	-	-	-	Configuration Port Address Byte 0 (Low Byte)
0x27	R/W	See Table 3-2	-	-	-	Configuration Port Address Byte 1 (High Byte)
0x28	R	-	-	-	-	Reserved
0x29	R/W	-	0x00	0x00	-	TEST
0x2A	R/W	-	0x00	0x00	-	TEST 6
0x2B	R/W	-	0x00	0x00	-	TEST 4
0x2C	R/W	-	0x00	0x00	-	TEST 5
0x2D	R/W	-	0x00	0x00	-	TEST 1
0x2E	R/W	-	0x00	0x00	-	TEST 2
0x2F	R/W	-	0x00	0x00	-	TEST 3
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (PARALLEL PORT) AVAILABLE IN SCH3227, SCH3224 RESERVED IN SCH3226, SCH3222						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	0x04	0x04	DMA Channel Select

TABLE 4-2: CONFIGURATION REGISTER SUMMARY (CONTINUED)

Index	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Configuration Register
0xF0	R/W	0x3C	0x3C	0x3C	-	Parallel Port Mode Register
0xF1	R/W	0x00	0x00	0x00	-	Parallel Port Mode Register 2
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (SERIAL PORT 1)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate (Note 4-1)
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 1 Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (SERIAL PORT 2)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate (Note 4-1)
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 2 Mode Register
0xF1	R/W	0x02	0x02	0x02	-	IR Options Register
0xF2	R/W	0x03	0x03	0x03	-	IR Half Duplex Timeout
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (KEYBOARD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select (Keyboard)
0x72	R/W	0x00	0x00	0x00	0x00	Secondary Interrupt Select (Mouse)
0xF0	R/W	0x00	0x00	0x00	-	KRESET and GateA20 Select
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (RESERVED)						
LOGICAL DEVICE A CONFIGURATION REGISTERS (RUNTIME REGISTERS)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x62	R/W	0x00	0x00	0x00	0x00	Secondary Base I/O Address High Byte
0x63	R/W	0x00	0x00	0x00	0x00	Secondary Base I/O Address Low Byte
0XF0	R/W	-	-	0X00	-	CLOCKI32
0xF1	R/W	0x00	0x00	0x00	0x00	FDC on PP Mode Register
0XF2	PME_STS1	0x04	0x04	0x04	-	Security Key Control Register
LOGICAL DEVICE B CONFIGURATION REGISTERS (SERIAL PORT 3) AVAILABLE IN SCH3227, SCH3226, SCH3222 RESERVED IN SCH3224						

TABLE 4-2: CONFIGURATION REGISTER SUMMARY (CONTINUED)

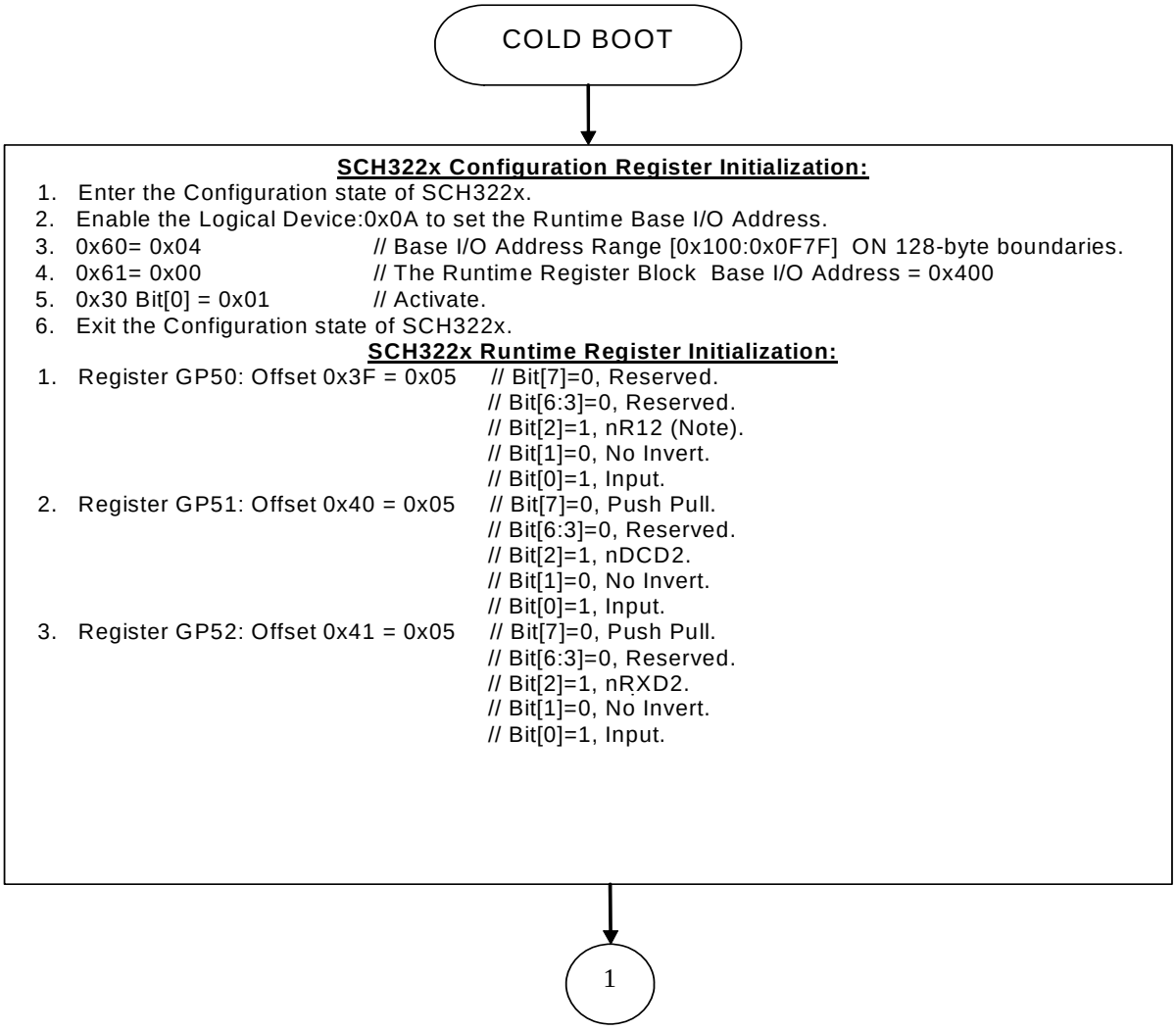
Index	Type	PCI Reset	VCC POR	VTR POR	Soft Reset	Configuration Register
0x30	R/W	0x00	0x00	0x00	0x00	Activate (Note 4-1)
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 3 Mode Register
LOGICAL DEVICE C CONFIGURATION REGISTERS (SERIAL PORT 4) AVAILABLE IN SCH3227, SCH3226, SCH3222 RESERVED IN SCH3224						
0x30	R/W	0x00	0x00	0x00	0x00	Activate (Note 4-1)
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 4 Mode Register
LOGICAL DEVICE D CONFIGURATION REGISTERS (SERIAL PORT 5) AVAILABLE IN SCH3224, SCH3222; IF STRAPOPT=1 SCH3227, SCH3226						
0x30	R/W	0x00	0x00	0x00	0x00	Activate (Note 4-1)
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 5 Mode Register
LOGICAL DEVICE E CONFIGURATION REGISTERS (SERIAL PORT 6) AVAILABLE IN SCH3224, SCH3222; IF STRAPOPT=1 SCH3227, SCH3226						
0x30	R/W	0x00	0x00	0x00	0x00	Activate (Note 4-1)
0x60	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address High Byte
0x61	R/W	0x00	0x00	0x00	0x00	Primary Base I/O Address Low Byte
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 6 Mode Register
LOGICAL DEVICE F CONFIGURATION REGISTERS (RESERVED)						

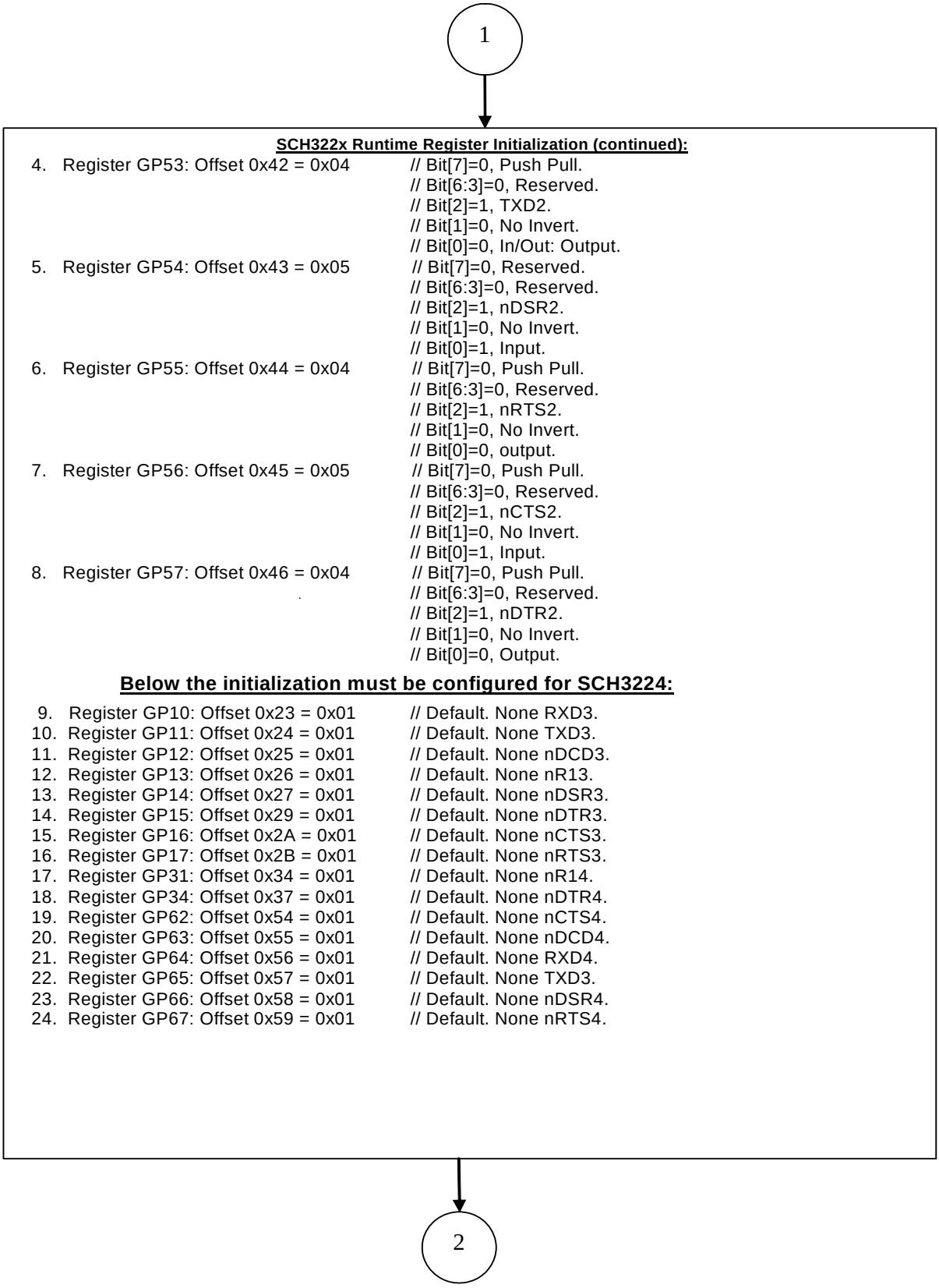
Note 4-1 Serial ports 1 and 2 may be placed in the powerdown mode by clearing the associated activate bit located at CR30 or by clearing the associated power bit located in the Power Control register at CR22. Serial ports 3,4,5,6 (if available) may be placed in the powerdown mode by clearing the associated activate bit located at CR30. When in the powerdown mode, the serial port outputs are tristated. In cases where the serial port is multiplexed as an alternate function, the corresponding output will only be tristated if the serial port is the selected alternate function.

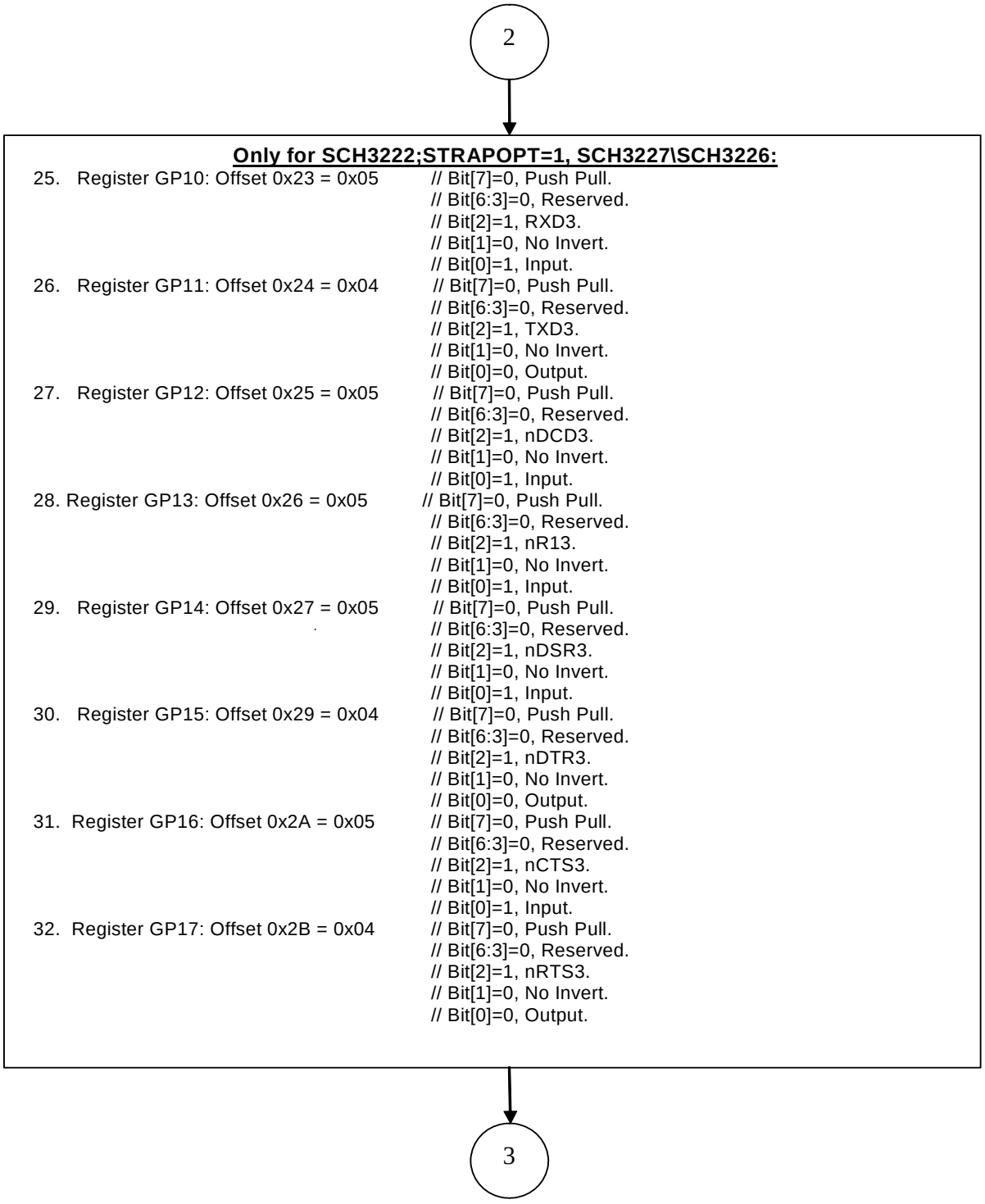
5.0 SUPER I/O INITIALIZATION IN EARLY POWER ON SELF-TEST

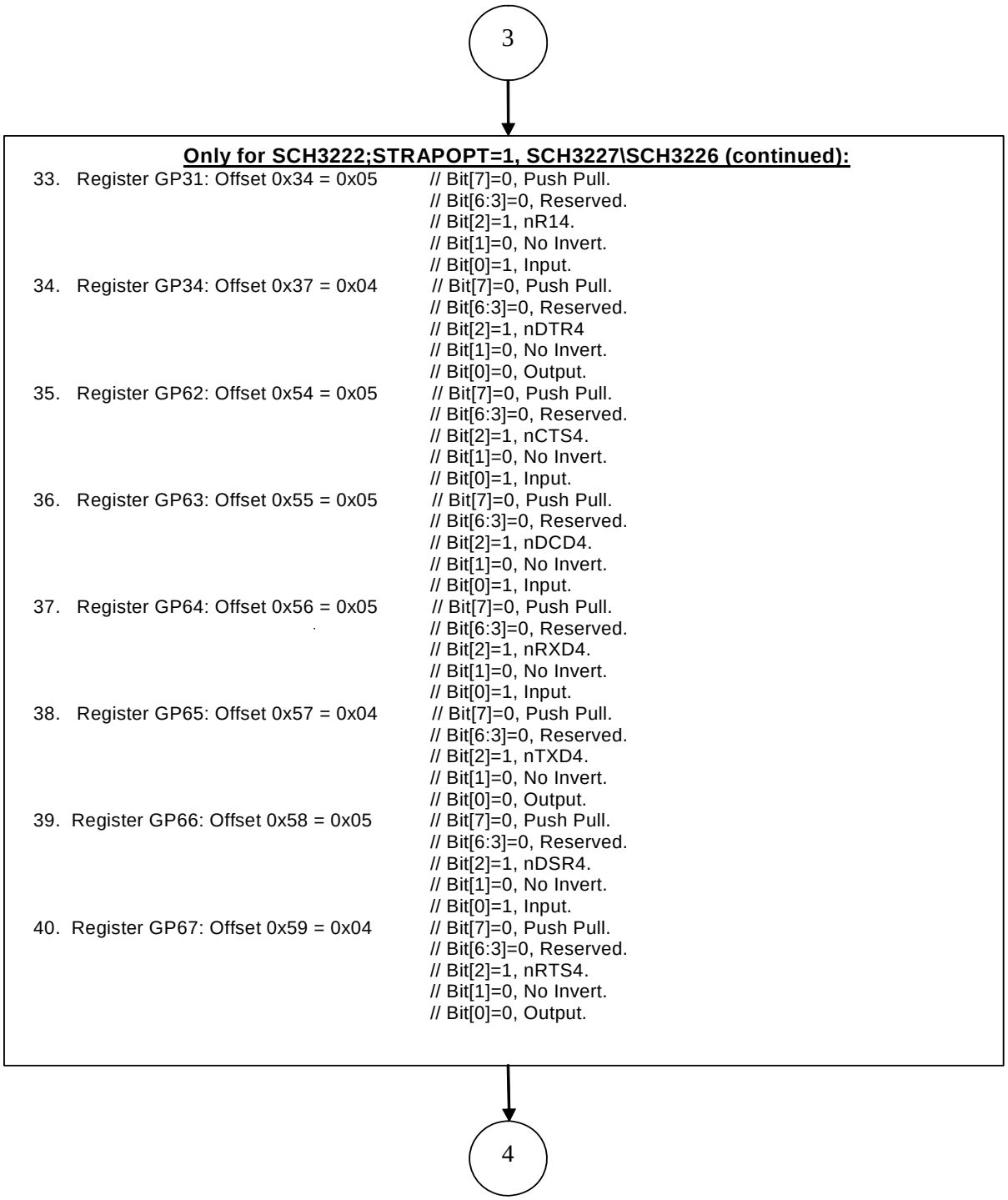
Note: It is very important, for these SCH322x products, that disconnected Logical Devices must not be programmed away from their hardware default configurations. Their Configuration Registers must not be changed, and especially they must not be Activated. Logical Device #0 must never be re-configured or Activated in any SCH322x product, and any Logical Device that is not connected to pins in a specific SCH322x family member (for example, the Parallel Port, or some UARTs) must also not be re-configured or Activated either.

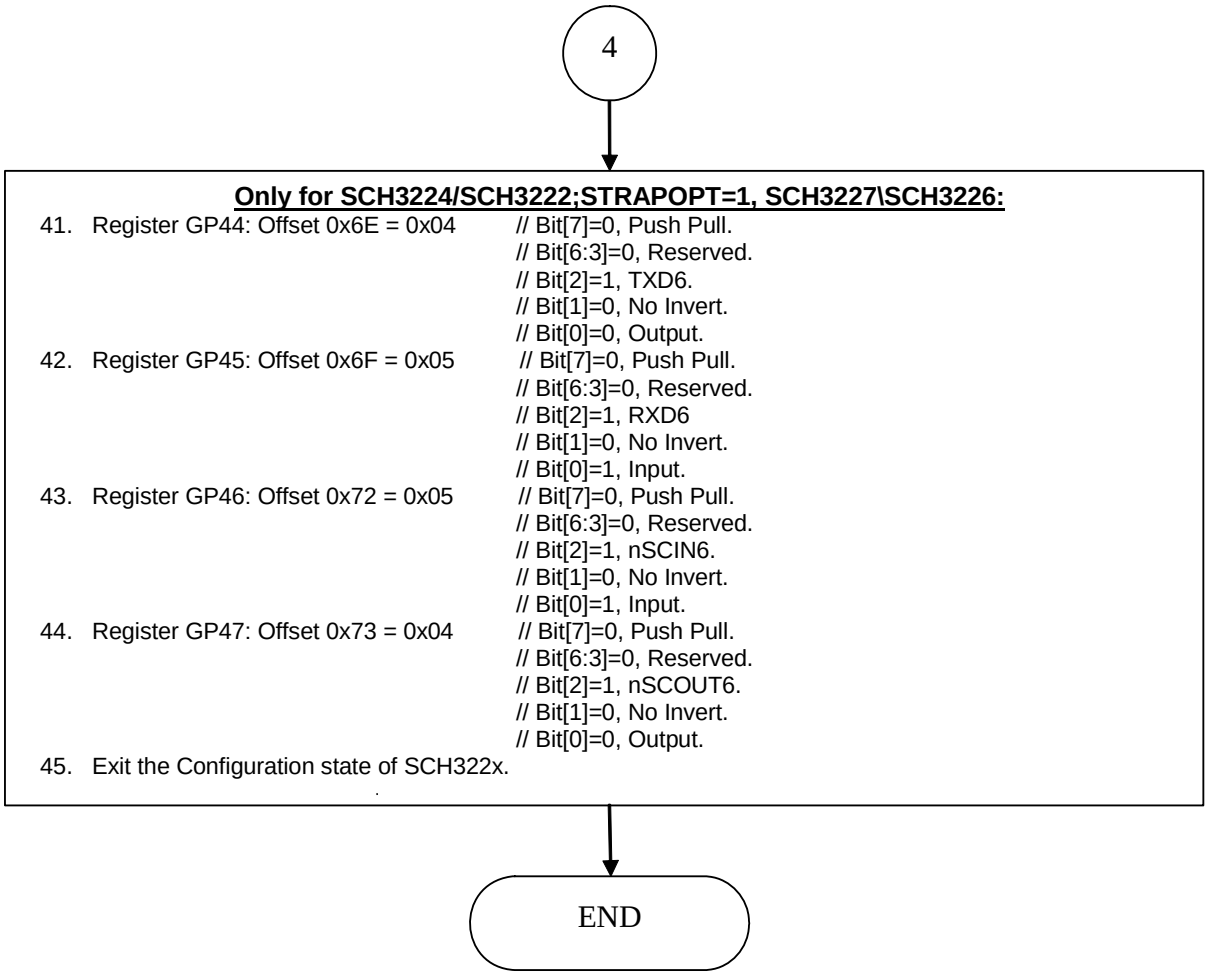
5.1 Runtime Register Block - Logical Device A Chart and Description




1
SCH322x Runtime Register Initialization (continued):
4. Register GP53: Offset 0x42 = 0x04 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, TXD2.
// Bit[1]=0, No Invert.
// Bit[0]=0, In/Out: Output.
5. Register GP54: Offset 0x43 = 0x05 // Bit[7]=0, Reserved.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nDSR2.
// Bit[1]=0, No Invert.
// Bit[0]=1, Input.
6. Register GP55: Offset 0x44 = 0x04 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nRTS2.
// Bit[1]=0, No Invert.
// Bit[0]=0, output.
7. Register GP56: Offset 0x45 = 0x05 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nCTS2.
// Bit[1]=0, No Invert.
// Bit[0]=1, Input.
8. Register GP57: Offset 0x46 = 0x04 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nDTR2.
// Bit[1]=0, No Invert.
// Bit[0]=0, Output.
Below the initialization must be configured for SCH3224:
9. Register GP10: Offset 0x23 = 0x01 // Default. None RXD3.
10. Register GP11: Offset 0x24 = 0x01 // Default. None TXD3.
11. Register GP12: Offset 0x25 = 0x01 // Default. None nDCD3.
12. Register GP13: Offset 0x26 = 0x01 // Default. None nR13.
13. Register GP14: Offset 0x27 = 0x01 // Default. None nDSR3.
14. Register GP15: Offset 0x29 = 0x01 // Default. None nDTR3.
15. Register GP16: Offset 0x2A = 0x01 // Default. None nCTS3.
16. Register GP17: Offset 0x2B = 0x01 // Default. None nRTS3.
17. Register GP31: Offset 0x34 = 0x01 // Default. None nR14.
18. Register GP34: Offset 0x37 = 0x01 // Default. None nDTR4.
19. Register GP62: Offset 0x54 = 0x01 // Default. None nCTS4.
20. Register GP63: Offset 0x55 = 0x01 // Default. None nDCD4.
21. Register GP64: Offset 0x56 = 0x01 // Default. None RXD4.
22. Register GP65: Offset 0x57 = 0x01 // Default. None TXD3.
23. Register GP66: Offset 0x58 = 0x01 // Default. None nDSR4.
24. Register GP67: Offset 0x59 = 0x01 // Default. None nRTS4.
2



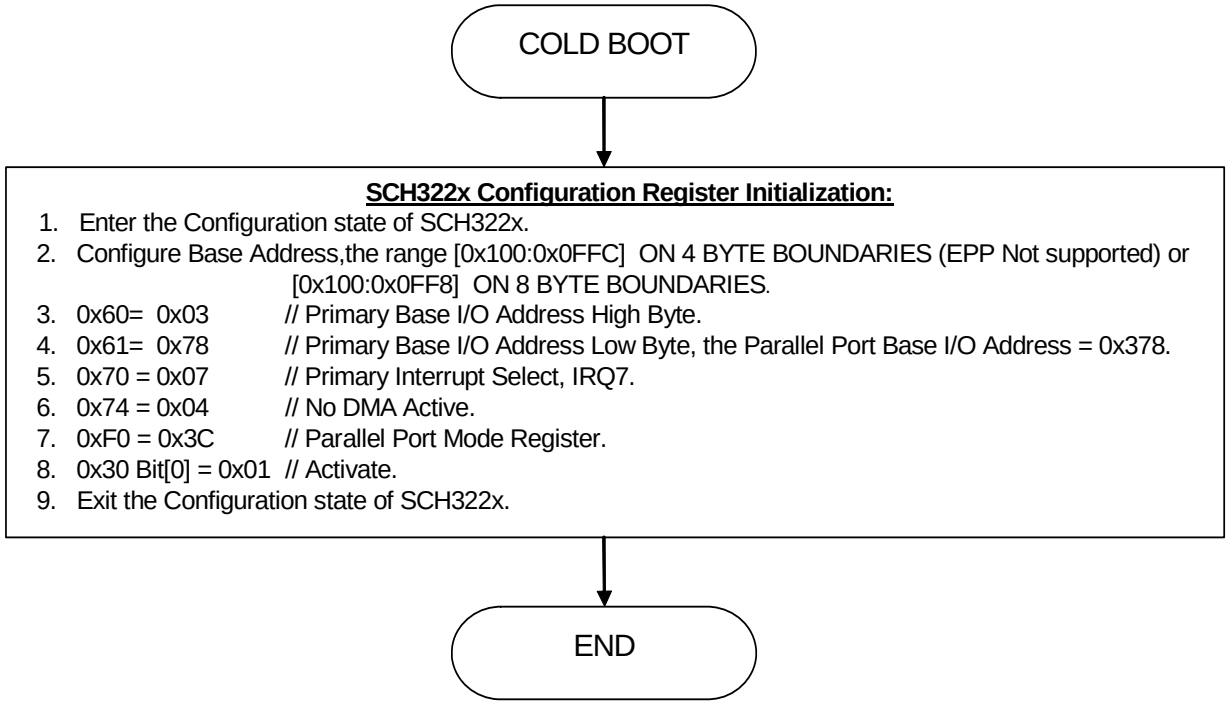

3
Only for SCH3222;STRAPOPT=1, SCH3227\SCH3226 (continued):
33. Register GP31: Offset 0x34 = 0x05 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nR14.
// Bit[1]=0, No Invert.
// Bit[0]=1, Input.
34. Register GP34: Offset 0x37 = 0x04 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nDTR4
// Bit[1]=0, No Invert.
// Bit[0]=0, Output.
35. Register GP62: Offset 0x54 = 0x05 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nCTS4.
// Bit[1]=0, No Invert.
// Bit[0]=1, Input.
36. Register GP63: Offset 0x55 = 0x05 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nDCD4.
// Bit[1]=0, No Invert.
// Bit[0]=1, Input.
37. Register GP64: Offset 0x56 = 0x05 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nRXD4.
// Bit[1]=0, No Invert.
// Bit[0]=1, Input.
38. Register GP65: Offset 0x57 = 0x04 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nTXD4.
// Bit[1]=0, No Invert.
// Bit[0]=0, Output.
39. Register GP66: Offset 0x58 = 0x05 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nDSR4.
// Bit[1]=0, No Invert.
// Bit[0]=1, Input.
40. Register GP67: Offset 0x59 = 0x04 // Bit[7]=0, Push Pull.
// Bit[6:3]=0, Reserved.
// Bit[2]=1, nRTS4.
// Bit[1]=0, No Invert.
// Bit[0]=0, Output.
4



5.2 PARALLEL PORT Initialization

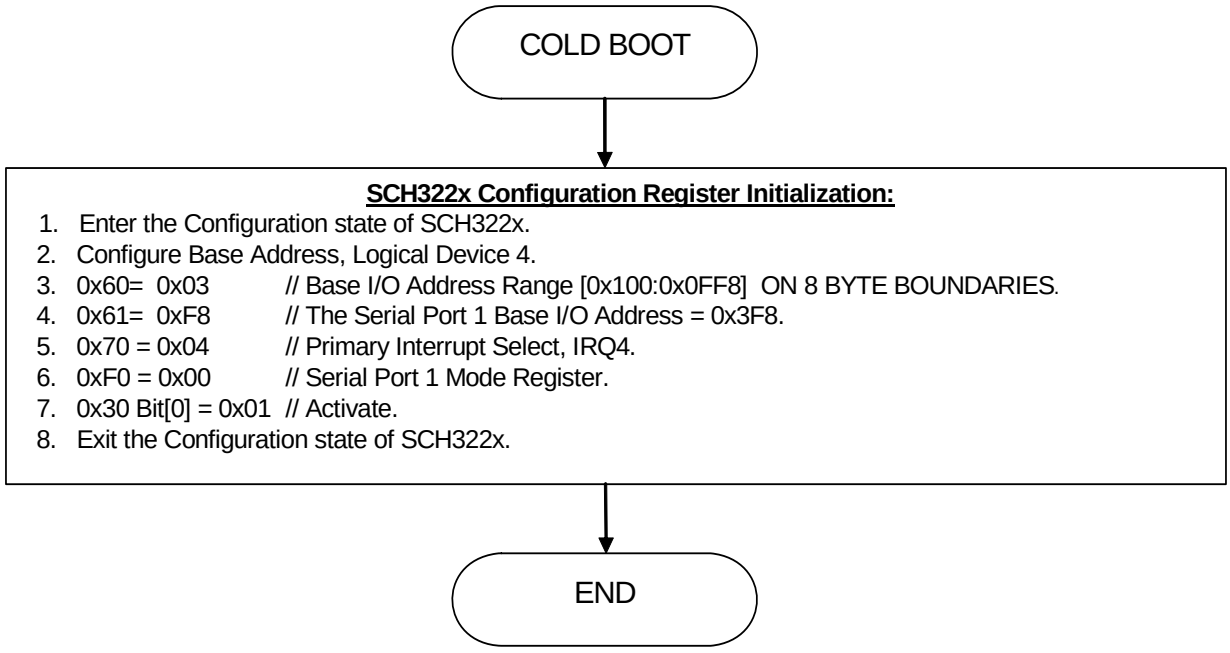
Below, the initialization is available in SCH3227, SCH3224.

5.2.1 PARALLEL PORT - Logical Device 3 Chart and Description



5.3 SERIAL PORT 1 Initialization

5.3.1 SERIAL PORT 1 - - Logical Device 4 Chart and Description



5.4 SERIAL PORT 2 Initialization

5.4.1 SERIAL PORT 2 - - Logical Device 5 Chart and Description

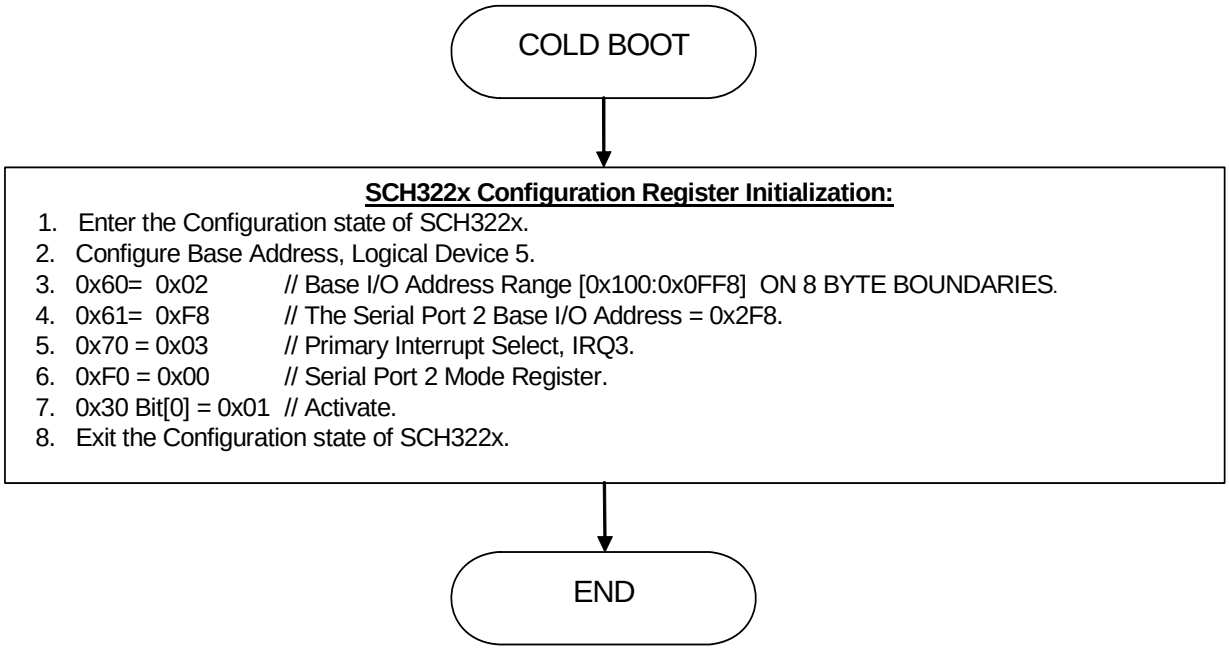
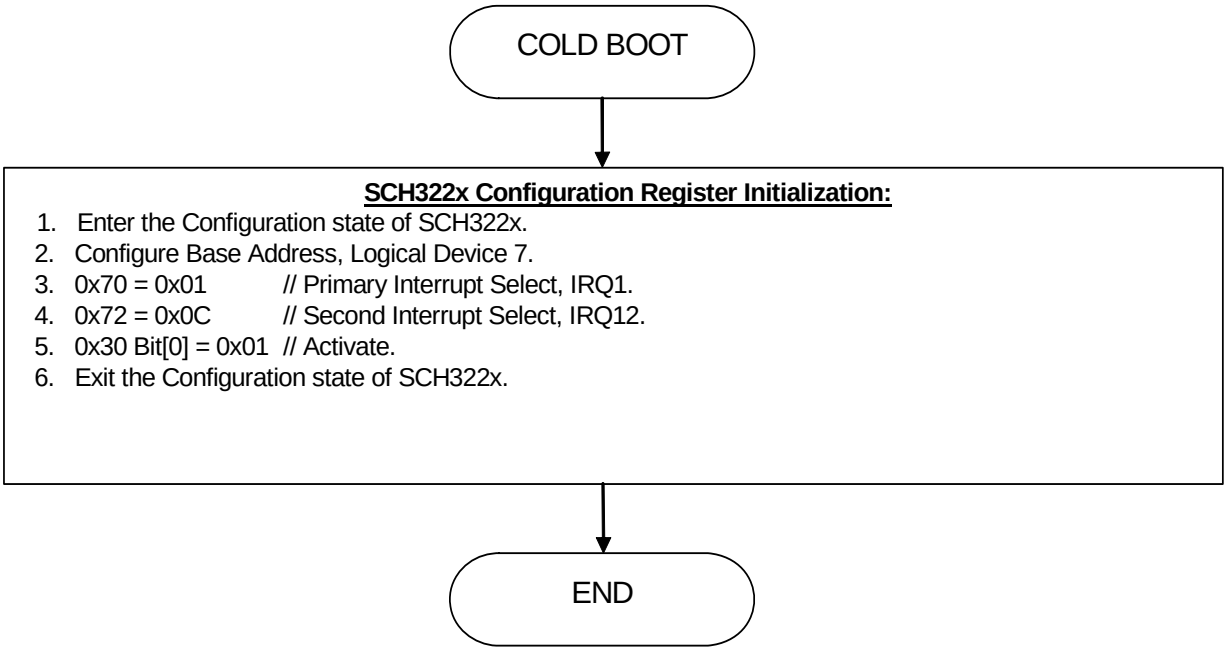


TABLE 5-1: SERIAL PORT 2. LOGICAL DEVICE 5 [LOGICAL DEVICE NUMBER = 0X05]

Name	REG Index	Definition
IR Option Register Default = 0x02 on VCC POR, VTR POR and PCI RESET	0xF1 R/W	Bit[0] Receive Polarity = 0 Active High (Default) = 1 Active Low Bit[1] Transmit Polarity = 0 Active High = 1 Active Low (Default) Bit[2] Duplex Select = 0 Full Duplex (Default) = 1 Half Duplex Bits[5:3] IR Mode = 000 Standard COM Functionality (Default) = 001 IrDA = 010 ASK-IR = 011 Reserved = 1xx Reserved Bit[6] Reserved Set to 0. Bit[7] Reserved, write 0.

5.5 KEYBOARD Initialization

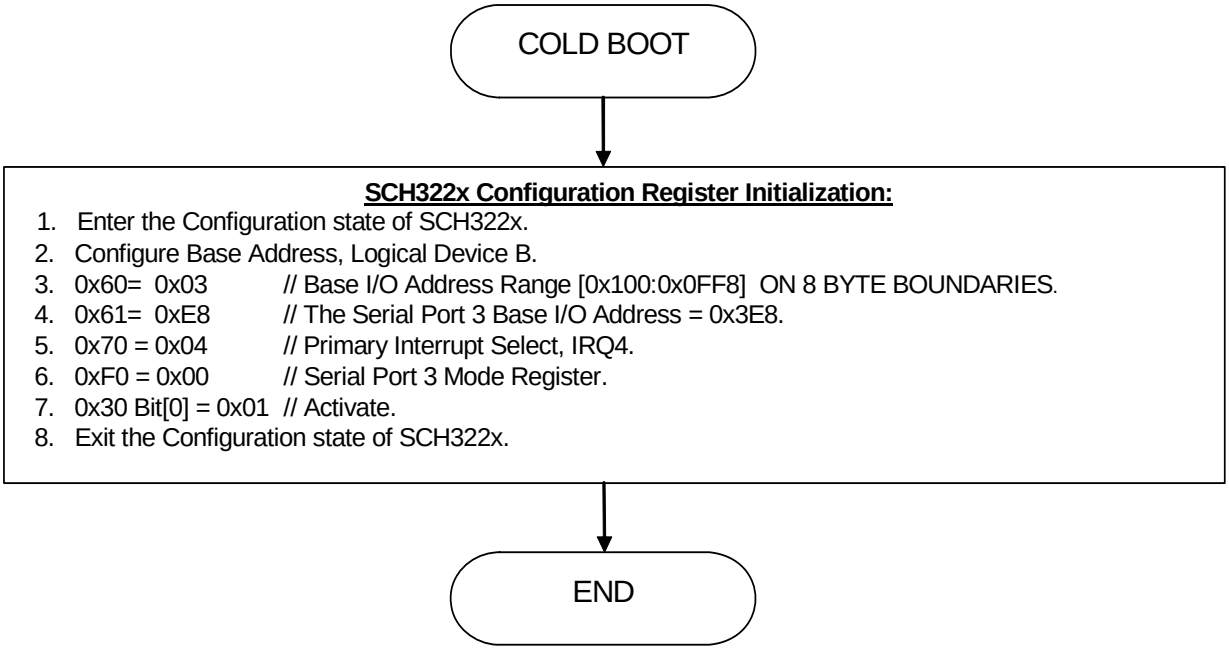
5.5.1 KBD - - Logical Device 7 Chart and Description



5.6 SERIAL PORT 3 Initialization

Below, the initialization is available in SCH3227, SCH3226, SCH3222.

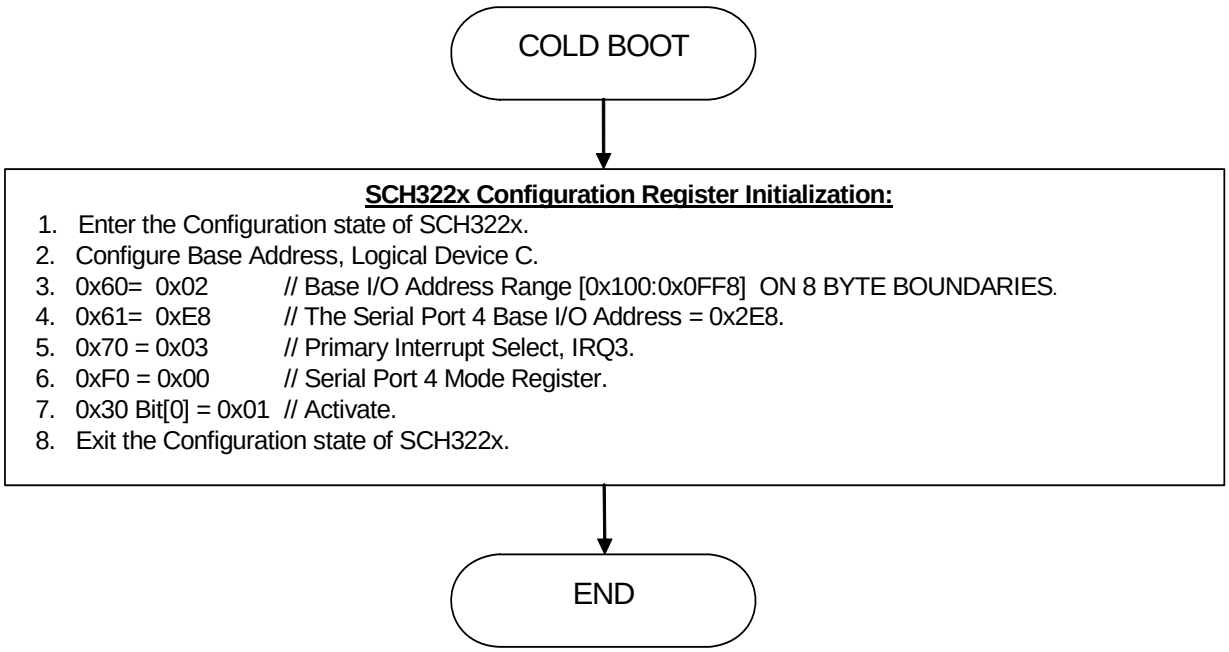
5.6.1 SERIAL PORT 3 - - Logical Device B Chart and Description



5.7 SERIAL PORT 4 Initialization

Below, the initialization is available in SCH3227, SCH3226, SCH3222.

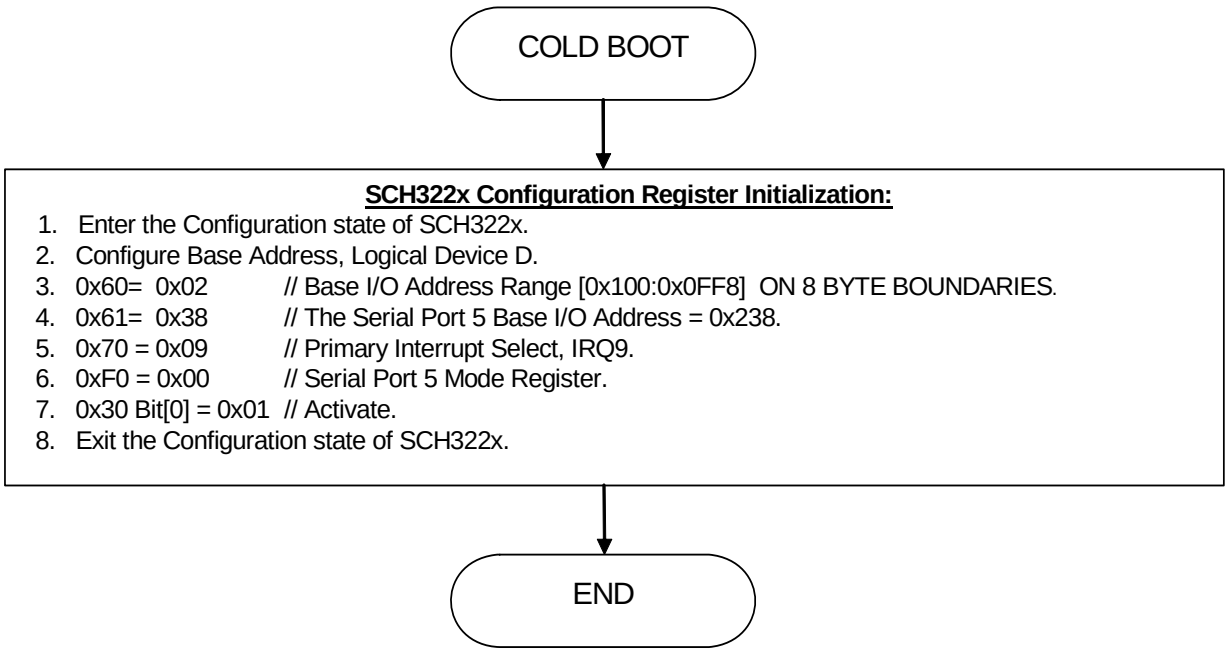
5.7.1 SERIAL PORT 4 - - Logical Device C Chart and Description



5.8 SERIAL PORT 5 Initialization

Below, the initialization is available in SCH3224, SCH3222; if STRAPOPT=1 SCH3227, SCH3226.

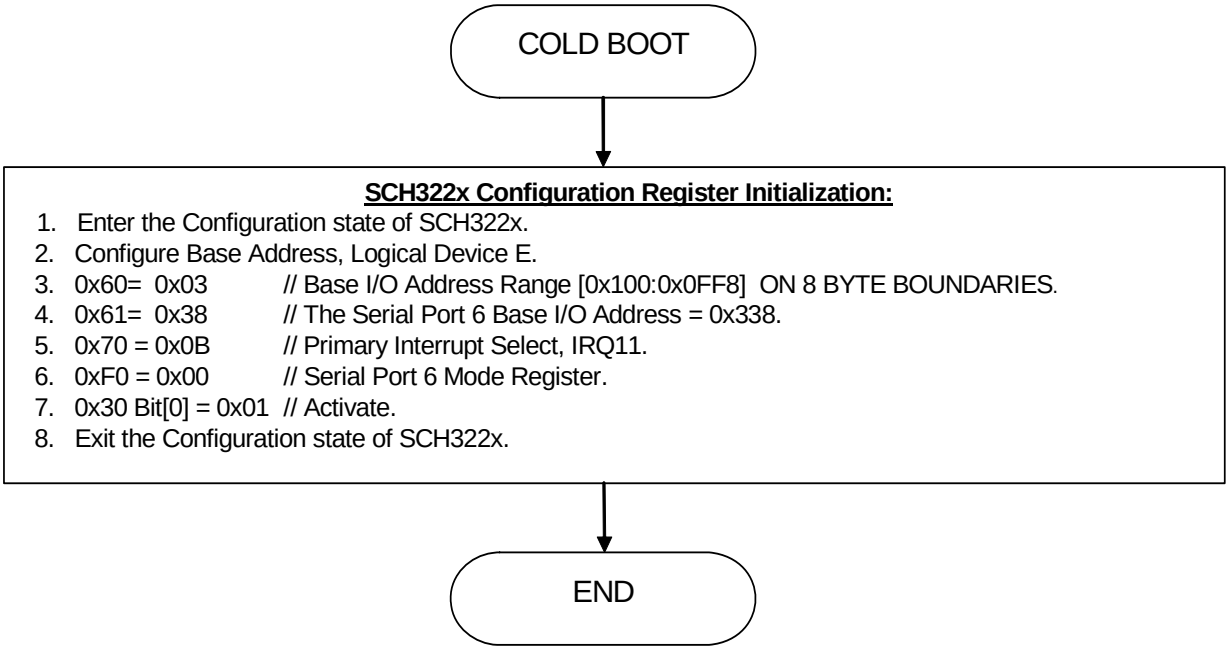
5.8.1 SERIAL PORT 5 - - Logical Device D Chart and Description



5.9 SERIAL PORT 6 Initialization

Below, the initialization is available in SCH3224, SCH3222; if STRAPOPT=1 SCH3227, SCH3226.

5.9.1 SERIAL PORT 6 - - Logical Device E Chart and Description



6.0 WATCHDOG TIMER INITIALIZATION

6.1 The Procedure to Enable the WDT

1. Set the runtime register offset 47h to 0Ch // Bits[3:2] = 11 WDT.
2. Set the runtime register offset 65h to 00h // In minute.
3. Set the runtime register offset 66h for testing minutes, 03h for 3 minutes, 05h for 5 minutes, and 0Ah for 10 minutes; then start counting time.
4. After time-out, please check the runtime register offset 68h bit[0] = 1, write 00h to the runtime register offset 68h then go to step 3 (set the runtime register offset 65h) and start next test.

7.0 Hardware Monitor Block Initialization

This section describes the Hardware Monitoring (HWM) block initializations in BIOS, the HWM block is available in SCH3227, SCH3226, SCH3224.

Note 7-1 The HWM block is not supported for SCH3222.

Note 7-2 For the SCH3222 only:

1. You should not touch Runtime registers 70h and 71h (HWM Index / HWM Data).
2. You should not enable the HWM sources for PME or SMI in the Runtime registers.
3. If you must do any of these above, please consult with Microchip.

7.1 Hardware Monitor Block Base I/O Address Initialization

The SCH3227\SCH3226\SCH3224 HWM block registers access port consists of two runtime registers that occupy two addresses in the Host I/O space: HWM Index Register at offset 70h and HWM Data Register at offset 71h.

To access a HWM register after the Runtime Register Block Base I/O Address has been initialized (Note 7-3), write the HWM Register index address to the HWM Index Register and read or write the HWM register data from the HWM Data Register.

For example: The Runtime Register Block Base I/O Address is 400h, both the HWM Index Register and the HWM Data Register are 470h and 471h.

- Host Reads the Read/Lock/Start register at offset 40h

  Write 40h to the HWM Index Register

  Read the HWM Data Register

- Host Write the Read/Lock/Start register at offset 40h

  Write 40h to the HWM Index Register

  Write 0x01 the HWM Data Register // Set bit[0]: START = 1 to start monitoring.

Note 7-3 See Section 5.1, "Runtime Register Block - Logical Device A Chart and Description," on page 10 to initialize the Runtime Register Block Base I/O Address.

8.0 IRQ SHARING AMONG SERIAL PORTS

Multiple sharing options are available for the SCH322x devices. Sharing an interrupt requires the following:

1. Configure the UART to be the generator to the desired IRQ.
2. Configure other shared UARTs to use No IRQ selected.
3. Set the desired share IRQ bit.

APPLICATION NOTE: If both UARTs are configured to use different IRQs and the share IRQ bit is set, then both of the UART IRQs will assert when either UART generates an interrupt.

Table 8-1 summarizes the various IRQ sharing configurations. In this table, the following nomenclature is used:

- N/A - not applicable
- NS - port not shared
- S12 - UART 1 and UART 2 share an IRQ
- S34 - UART 3 and UART 4 share an IRQ
- S56 - UART 5 and UART 6 share an IRQ
- S1234 - UARTs 1,2,3,4 share the same IRQ
- S1256 - UARTs 1,2,5,6 share the same IRQ
- S3456 - UARTs 3,4,5,6 share the same IRQ
- S123456 - all UARTs share the same IRQ

TABLE 8-1: SCH322X IRQ SHARING SUMMARY

Device	SP1 Mode REG (0xF0) Bit6 All Share Bit Table 8-3 on page 23	SP1 Mode REG (0xF0) Bit7 SP12 Share Bit Table 8-2 on page 22	SP3 Mode REG (0xF0) Bit7 SP34 Share Bit Table 8-3 on page 23	SP5 Mode REG (0xF0) Bit7 SP56 Share Bit Table 8-4 on page 24	SP1	SP2	SP3	SP4	SP5	SP6
SCH3224	0	0	N/A	0	NS	NS	N/A	N/A	NS	NS
	0	1	N/A	0	S12	S12	N/A	N/A	NS	NS
	0	0	N/A	1	NS	NS	N/A	N/A	S56	S56
	0	1	N/A	1	S12	S12	N/A	N/A	S56	S56
	1	0	N/A	0	NS	NS	N/A	N/A	NS	NS
	1	1	N/A	0	S12	S12	N/A	N/A	NS	NS
	1	0	N/A	1	NS	NS	N/A	N/A	S56	S56
	1	1	N/A	1	S1256	S1256	N/A	N/A	S1256	S1256
STRAPOPT=0, SCH3227\SCH3226	0	0	0	N/A	NS	NS	NS	NS	N/A	N/A
	0	1	0	N/A	S12	S12	NS	NS	N/A	N/A
	0	0	1	N/A	NS	NS	S34	S34	N/A	N/A
	0	1	1	N/A	S12	S12	S34	S34	N/A	N/A
	1	0	0	N/A	NS	NS	NS	NS	N/A	N/A
	1	1	0	N/A	S12	S12	NS	NS	N/A	N/A
	1	0	1	N/A	NS	NS	S34	S34	N/A	N/A
	1	1	1	N/A	S1234	S1234	S1234	S1234	N/A	N/A

TABLE 8-1: SCH322X IRQ SHARING SUMMARY (CONTINUED)

Device	SP1 Mode REG (0xF0) Bit6 All Share Bit Table 8-3 on page 23	SP1 Mode REG (0xF0) Bit7 SP12 Share Bit Table 8-2 on page 22	SP3 Mode REG (0xF0) Bit7 SP34 Share Bit Table 8-3 on page 23	SP5 Mode REG (0xF0) Bit7 SP56 Share Bit Table 8-4 on page 24	SP1	SP2	SP3	SP4	SP5	SP6
SCH3222\ STRAPOPT=1, SCH3227\ SCH3226	0	0	0	0	NS	NS	NS	NS	NS	NS
	0	1	0	0	S12	S12	NS	NS	NS	NS
	0	0	1	0	NS	NS	S34	S34	NS	NS
	0	1	1	0	S12	S12	S34	S34	NS	NS
	0	0	0	1	NS	NS	NS	NS	S56	S56
	0	1	0	1	S12	S12	NS	NS	S56	S56
	0	0	1	1	NS	NS	S34	S34	S56	S56
	0	1	1	1	S12	S12	S34	S34	S56	S56
	1	0	0	0	NS	NS	NS	NS	NS	NS
	1	1	0	0	S12	S12	NS	NS	NS	NS
	1	0	1	0	NS	NS	S34	S34	NS	NS
	1	1	1	0	S1234	S1234	S1234	S1234	NS	NS
	1	0	0	1	NS	NS	NS	NS	S56	S56
	1	1	0	1	S1256	S1256	NS	NS	S1256	S1256
	1	0	1	1	NS	NS	S3456	S3456	S3456	S3456
	1	1	1	1	S123456	S123456	S123456	S123456	S123456	S123456

TABLE 8-2: SERIAL PORT 1, LOGICAL DEVICE 4 [LOGICAL DEVICE NUMBER = 0X04

Serial Port 1 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled (default) = 1 High Speed Enabled Bit [3:2] Enhanced Frequency Select = 00 Standard Mode (default) = 01 Select 921K = 10 Select 1.5M = 11 Reserved Bit[5:4] Reserved, set to zero Bit[6] All Share IRQ =0 Use bit 7 to determine sharing =1 Share all serial ports on the SCH322x device. SCH3224 - share 4 serial ports SCH3226 - share 6 serial ports SCH3227 - share 7 serial ports Bit[7]: Share IRQ =0 UARTs 1,2 use different IRQs =1 UARTs 1,2 share a common IRQ (Note 8-1)

Note 8-1 To properly share and IRQ:

1. Configure UART1 (or UART2) to use the desired IRQ.
2. Configure UART2 (or UART1) to use No IRQ selected.
3. Set the share IRQ bit.

Note:	If both UARTs are configured to use different IRQs and the share IRQ bit is set, then both of the UART IRQs will assert when either UART generates an interrupt.

TABLE 8-3: SERIAL PORT 3, LOGICAL DEVICE B [LOGICAL DEVICE NUMBER = 0X0B

Name	REG Index	Definition
Serial Port 3 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET SCH3224 device.	0xF0 R/W	SCH3224 Device Bit[7:0] SMSC Test Bit Must be written with zero for proper operation.
Serial Port 3 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET SCH3227, SCH3226 and SCH3222 devices.	0xF0 R/W	SCH3227, SCH3226 and SCH3222 devices Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled (default) = 1 High Speed Enabled Bit [3:2] Enhanced Frequency Select = 00 Standard Mode (default) = 01 Select 921K = 10 Select 1.5M = 11 Reserved Bit[5:4] Reserved, set to zero Bit[6] SMSC Test Bit Must be written with zero for proper operation. Bit[7]: Share IRQ =0 UARTs 3,4 use different IRQs =1 UARTs 3,4 share a common IRQ (Note 8-1)

TABLE 8-4: SERIAL PORT 5, LOGICAL DEVICE D [LOGICAL DEVICE NUMBER = 0X0D]

Name	REG Index	Definition
Serial Port 5 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET SCH3224 device.	0xF0 R/W	SCH3224 Device Bit[7:0] SMSC Test Bit Must be written with zero for proper operation.
Serial Port 5 Mode Register Default = 0x00 on VCC POR, VTR POR and PCI RESET SCH3227, SCH3226 and SCH3222 devices	0xF0 R/W	SCH3227, SCH3226 and SCH3222 devices Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled (default) = 1 High Speed Enabled Bit [3:2] Enhanced Frequency Select = 00 Standard Mode (default) = 01 Select 921K = 10 Select 1.5M = 11 Reserved Bit[5:4] Reserved, set to zero Bit[6] SMSC Test Bit Must be written with zero for proper operation. Bit[7]: Share IRQ =0 UARTs 5,6 use different IRQs =1 UARTs 5,6 share a common IRQ (Note 8-1)

TABLE 8-5: ASL SAMPLE CODES - BOTH COM1 AND COM2 ARE SHARING IRQ4

	I/O Port	Serial Port Mode Register : 0xF0	IRQ FORMAT
COM1	03F8h	0xC0	0x19
COM2	02F8h	0	0x19

8.1 The Serial Port IRQ Format Definition in ASL Code

The following is the IRQ Format ID.

```
IRQ(s): Small Item Name 0x04 = 0x19
Bit[4] = 1          // Interrupt is sharable, _SHR
Bit[3] = 1          // Low true level sensitive, _LL
Bit[0] = 1          // High true edge sensitive, _HE
```

This IRQ Format ID depends on the ACPI Specification, Rev.5.0, Table 6-163, “IRQ Descriptor Definition” Byte 3: IRQ Information.

```
// COM1 _CRS
Method(_CRS)
Name(BUF1, Buffer() {
        0x47,       // I/O Port Descriptor
        0x01,       // 16 bit decode
        0xF8,       // I/O Port Range Minimum Base Low
        0x03,       // I/O Port Range Minimum Base High
        0xF8,       // I/O Port Range Minimum Base Low
        0x03,       // I/O Port Range Minimum Base High
        0x00,       // Base Alignment
        0x08,       // Length of contiguous I/OPorts
        0x23,       // IRQ Descriptor
        0x10,       // IRQ Mask Lo = bit[4]
        0x00,
        0x19,       // I/OFormat
        0x79,       // End tag
        0x00,
} )
Return(BUF1)
}     // End of COM1 _CRS

// COM1 _PRS
Method(_PRS, Buffer() {
        0x30,       // Start Dependent Function
        0x47,       // I/OPort Descriptor
        0x01,       // 16 bit decode
        0xF8,       // I/OPort Range Minimum Base Low
        0x03,       // I/OPort Range Minimum Base High
        0xF8,       // I/OPort Range Minimum Base Low
        0x03,       // I/OPort Range Minimum Base High
        0x00,       // Base Alignment
        0x38,       // Length of contiguous I/OPorts
        0x23,       // IRQ Descriptor
        0x10,       // IRQ Mask Lo = bit[4]
        0x00,
        0x19,       // I/OFormat
        0x79,       // End tag
        0x00,
} )                 // End of COM1 _PRS

// COM2 _CRS
Method(_CRS)
Name(BUF1, Buffer() {
        0x47,       // I/OPort Descriptor
        0x01,       // 16 bit decode
        0xF8,       // I/OPort Range Minimum Base Low
        0x02,       // I/OPort Range Minimum Base High
        0xF8,       // I/OPort Range Minimum Base Low
        0x02,       // I/OPort Range Minimum Base High
        0x00,       // Base Alignment
        0x08,       // Length of contiguous I/OPorts
        0x23,       // IRQ Descriptor
        0x10,       // IRQ Mask Lo = bit[4]
        0x00,
        0x19,       // I/OFormat
        0x79,       // End tag
        0x00,
} )
```

```
Return(BUF1)
}       // End of COM2 _CRS

// COM2 _PRS
Method(_PRS, Buffer() {
        0x30,       // Start Dependent Function
        0x47,       // I/OPort Descriptor
        0x01,       // 16 bit decode
        0xF8,       // I/OPort Range Minimum Base Low
        0x02,       // I/OPort Range Minimum Base High
        0xF8,       // I/OPort Range Minimum Base Low
        0x02,       // I/OPort Range Minimum Base High
        0x00,       // Base Alignment
        0x38,       // Length of contiguous I/OPorts
        0x23,       // IRQ Descriptor
        0x10,       // IRQ Mask Lo = bit[4]
        0x00,
        0x19,       // I/OFormat
        0x79,       // End tag
        0x00,
}       // End of COM2 _PRS
```


9.0 Intel LPC Interface Bridge Register Initialization

This section provides the initialization of the Intel LPC Interface Bridge registers (D31:F0) to support SCH322x SIO devices in cold booting.

1. LPC_I/O_DEC-I/O Decode Ranges Register 80h - 81h = 0010h

- FDD Decode Range Bit[12] 0h // 3F0h-3F5h, 3F7h (Primary)
- LPT Decode Range Bit[9:8] = 00h // 378h-37Fh and 778h-77Fh
- COMB Decode Range Bit[6:4] = 001h // 2F8h-2FFh (COM2)
- COMA Decode Range Bit[2:0] = 000h // 3F8h-3FFh (COM1)

2. LPC_EN-LPC I/F Enables Register 82h - 83h = 3F0Fh

- CNF2_LPC_EN Bit[13] = 1// Enables the decoding of the I/O locations 4Eh and 4Fh to the LPC interface.
- CNF1_LPC_EN Bit[12] = 1// Enables the decoding of the I/O locations 2Eh and 2Fh to the LPC interface.
- MC_LPC_EN Bit[11] = 1// Enables the decoding of the I/O locations 62h and 66h to the LPC interface.
- KBC_LPC_EN Bit[10] = 1// Enables the decoding of the I/O locations 60h and 64h to the LPC interface.
- GAMEH_LPC_EN Bit[9] = 1 // Enables the decoding of the I/O locations 208 to 20Fh to the LPC interface.
- GAMEL_LPC_EN Bit[8] = 1 // Enables the decoding of the I/O locations 200 to 207h to the LPC interface.
- FDD_LPC_EN Bit[3] = 0 // Disables the decoding of the FDD range to the LPC interface.
- LPT_LPC_EN Bit[2] = 1 // Enables the decoding of the LPC range to the LPC interface.
- COMB_LPC_EN Bit[1] = 1 // Enables the decoding of the COMB range to the LPC interface.
- COMA_LPC_EN Bit[0] = 1 // Enables the decoding of the COMA range to the LPC interface.

3. GEN1_DEC - LPC I/F Generic Decode Range 1 Register 84h - 87h = 007C0401h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 7Ch
- Generic I/O Decode Range 1 Base Address (GEN1_BASE) Bits[15:2] = 040h
- Generic Decode Range 1 Enable (GEN1_EN) Bit[0] = 1 // Enable the GEN1 I/O range to be forwarded to the LPC I/F.

4. GEN2_DEC - LPC I/F Generic Decode Range 2 Register 88h - 8Bh = 000C0501h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 0Ch
- Generic I/O Decode Range 2 Base Address (GEN2_BASE) Bits[15:2] = 050h
- Generic Decode Range 2 Enable (GEN2_EN) Bit[0] = 1 // Access to the GEN2 I/O range is forwarded to the LPC I/F.

5. GEN3_DEC - LPC I/F Generic Decode Range 3 Register 8C - 8Fh = 007C0151h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 7Ch
- Generic I/O Decode Range 3 Base Address (GEN3_BASE) Bits[15:2] = 015h
- Generic Decode Range 3 Enable (GEN3_EN) Bit[0] = 1// Access to the GEN3 I/O range is forwarded to the LPC I/F.

6. GEN4_DEC - LPC I/F Generic Decode Range 4 Register 90h - 93h = 000C06A1h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 0Ch
- Generic I/O Decode Range 4 Base Address (GEN4_BASE) Bits[15:2] = 06Ah
- Generic Decode Range 4 Enable (GEN4_EN) Bit[0] = 1 // Access to the GEN4 I/O range is forwarded to the LPC I/F.

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001975A (06-25-15)	Document Release	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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China - Zhuhai
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India - Bangalore
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India - Pune
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Japan - Osaka
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Japan - Tokyo
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Korea - Daegu
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Fax: 82-53-744-4302

Korea - Seoul
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Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
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Malaysia - Penang
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Philippines - Manila
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Taiwan - Kaohsiung
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Fax: 34-91-708-08-91

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Fax: 44-118-921-5820

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