AN 18.3

Migrating from the LAN9210/LAN9211 to the LAN9220/LAN9221

1 Objective

The purpose of this application note is to assist SMSC customers with existing LAN9210/LAN9211 designs when upgrading to the new LAN9220/LAN9221 devices. The LAN9220/LAN9221 are drop-in replacements for the LAN9210/LAN9211 and existing designs will require little modifications. Additionally, the LAN9220/LAN9221 provide variable I/O pads that accommodate a wide range of I/O signalling without the use of voltage level shifters. This application note addresses all the differences between the LAN9210/LAN9211 and the LAN9220/LAN9221 devices, making this transition as easy as possible.

1.1 References

- LAN9220/LAN9221 Datasheet
- LAN9210/LAN9211 Datasheet
- Reference Design for the LAN9220/LAN9221
- Reference Design for the LAN9210/LAN9211

1.2 Overview of Changes Required

Table 1.1 summarizes the changes needed to migrate from the LAN9210/LAN9211 to the LAN9220/LAN9221.

Table 1.1 Summary of Changes Required

CHANGE REQUIRED	COMMENTS	REFERENCES
Bus Timing & Output Buffer De-rated	Needed to support variable IO voltages < 3.0V.	Refer to section Section 2.1.4
Internal PU/PD resistors augmented & stronger external PU/PD resistors	Needed to support variable IO voltages < 3.0V.	Refer to section Section 2.1.4
Upgrade drivers	Recognize new device ID	Refer to Table 4.1

2 Hardware Changes

2.1 Pin Changes

2.1.1 Signal Name Changes

The following signal names have changed from the LAN9210/LAN9211: (see Table 2.1 and Figure 2.1)

Table 2.1 Signal Name Changes

PIN	LAN9210/LAN9211	LAN9220/LAN9221
46, 49, 51	VDD_A33	VDD33A
53	VDD_A18	VDD18A
18, 24, 30, 56	VDD_IO	VDDVARIO
1	VDD_IO	VDD33REG
2, 37	VDD_CORE	VDD18CORE
14	NC	TEST

2.1.2 Pin Function Changes

The LAN9220/LAN9221 incorporates variable voltage IO pads that are capable of operation at:

- 1.8V +/-10% (1.62V - 1.98V)
- 2.5V +/-10% (2.25V - 2.75V)
- 3.3V +/- 300mV (3.00V - 3.60V)

The VDDVARIO pins (18, 24, 30 and 56) of the LAN9220/LAN9221 must be supplied with the appropriate IO voltage. If the LAN9220/LAN9221 is being used in an existing LAN9210/LAN9211 design, the device will operate properly with no modifications.

Pin 1 has been changed from VDD_IO to VDD33REG. This pin is now the +3.3V power supply for the internal +1.8V regulator. It must be connected to +3.3V +/-300mV.

Pin 14 has been changed from NC (no connect) to TEST on the LAN9220/LAN9221. This pin must be pulled low or tied to ground at VDDVARIO < 3.0V. It can be left unconnected in 3.3V applications.

Caution: In the case of a +1.8V I/O application, the VDDVARIO pins cannot be supplied from the VDD18CORE regulator of the LAN9220/LAN9221. The VDDVARIO pins must be supplied from an on-board, external +1.8V regulator.

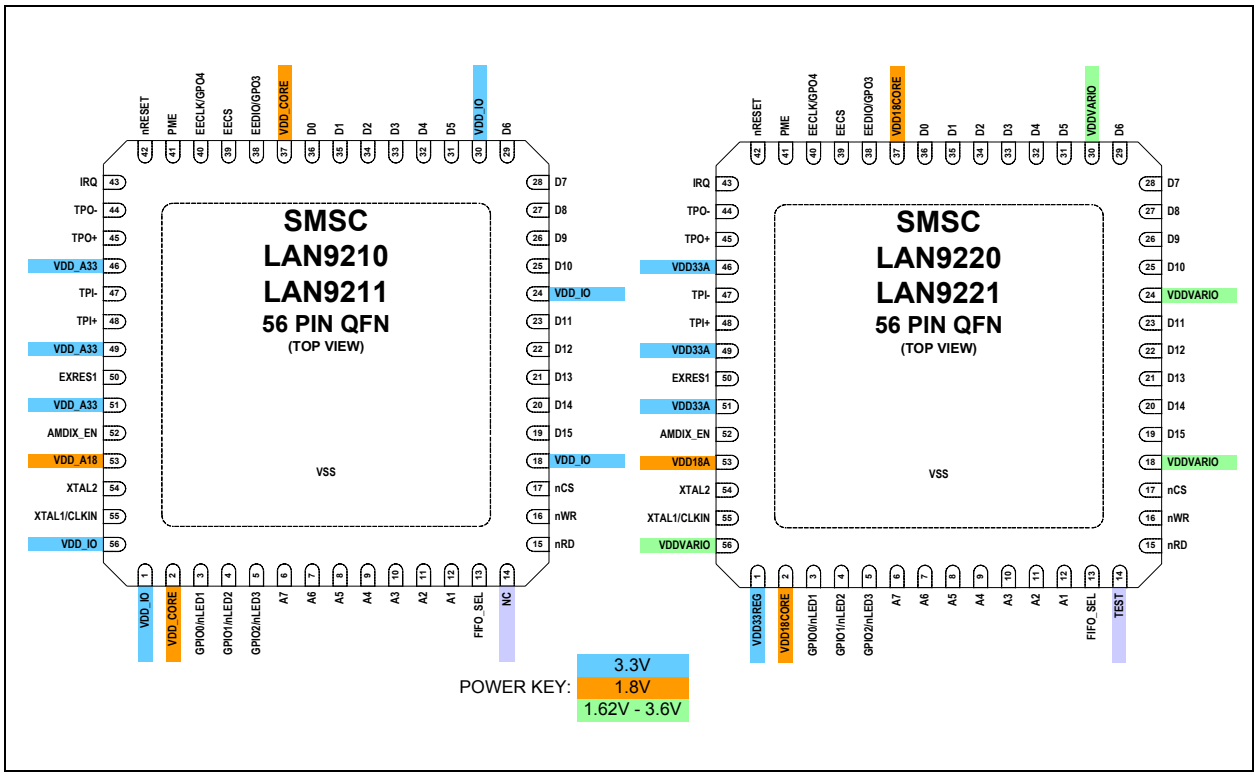

Figure 2.1 Pin Changes

2.1.3 Operating Voltage Requirements

The LAN9220/LAN9221 operating voltage requirements for both VDD33A and VDD33REG have been tightened from +3.3V +/-10% (2.97V - 3.63V) to +3.3 +/-300mV (3.00V - 3.60V).

2.1.4 Variable I/O Pads

If you wish to take advantage of the variable IO capablility, there are some changes you should be aware of.

- Bus timing is maintained regardless of VDDVARIO, except that at VDDVARIO = 3.3V or 2.5V, the maximum t_{doff} is 7ns and at VDDVARIO = 1.8V, the maximum t_{doff} is 9ns.
- The specified load capacitance is reduced from 25pF to 10pF at VDDVARIO = 1.8V and 2.5V. For higher capacitance the bus timing must be de-rated.
- Maximum output current is de-rated at reduced VDDVARIO (see Table 2.2).

Table 2.2 IO Buffer Current De-rating

IO BUFFER	3.3V	2.5V	1.8V
VO12	12mA	9mA	4mA
VOD12	12mA	9mA	4mA
VO8	8mA	6mA	3mA
VOD8	8mA	6mA	3mA

- Internal PU/PD resistors must be augmented with external resistors at VDDVARIO < 3.0V, including default selections (see Table 2.3).
- Stronger external PU/PDs are recommended at VDDVARIO < 3.0V, 10K resistors are still acceptable for 3.3V applications (see Table 2.3).
- When an EEPROM is used, it must be compatible with the selected VDDVARIO voltage.

Table 2.3 External Pull-Up/Pull-Down Resistor Values

I/O VOLTAGE	PULL-UP/PULL-DOWN RESISTOR VALUE (OHMS)
3.3V +/- 300mV	10K
2.5V +/- 10%	7.5K
1.8V +/- 10%	4.7K

3 Register Changes

3.1 SCSR Register Changes

3.1.1 ID_REV Register (offset: 50h)

- For the LAN9220 - Bit 31:16 changed to 9220h.
- For the LAN9221 - Bit 31:16 changed to 9221h.

4 Driver Support

Table 4.1 below shows the version of drivers needed to support the LAN9220/LAN9221.

Table 4.1 Driver Support

DRIVER	REVISION
WinCE 5.0 - XScale (PXA270)	1.3 or later
Linux - XScale (PXA270)	1.56 or later
VXWorks 5.5	2.08 or later

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