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DOCUMENT DESCRIPTION

Schematic Checklist for the LAN9420, 128-pin VTQFP Package

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Schematic Checklist for LAN9420

Information Particular for the 128-pin VTQFP Package

LAN9420 VTQFP Phy Interface:

1. TPO+ (pin 101), this pin is the transmit twisted pair output positive connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

2. TPO- (pin 100), this pin is the transmit twisted pair output negative connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. TPI+ (pin 106), this pin is the receive twisted pair input positive connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

5. TPI- (pin 104), this pin is the receive twisted pair input negative connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

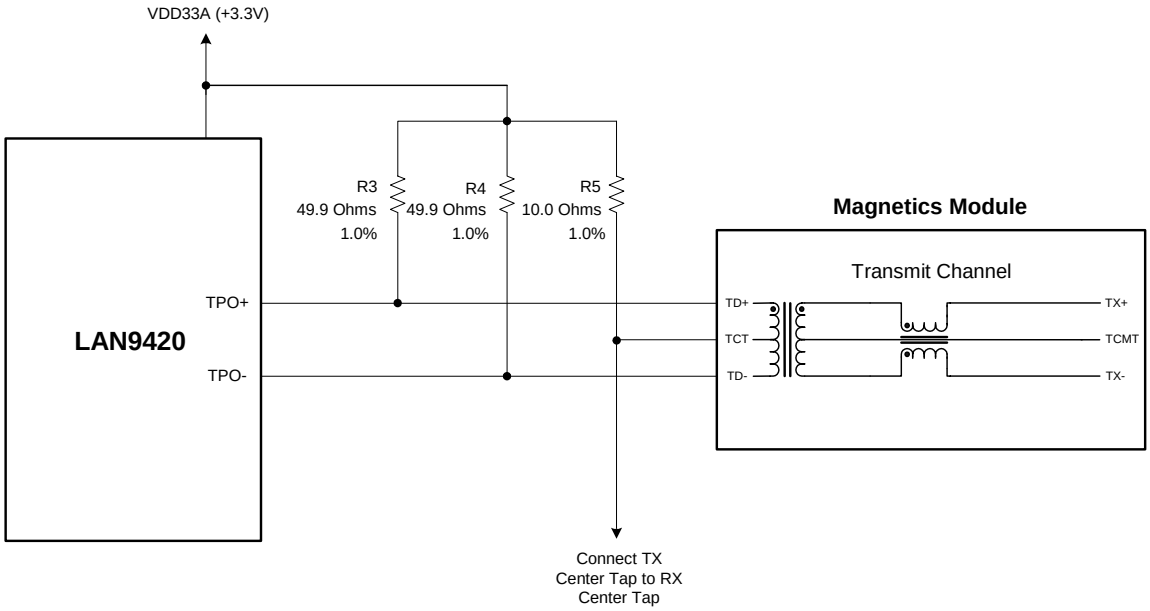

Figure 1 – Transmit Channel Connections and Terminations

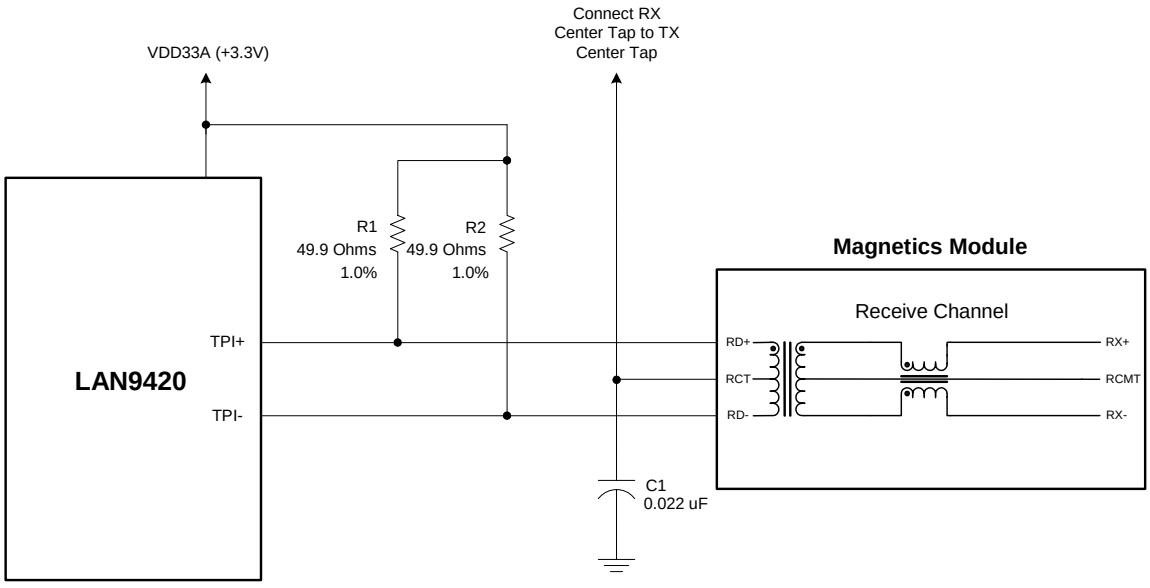

Figure 2 - Receive Channel Connections and Terminations

LAN9420 VTQFP Magnetics:

1. The center tap connection on the LAN9420 side for the transmit channel must be connected to VDD33A (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the primary magnetics also connects to the receive channel center tap of the primary magnetics.

2. The center tap connection on the LAN9420 side for the receive channel is connected to the transmit channel center tap on the primary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the primary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the primary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the primary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TPO+ (pin 101) of the LAN9420 VTQFP.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TPO- (pin 100) of the LAN9420 VTQFP.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to TPI+ (pin 106) of the LAN9420 VTQFP.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to TPI- (pin 104) of the LAN9420 VTQFP.

10. When using the SMSC LAN9420 Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 “Suggested Magnetics” for proper magnetics.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

+3.3V Power Supply Connections:

1. The digital supply (VDD33IO) pins on the LAN9420 VTQFP are 3, 5, 6, 7, 13, 21, 28, 36, 43, 51, 58, 67, 74, 81 & 90. They require a connection to +3.3V.

2. Each VDD33IO power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9420. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD33A) pins for the Phy in the LAN9420 VTQFP are pins 103 & 107. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD33A pin should have one .01 μF (or smaller) capacitor to decouple the LAN9420. The capacitor size should be SMD_0603 or smaller.

5. VDD33BIAS (pin 111), this pin serves as the master bias voltage supply for the LAN9420. Since this pin is analog based, this pin requires a direct connection to VDD33A.

6. The VDD33BIAS pin should have one .01 μF (or smaller) capacitor to decouple the LAN9420. The capacitor size should be SMD_0603 or smaller.

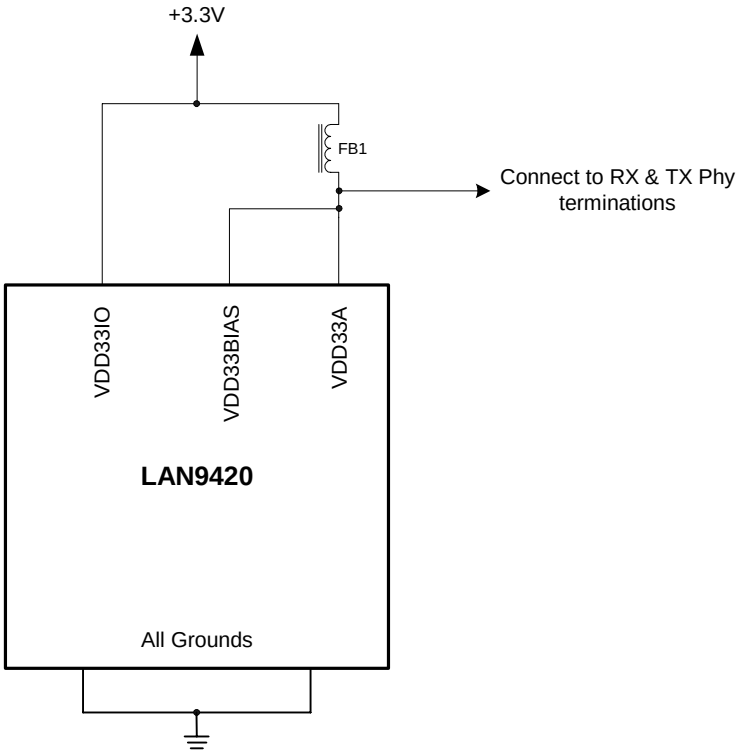

Figure 3 – LAN9420 +3.3V Power Connections

VDD18CORE:

1. VDD18CORE (pins 8, 9 & 82), these three pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF bypass capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 8 requires a bulk capacitor placed as close as possible to pin 8. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 0.1 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only and LAN9420 use only. **Do Not** power other circuits or devices with this supply.

2. VDD18PLL (pin 117), this pin supplies power for the core PLL. This pin must be connected to VDD18CORE through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

3. The VDD18PLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN9420. The capacitor size should be SMD_0603 or smaller.

4. VDD18TX (pin 116), this pin supplies power for the Phy. This pin should be connected to VDD18PLL.

5. The VDD18TX pin should have one .01 μF (or smaller) capacitor to decouple the LAN9420. The capacitor size should be SMD_0603 or smaller.

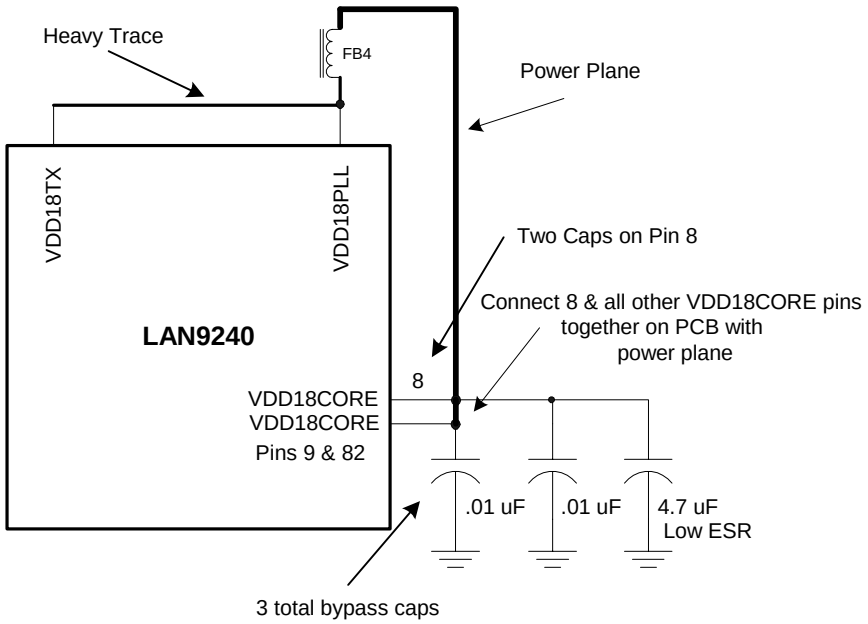

Figure 4 LAN9420 +1.8V Power Connections

Ground Connections:

1. The digital ground pins (VSS) on the LAN9420 VTQFP are 4, 10, 11, 12, 20, 27, 35, 42, 49, 50, 57, 66, 73, 80, 83, 89, 99, 102, 108, 110 & 118. They need to be connected directly to a solid, contiguous ground plane.

2. We recommend that the Digital Ground pins and all ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9420 VTQFP. For exact specifications and tolerances refer to the latest revision LAN9420 data sheet.

2. XI (pin 120) on the LAN9420 VTQFP is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 119) on the LAN9420 VTQFP is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

EEPROM Interface:

1. EECS (pin 94) on the LAN9420 VTQFP connects to the external EEPROM's CS pin.

2. EECLK (pin 95) on the LAN9420 VTQFP connects to the external EEPROM's serial clock pin.

   Caution: To ensure normal device operation, the EECLK pin must be high during any power-up and/or hardware reset event. Do not add any type of external pull-down or grounding connection to this pin as this will result in configuring the device disabled.

3. EEDIO (pin 92) on the LAN9420 VTQFP connects to the external EEPROM's Data In pin. This pin on the LAN9420 is a bi-directional pin and it also connects to the EEPROM's Data Out pin through a 1.0K Ω resistor.

4. Be sure to select a 3-wire style 1K EEPROM that is organized for 128 x 8-bit or the ability to be strapped for 128 x 8-bit operation. Recommended EEPROMs can be found in our LAN9118 Designing with the LAN9118 - Getting Started design guide, application note AN 12.5.

EXRES Resistor:

1. EXRES (pin 109) on the LAN9420 VTQFP should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

Required External Pull-ups/Pull-downs:

1. GPIO0/nLED1 (pin 123) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

2. GPIO1/nLED2 (pin 1) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

3. GPIO2/nLED3 (pin 2) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

PCI Bus Required External Pull-ups:

1. When implementing the LAN9420 device in an embedded application, the PCI control signals require pull-up resistors on the system board (not an add-in card). These resistors should be pulled up to the V_{CC} of the signaling environment. These pull-ups ensure stable signal values when no agent is actively driving the bus. Typical pull-up resistor values for all subsequent pins are 2.7K ohms for +5V signaling rail or 8.2K ohms for +3.3V signaling rail.

2. nFRAME (pin 48), this pin is the PCI Cycle Frame signal and requires a pull-up resistor.

3. nTRDY (pin 53), this pin is the PCI Target Ready signal and requires a pull-up resistor.

4. nIRDY (pin 52), this pin is the PCI Initiator Ready signal and requires a pull-up resistor.

5. nDEVSEL (pin 54), this pin is the PCI Device Select signal and requires a pull-up resistor.

6. nSTOP (pin 55), this pin is the PCI Stop signal and requires a pull-up resistor.

7. nSERR (pin 59), this pin is the PCI System Error signal and requires a pull-up resistor.

8. nPERR (pin 56), this pin is the PCI Parity Error signal and requires a pull-up resistor.

9. nINT (pin 14), this pin is the PCI Interrupt pin, it is an open-drain output and requires a pull-up resistor.

10. nPME (pin 19), this pin is the PCI Power Management Event signal, it is an open-drain output and requires a pull-up resistor.

11. nREQ (pin 18), this pin is the PCI Bus Request signal and requires a pull-up resistor.

12. PCInRST (pin 15), this pin is used to bring PCI-specific registers, sequencers and signals to a consistent state and requires a pull-up resistor.

PCI Device Interface:

1. AD[31:0] Address & Data Bus: Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. All AD[31:0] signals should be bussed accordingly to the PCI Bus.

2. PCICLK (pin 16), this clock is an input used to provide timing for all transactions on the PCI Bus. The PCICLK is supplied from a PCI Host. The clock shall be in the range of 0 – 33 MHz.

3. PCInRST (pin 15), this pin is used to bring PCI-specific registers, sequencers and signals to a consistent state. This pin is an input and should be driven by the PCI Host.

4. nCBE[3:0] (pins 33, 47, 61 & 76), these pins are the multiplexed PCI bus command and byte enable signals. During the address phase of the transaction, nCBE[3:0] define the bus command. During the data phase, nCBE[3:0] are used as byte enables. These four signals are driven by the current Bus Master. These pins should be bussed to all other nCBE[3:0] signals on the PCI Bus.

5. nFRAME (pin 48), this pin is the PCI Cycle Frame signal and indicates the beginning and duration of an access. This signal is driven by the current Bus Master. This signal should be bussed to all other nFRAME signals on the PCI Bus.

6. nIRDY (pin 52), this pin is the PCI Initiator Ready signal and indicates the Bus Master's ability to complete the current data phase of the transaction. During a write, nIRDY indicates that valid data is present on AD[31:0]. During a read, it indicates the master is prepared to accept data. It is used in conjunction with nTRDY and wait cycles are inserted until both nIRDY and nTRDY are asserted together. This signal is driven by the current Bus Master. This pin should be bussed to all other nIRDY signals on the PCI Bus.

7. nTRDY (pin 53), this pin is the PCI Target Ready signal and indicates the Target's ability to complete the current data phase of the transaction. During a read, nTRDY indicates that valid data is present on AD[31:0]. During a write, it indicates the Target is prepared to accept data. It is used in conjunction with nIRDY and wait cycles are inserted until both nIRDY and nTRDY are asserted together. This signal is driven by the current selected Target. This pin should be bussed to all other nTRDY signals on the PCI Bus.

8. nSTOP (pin 55), this pin is the PCI Stop signal and indicates the current Target is requesting the Master to stop the current transaction. This signal is driven by the current selected Target. This signal should be bussed to all other nSTOP signals on the PCI Bus.

9. nDEVSEL (pin 54), this pin is the PCI Device Select signal and indicates the device has decoded it's address as the target of the current transaction. This signal is driven by the current selected Target. As an input, nDEVSEL indicates whether any device on the bus has been selected. This signal should be bussed to all other nDEVSEL signals on the PCI Bus.

10. PAR (pin 60), this pin is the PCI parity signal and indicates even parity across AD[31:0] and nCBE[3:0]. This signal is driven by the current Master for address and write data phases; the Target drives PAR for read data phases. This signal should be bussed to all other PAR signals on the PCI Bus.

11. nPERR (pin 56), this pin is the PCI Parity Error signal and indicates an error in parity for all PCI transactions except a Special Cycle. This signal is driven by the agent receiving data. This signal should be bussed to all other nPERR signals on the PCI Bus.

12. nSERR (pin 59), this pin is the PCI System Error signal and indicates an error in parity for all address and data PCI transactions on the Special Cycle command or any other system error. This signal is driven by the agent reporting the error. This signal should be bussed to all other nSERR signals on the PCI Bus.

13. nINT (pin 14), this pin is the PCI Interrupt (nINT) output signal in Device Mode. Interrupts are defined as level triggered and active low. This signal should be connected to the Host's interrupt input pin.

14. nREQ (pin 18), this pin is the PCI Request signal and indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal and every Bus Master has it's own nREQx pin. The nREQ signal is a tri-state output.

15. IDSEL (pin 34), this pin is the PCI Initialization Device Select signal and is used as a chip select (input) during configuration read and write transactions. This signal is driven by the current Bus Master. A unique ADxx line should be used for the IDSEL input for each device and/or slot in the application.

16. nGNT (pin 17), this pin is the PCI Grant signal and indicates to the agents that access to the bus has been granted. This is a point-to-point signal and every Bus Master has it's own nGNTx pin. When in Device Mode, this signal is an input.

17. nPME (pin 19), this pin is the PCI Power Management Event signal and indicates that the device is requesting a change in the device or system power state. When in Device Mode, this signal is an open drain output.

18. VAUXDET (pin 122), this pin is used to sense the presence of a +3.3V Auxilliary power supply in order to define the PME support available. This pin is pulled low through an internal pull-down. This pin is an input for the LAN9420. When this pin is tied to the system's +3.3V_AUX power supply, wake from $D3_{COLD}$ is enabled. When tied to ground, no connection, wake from $D3_{COLD}$ is disabled. See the LAN9420 Data Sheet for further details.

19. PWRGOOD (pin 121), this pin is used to sense the presence of PCI Bus power during the D3 power management state. This pin is pulled low through an internal pull-down. This pin is an input for the LAN9420. If VAUXDET is low, PWRGOOD must be tied to +3.3V power (VDD33IO). PWRGOOD cannot be left as a no connection. See the LAN9420 Data Sheet for further details.

Miscellaneous:

1. There are 17 No-Connect pins on the LAN9420. It is very important that these pins remain as no-connects. These pins are 32, 63, 64, 91, 93, 96, 97, 98, 105, 112, 113, 114, 124, 125, 126, 127 & 128.

   Caution: To ensure normal device operation, pin 96 must be low at all times. Pin 96 has an internal pull-down. Do not add any type of external pull-up or other circuit connection to this pin as this will result in configuring the device disabled. This pin must be left as a No-Connect.

2. AUTOMDIX_EN (pin 115), this pin enables the HP Auto MDIX feature of the LAN9420.

   This pin has a weak internal pull-up, so this pin can be left as a no-connection in order to take advantage of the Auto MDIX feature (Auto MDIX enabled).

   To disable the Auto MDIX feature, a 1.0K Ω external pull-down resistor must be attached to this pin.

3. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

4. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

LAN9420 VTQFP QuickCheck Pinout Table:

Use the following table to check the LAN9420 VTQFP shape in your schematic.

LAN9420 VTQFP							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GPIO1/nLED2	33	nCBE3	65	AD14	97	NC7
2	GPIO2/nLED3	34	IDSEL	66	VSS	98	NC8
3	VDD33IO	35	VSS	67	VDD33IO	99	VSS
4	VSS	36	VDD33IO	68	AD13	100	TPO-
5	VDD33IO	37	AD23	69	AD12	101	TPO+
6	VDD33IO	38	AD22	70	AD11	102	VSS
7	VDD33IO	39	AD21	71	AD10	103	VDD33A
8	VDD18CORE	40	AD20	72	AD9	104	TPI-
9	VDD18CORE	41	AD19	73	VSS	105	NC9
10	VSS	42	VSS	74	VDD33IO	106	TPI+
11	VSS	43	VDD33IO	75	AD8	107	VDD33A
12	VSS	44	AD18	76	nCBE0	108	VSS
13	VDD33IO	45	AD17	77	AD7	109	EXRES
14	nINT	46	AD16	78	AD6	110	VSS
15	PCInRST	47	nCBE2	79	AD5	111	VDD33BIAS
16	PCICLK	48	nFRAME	80	VSS	112	NC10
17	nGNT	49	VSS	81	VDD33IO	113	NC11
18	nREQ	50	VSS	82	VDD18CORE	114	NC12
19	nPME	51	VDD33IO	83	VSS	115	AUTOMDIX_EN
20	VSS	52	nIRDY	84	AD4	116	VDD18TX
21	VDD33IO	53	nTRDY	85	AD3	117	VDD18PLL
22	AD31	54	nDEVSEL	86	AD2	118	VSS
23	AD30	55	nSTOP	87	AD1	119	XO
24	AD29	56	nPERR	88	AD0	120	XI
25	AD28	57	VSS	89	VSS	121	PWRGOOD
26	AD27	58	VDD33IO	90	VDD33IO	122	VAUXDET
27	VSS	59	nSERR	91	NC4	123	GPIO0/nLED1
28	VDD33IO	60	PAR	92	EEDIO	124	NC13
29	AD26	61	nCBE1	93	NC5	125	NC14
30	AD25	62	AD15	94	EECS	126	NC15
31	AD24	63	NC2	95	EECLK	127	NC16
32	NC1	64	NC3	96	NC6	128	NC17

Notes:

Reference Material:

1. SMSC LAN9420 Data Sheet; check web site for latest revision.
2. SMSC LAN9420 EVB Schematic, Assembly No. 6492; check web site for latest revision.
3. SMSC LAN9420 EVB PCB, Assembly No. 6492; order PCB from web site.
4. SMSC LAN9420 EVB PCB Bill of Materials, Assembly No. 6492; check web site for latest revision.
5. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.